Position : Static Timing Analysis Lead

Job Overview

Position Title: Static Timing Analysis Lead

Location: Bangalore

Primary Skills: EDA Tool Expertise, Static Timing Analysis (STA) Flow Development – Multi-mode, multi-corner (MMMC), SI analysis, OCV/AOCV/POCV/LVF modelling, Timing Signoff Methodology, Constraint Development & Validation.

Experience Level: 7–18 years.

Salary Package: Best in the Industry.

Job Type: Full-Time, 5 days' work from office.

Job Description

Semiconductors | AI | Networking | ASIC Design.

Role Overview

We're looking for an experienced and driven Static Timing Analysis (STA) and Timing Signoff Methodology lead. In this role, you'll be the expert responsible for defining, developing, and maintaining the entire STA flow and signoff methodology for our cutting-edge SoCs and IPs. Your work is crucial for ensuring our complex, high-performance designs meet their timing goals and are first-pass successful.
You'll be tackling challenges at advanced process nodes and directly influencing the performance and reliability of our next-generation products.

Key Responsibilities

- STA Flow Development: Design, build, and maintain a robust, automated, and scalable STA infrastructure. This includes flows for various modes and corners, signal integrity (SI) analysis, and on-chip variation (OCV) modelling.

- Timing Signoff Methodology: Define the signoff criteria and methodology for all projects. Ensure timing closure with the highest accuracy and correlation with silicon performance. This includes developing methodologies for handling new challenges at advanced nodes (eg.5nm and below).
- Constraint Development & Validation: Develop a comprehensive methodology for creating and validating SDC (Synopsys Design Constraints). Build automated checks and tools to ensure the quality and correctness of timing constraints throughout the design cycle.
- Tool & Flow Automation: Create and manage scripts (TCL, Perl, Python) to automate the timing signoff process, generate reports, and improve overall productivity for the design teams.
- Technical Support & Guidance: Act as the primary technical contact for all STA-related issues. Provide expert-level support to RTL and physical design teams on timing closure, constraint issues, and advanced STA techniques.
- EDA Vendor Collaboration: Work closely with EDA vendors (like Synopsys, Cadence) to resolve tool bugs, deploy new features, and drive their tool roadmaps to meet our technical needs.
- Advanced STA Techniques: Lead the evaluation and implementation of advanced timing methodologies, including statistical static timing analysis (SSTA), variation-aware modelling, and hierarchical STA flows.

Required Skills and Qualifications

- Education: A Bachelor's or Master's degree in Electrical Engineering (EE), Computer Engineering (CE), or a related field.
- Experience: A minimum of 7-18+ years of hands-on experience in Static Timing Analysis and timing closure on large-scale, high-performance designs.
- Expert Tool Knowledge: Deep, hands-on expertise with industry-standard STA tools, primarily Synopsys Primetime (PT). Familiarity with alternative tools is a plus.
- Timing Concepts: A profound understanding of core STA concepts, including:
    - SDC (Synopsys Design Constraints) and constraint generation.
    - Crosstalk (SI), noise analysis, and mitigation techniques.
    - On-Chip Variation (AOCV, POCV, LVF) and statistical timing.
    - Clock and data path analysis, and multi-mode, multi-corner (MMMC) analysis.

- Scripting Proficiency: Strong scripting skills are a must. High proficiency in TCL is essential, with strong capabilities in Perl or Python.
- Process Nodes: Experience with designs on advanced FinFET nodes (16nm and below) is highly desirable.
- Problem-Solving: Excellent analytical and debugging skills with a proven track record of solving complex timing closure and methodology challenges.
- Communication: Strong communication and interpersonal skills, with the ability to effectively collaborate with various teams and clearly document methodologies.

Preferred Qualifications

Master's or PhD in Electrical Engineering, Computer Engineering, or related field.

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