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ELEC3500: Digital Electronics

LAB 3: CMOS Combinational Logic

Lab Section: A3 Tuesday 11:30a.m. – 2:30p.m.

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1. The MUX

Q1.

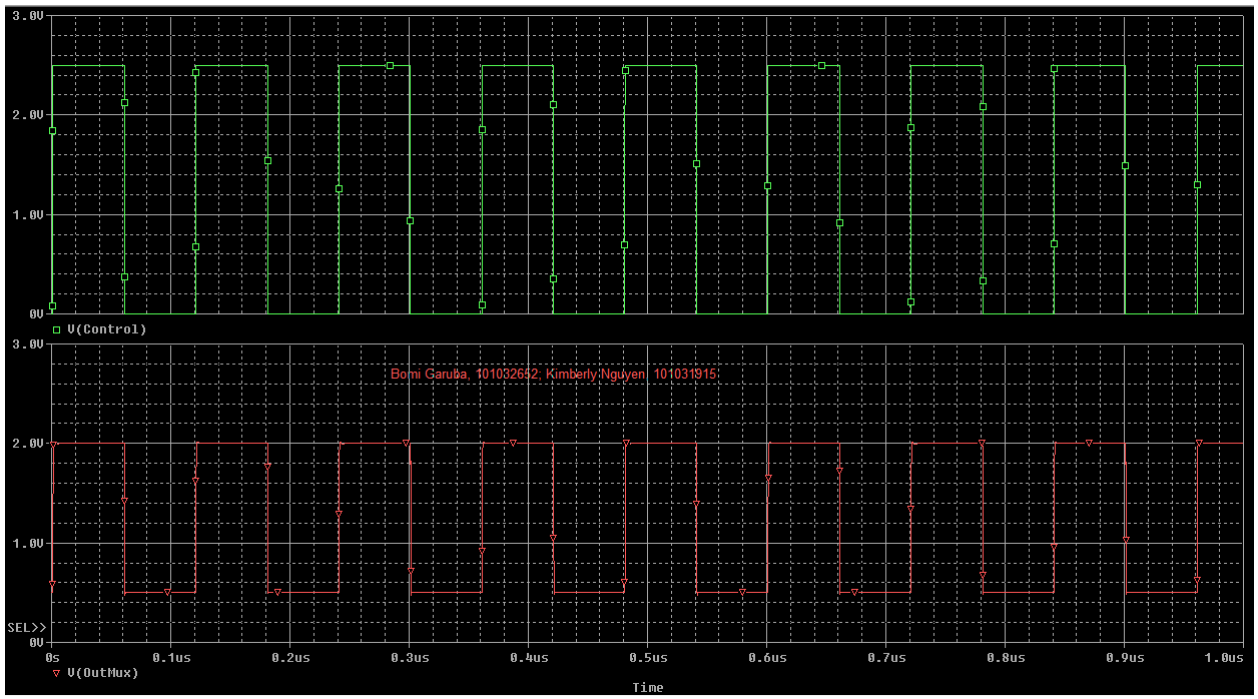

Fig 1. Output waveforms for CTRL and Y signals

When the CLK is high, the "d" transmission gate turns ON (why? Because its PMOS component is being fed $CLK_{inverse}$ Which is low it turns ON and its NMOS component is getting CLK that which is high). Input thus latches to "d".

When the CLK is low, the "q" transmission gate turns ON (why? Because its PMOS component is being fed CLK Which is low it turns ON and its NMOS component is getting $CLK_{inverse}$ that which is high). Input thus latches to "q".

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Q2.

Trace Color	Trace Name	Y1	Y2	Y1 - Y2
	X Values	301.150n	301.383n	-232.677p
	V(OUTMUX)	1.9151	1.2520	663.171m
CURSOR 1,2	V(Control)	1.2529	0.000	1.2529

Fig 2. Measuring time from Control High to Y Valid

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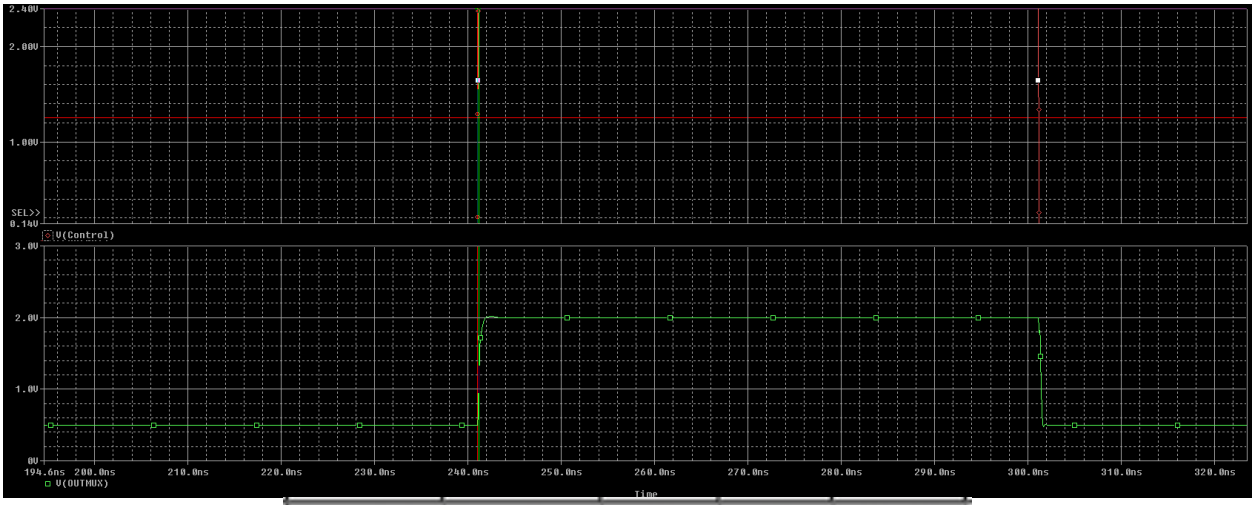

Trace Color	Trace Name	Y1	Y2	Y1 - Y2
	X Values	241.050n	241.188n	-137.792p
	V(OUTMUX)	527.586m	1.1690	-641.379m
CURSOR 1,2	V(Control)	1.2528	2.5000	-1.2472

Fig 3. Measuring time from Control Low to Y Valid

By simulation and observation, the times from control low/high to Y valid were measured to be:

- $t_{CHYV} = 232.677\ ps$
- $t_{CLYV} = 137.792\ ps$

2. The D-Latch

Q3.

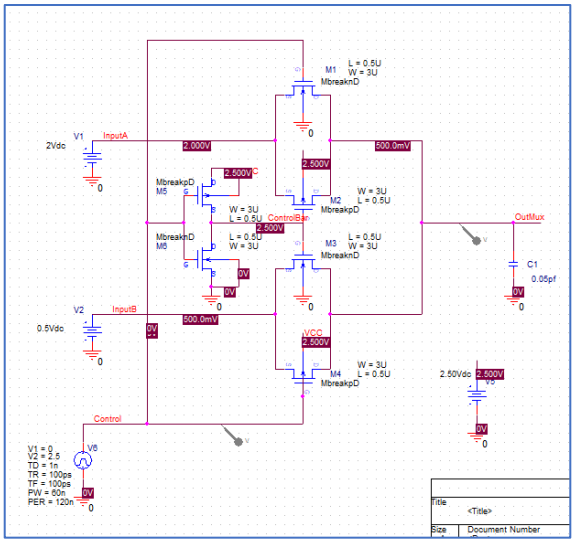

Fig 4. MUX Circuit schematic

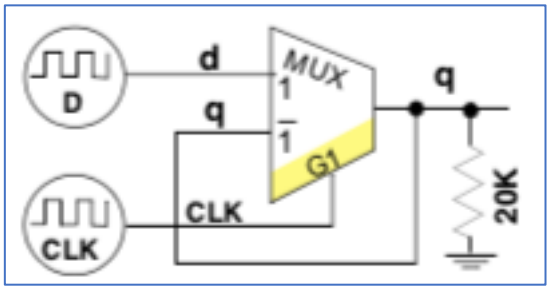

Fig 5. D-Latch using MUX

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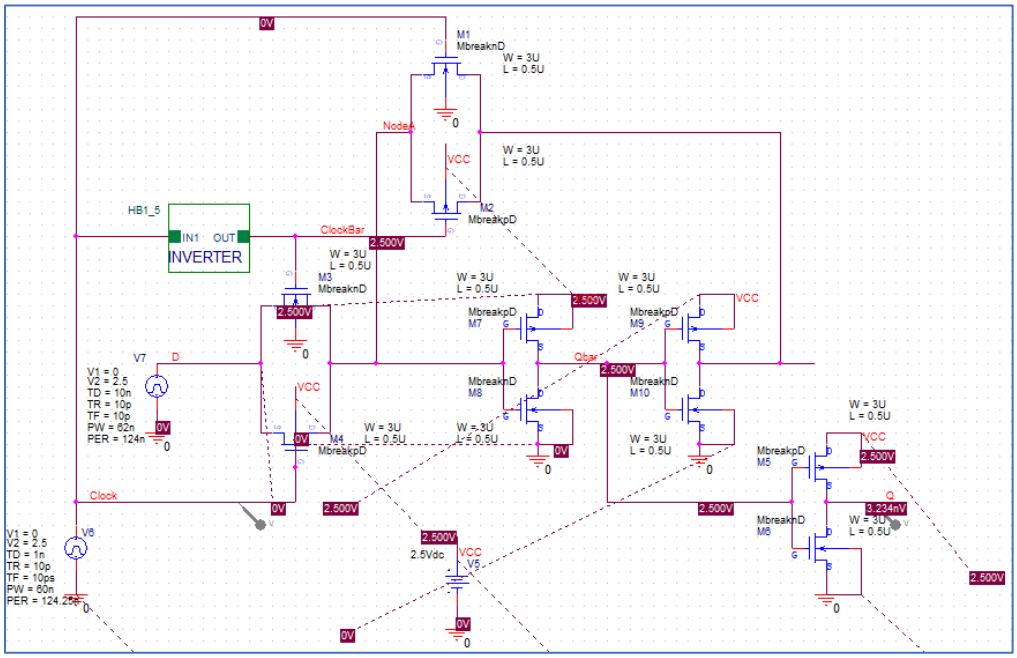

Fig 6. D-Latch Circuit schematic with added parts

A 2:1 multiplexer selects between two inputs depending upon the value of its select input. Also, a latch holds its previous value when its enable pin is in a particular state (‘0’ for positive level sensitive latch and ‘1’ for negative level sensitive latch). To achieve this, a connection was made from the output of the MUX (Qbar) to the 0 input, to create a feedback. Inverters were also added to Qbar to generate Q output. See figure below.

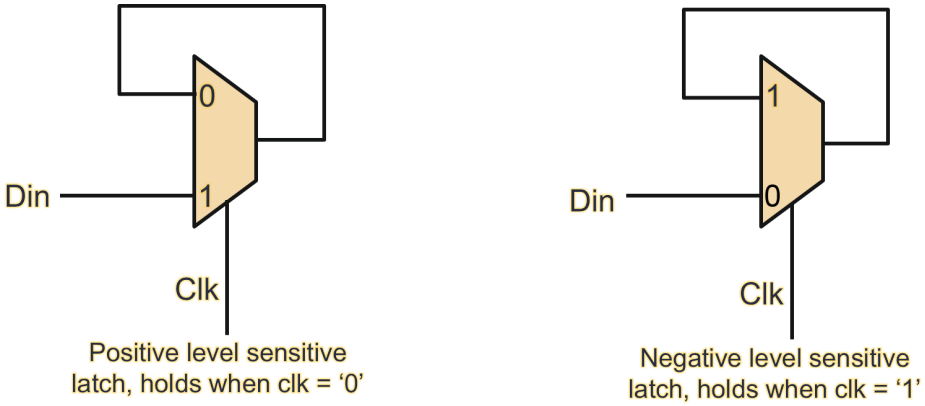

Fig 7. D-Latch created from MUX

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Q4.

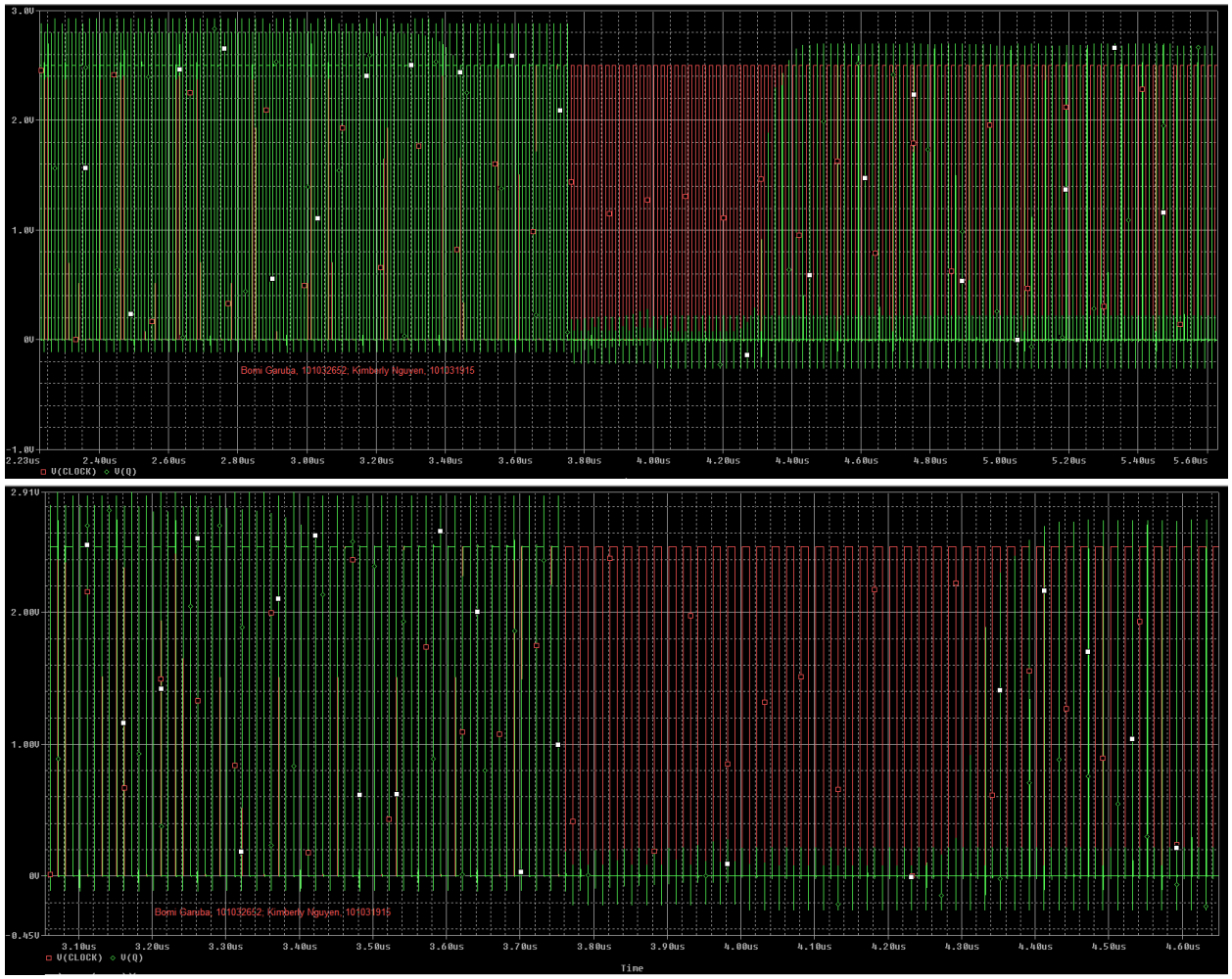

Fig 8. Waveform showing transparent latching

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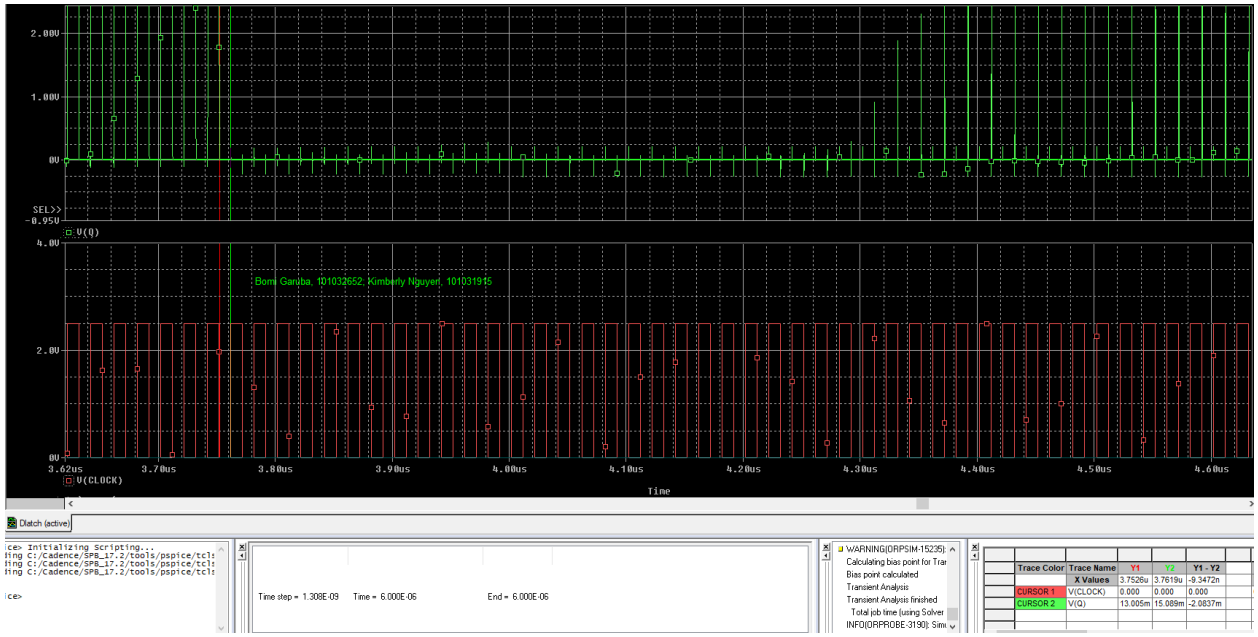
Q5.



Trace Color	Trace Name	Y1	Y2	Y1 - Y2
	X Values	3.7526u	3.7619u	-9.3472n
CURSOR 1	V(CLOCK)	0.000	0.000	0.000
CURSOR 2	V(Q)	13.005m	15.089m	-2.0837m

Fig 4. Measuring setup time for Latch circuit

Setup time is seen to be 9.347ns.

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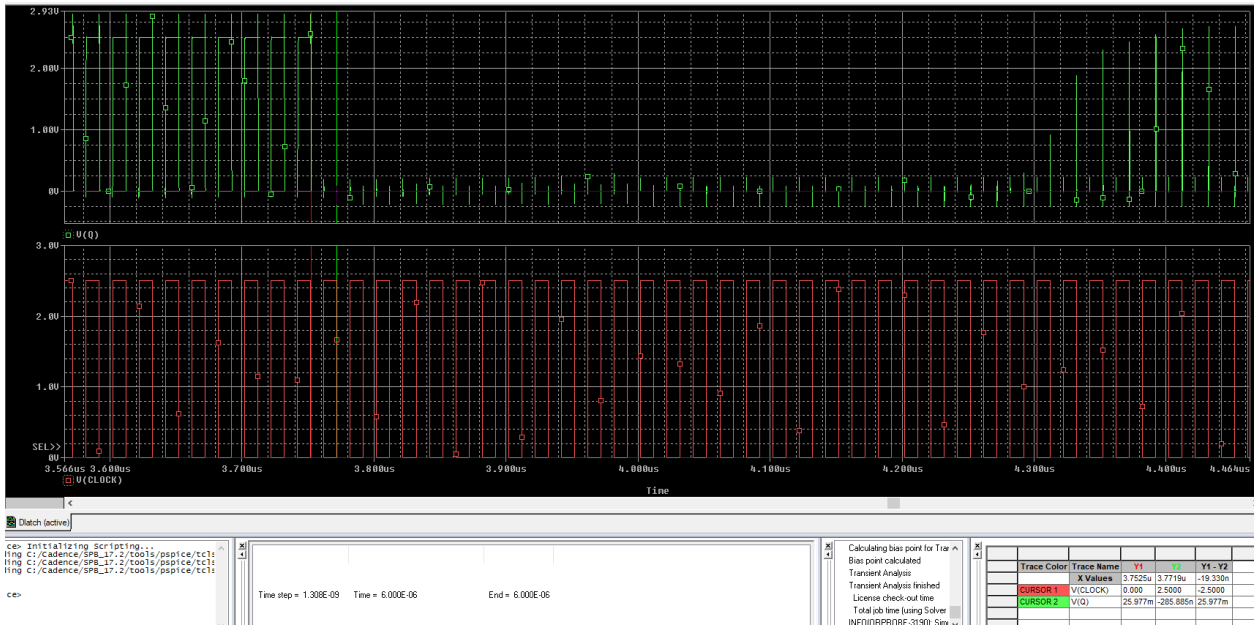
Q6.



Trace Color	Trace Name	Y1	Y2	Y1 - Y2
	X Values	3.7525u	3.7719u	-19.330n
CURSOR 1	V(CLOCK)	0.000	2.5000	-2.5000
CURSOR 2	V(Q)	25.977m	-285.885n	25.977m

Fig 5. Measuring setup time for Latch circuit containing 0.5pF

Capacitor

The delay setup time was noticed to have increased by 10 ns on Fig 5.It is now 19.33ns

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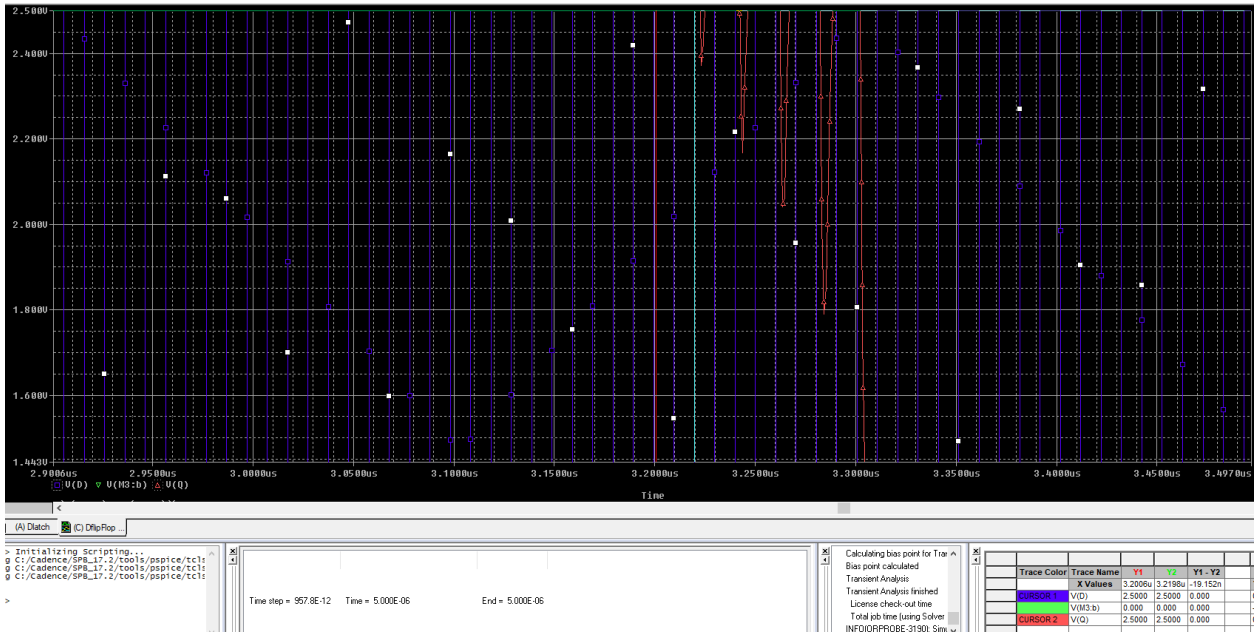
Q7.



Trace Color	Trace Name	Y1	Y2	Y1 - Y2
	X Values	3.2006u	3.2198u	-19.152n
CURSOR 1	V(D)	2.5000	2.5000	0.000
	V(M3:b)	0.000	0.000	0.000
CURSOR 2	V(Q)	2.5000	2.5000	0.000

Fig 6. Measuring setup time for D flip-flop at the first invalid V_{out} point

The setup time as shown is 19.152 s.

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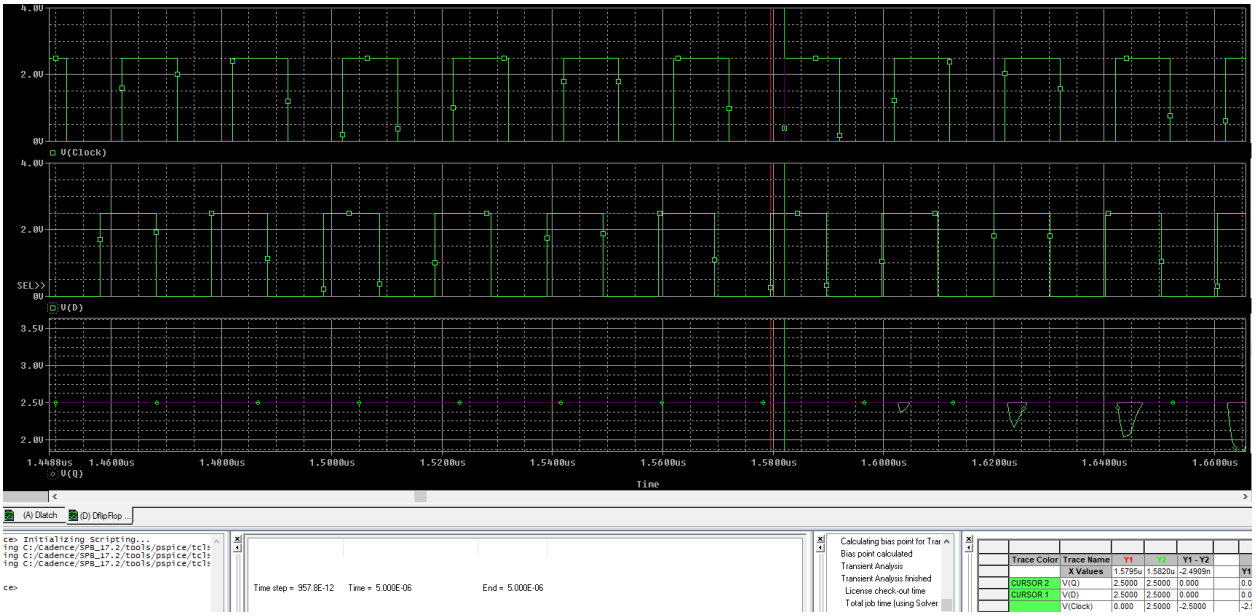

Trace Color	Trace Name	Y1	Y2	Y1 - Y2
	X Values	1.5795u	1.5820u	-2.4909n
CURSOR 2	V(Q)	2.5000	2.5000	0.000
CURSOR 1	V(D)	2.5000	2.5000	0.000
	V(Clock)	0.000	2.5000	-2.5000

Fig 7. Measuring setup time for D flip-flop at the last valid V_{out} point

The overall setup time I gotten by subtracting the setup time in Fig 7. From the time in Fig.6:

19.152ns – 2.4909ns = 16.66ns.