NOTE from Bomi Garuba: Due to the Data submission constraint on this application portal, I have taken the executive decision to cut up this Capstone report into a shorted file with sections 3 and 4 taken out. This submission is just to provide an illustration of the professional engineering graduate attributes acquired from Carleton University.

ELEC 4907 Capstone Engineering Project Report:

An Adaptive Phased Array Beamformer for 5G

ADAR 1000™ X-Band Beamformer Replication Prototype

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Abstract

5G communication, the cutting edge of wireless network capabilities for the 21st century. Through high density fiber optic cables layered on ocean floors and high-frequency tracking cellular towers 5G networks have a foundation to handle the astronomical demands of extensive clientele traffic. Adaptive 5G beamforming is a hot bed for communication network solutions as habits around remote professional work change not only in North America but the entire world. The goal of the project was research, design, verify, and create an adaptive 5G beamformer prototype layout with the purpose of taping out the complete circuit and getting it fabricated. The individual component of focus in this report includes the design of a Microcontroller based – RF Tx and Rx MMIC system and the implementation of a plausible beamforming algorithm to re-adjust the beam steering functionality of the prototype antennae. This report outlines the process of integrating MMIC sub-components through a serial peripheral interface for the adaptive controls' functionality of the prototype. Overall, the design and layout portion of the project was partially completed.

Contents

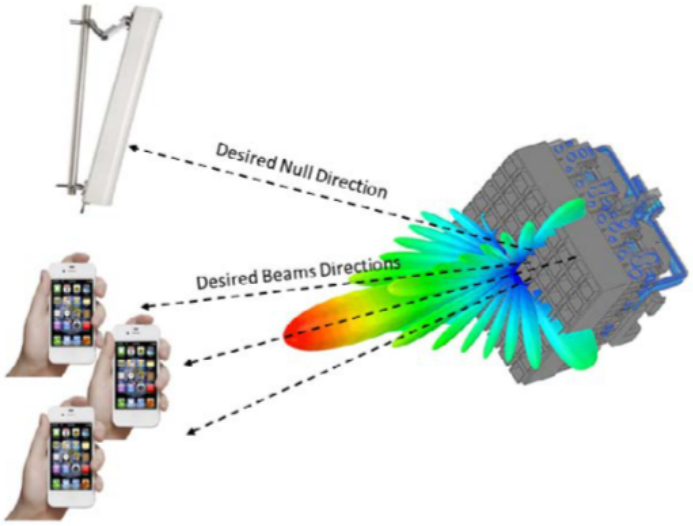
1 Report Symbols and Nomenclature

Showings:

- ADC: Analog to Digital Convertor
- ANT: Antenna Array Module
- ATN: Attenuetor Module
- AWGN: Additive white Gaussian noise
- BER: Bit Error Rate
- CDMA: Code Division Multiple Access
- CMOS: Complementary Metal-Oxide Semiconductor
- DAC: Digital to Analog Convertor
- DOA: Direction of Arrival
- DRR: Double Ring Resonator
- DVB: Digital Video Broadcasting
- EIRP: Effective Isotropic Radiated Power
- FDTD: Finite Difference Time Domain
- FIR: Finite Impulse Response
- HPBW: Half Power Beam-Width
- IF: Intermediate Frequency
- IL: Insertion Loss
- LHCP: Left Hand Circular Polarization
- LCMV: Linearly Constrained Minimum Variance
- LMS: Least Mean Square
- LNA: Low Noise Amplifier
- LO: Local Oscillator
- LOS: Line Of Sight for Boresight
- MMW: Milli-Meter Wave
- MVDR: Minimum variance distortionless response
- NF: Noise Figure
- NZR: Non-Return-to-Zero
- EIRP: Effective Isotropic Radiated Power
- PAA: Phased Array Antenna
- PDF: Probability Density Function
- PHS: Phase Shifter Module
- RF: Radio Frequency
- SPI: serial peripheral interface
- SNR: Signal to Noise Ratio
- SWT: Single Pole, Double Throw (SPDT) Level Switch
- WPAN: Wireless Personal Area Network

2 Project Introduction

The objective of this phased array antenna transceiver system prototype, through proposed design and fabrication, is to achieve similar, or better, beam signal characteristics of the commercially available ADAR 1000™[1] X-Band Beamformer module from Analog Devices, Inc. The following sections provide a prerequisite overview, RF background, and project motivations for endeavoring in the project, as well as going through design objectives, specifications and relevant publications.



(a) Functionality of a Planar Phased Array Beamformer[2]

2.1 Overview

- RF Tx and Rx systems controls: Micro-controller SPI interface
- MMIC Component: Phase Shifter
- MMIC Component: Attenuetor
- MMIC Component: SPDT Switch
- 2x2 Phased Array Transceiver: Patch Antenna

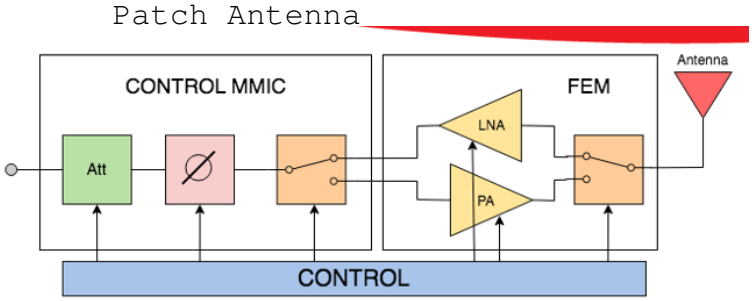


Figure 4. Subsystems of a transmit/receive module in one array

Figure 3: Proposed Adaptive Phased Array Beamformer Project Prototype Architecture for 1 array sub-block

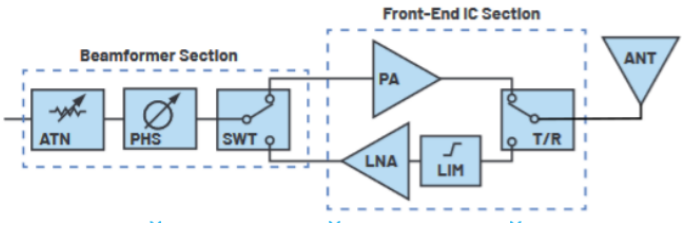
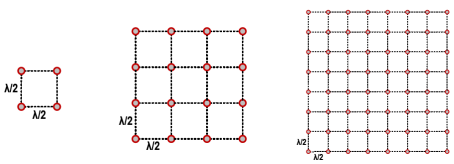


Figure 2: ADAR 1000™[3] X-Band Beamformer Architecture for 1 array sub-block

The purpose of phased array antenna technology is to serve as a medium to steer and augment high frequency (typically MMW) beam signals to a similar or better degree of efficiency than that of traditional rotating antenna gimbals. The functionality that champions phased array technology over the ancient rotating gimbals is that phased array technology does not require mechanical movement to steering the beam signals. The RF signal transceiver detection is all done electronically in phased arrays by controlling phase or time delay across array elements.

This mode of signal modulation aims to create narrow, search-light beams that can track multiple targets with electronically variable phase shifter to conduct these rapid scans[4].



(a) Established Planar Phased Antenna Array Orientation[2]

(b) Traditional Rotating Antenna for WPAN

2.2 Description

There is a consistent design theme in the majority of the commercially available beamformer suite topologies that keeps the understanding

of the technology for newcomers in the simple Due to the forced lockdown, however, of most of the known world as a result of the early 2020 COVID-19 pandemic, enormous spikes in civilian households scattered across various regions in North America did not have the readily available adaptive 5G-phased array infrastructure to match with supply efficiently[5]. The 2 general challenges present in many scholarly resources on adaptive beam steering is that the distortive loss in signal strength as the Azimuth angle changes from the LOS in RF simulation environments:

5G BEAMFORMER DESIGN CHALLENGES

1. THE DYNAMIC IMPEADANCE BETWEEN THE PATCH ANTENNA ARRAY AND THE ANTENNA
   - → AS THE SCAN ANGLE OF THE ANTENNA CHANGES, THE EXCITATION ENERGY IN THE ARRAY ELEMENT CHANGE. THE EFFECT OF THAT IS A VICIOUS CYCLE OF A LOSS IN THE POWER OF THE MAIN BEAM LOBE ALONG WITH A FATTENING OF THE LOBE SHAPE THAT FURTHER EXAGGERATES THAT EXCITATION ENERGY CHANGE.
   - → IN THE EXTREME CASE OFF THIS LOSS OF POWER THERE WOUID BE A BLIND SPOT CREATED WHERE NO POWER IN THE MAIN LOBE FOR PICKING UP SIGNALS

* REFERENCE: "AN INTRODUCTION TO PHASED ARRAY DESIGN" BY Dr. NEIL TUCKER

ILLUSTRATION:

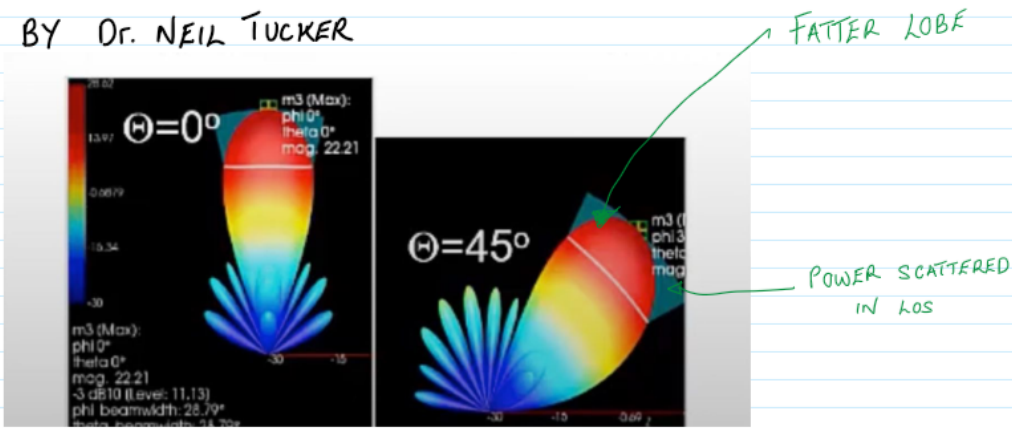
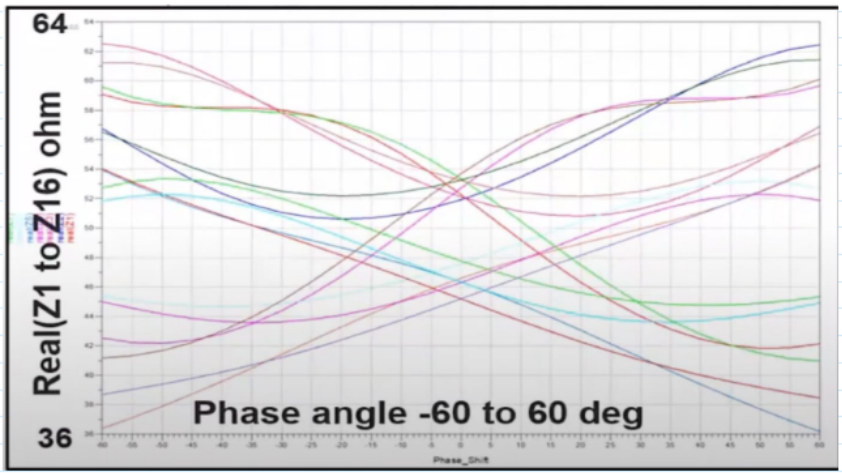


Figure 5: Beam Steering Control Challenge A[6]

2. ACTIVE INPUT IMPEDANCE COUPLING BETWEEN ARRAY ELEMENTS

→ THE EXPERIMENTAL CASE STUDIES OF E-PLANE AND H-PLANE COUPLING IN RECTANGULAR MICROSTRIP ANTENNAS SHOW THAT, IN THEORY, THE BUILT-IN INPUT IMPEDANCE OF EACH ELEMENT IN THE ARRAY STACK UP ARITHEMETICALLY ALONG EVERY ADJACENT ELEMENT IN THE ARRAY IF THE SPACING BETWEEN EACH PATCH IS LESS THAN 0.5 λ.



REFERENCE: "THE EFFECT OF MUTUAL COUPLING ON THE INPUT IMPEDANCE OF MICROSTRIP ARRAYS"
BY PROF. A.K BHATTACHARYYA &
PROF. L. SHAFAI

Figure 6: Beam Steering Control Challenge B[7]

artificially made market demand for improved internet network infrastructure.
The team carried out this project with an aptitude goal of learning the pre-existing constraints and restrictions on RF Phased Array technology in Canada and the educational goal of gaining first hand experience in digital IC design through Design, Simulation, Verification and Layout in 65nm CMOS process mediums.
I, personally, aim to use the experience gained with Microcontroller bit-banging into MMIC components for digital IC control to seek opportunities for career paths post graduation.

2.4 Design Objectives

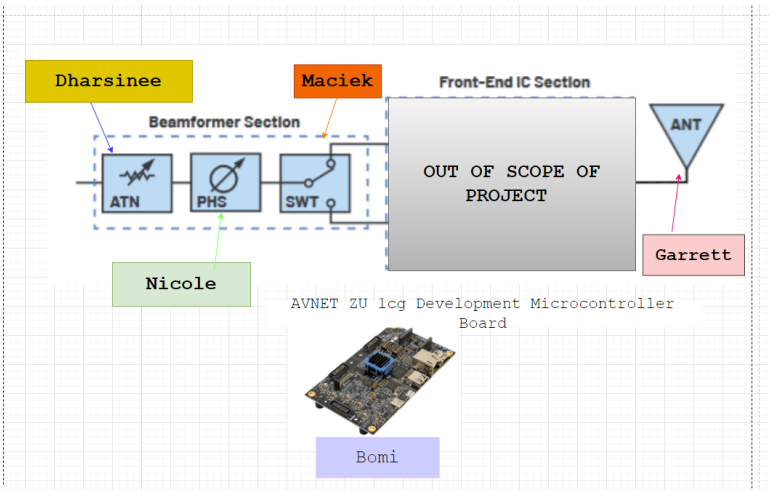


Figure 12: ADAR 1000™ X-Band Beamformer Replication Prototype Diagram

The design is composed of 5 main sub-assemblies, each of which has been delegated across the team to fit what each member is comfortable undertaking. A brief snapshot of what each component is and its functionality is shown below:

- 6-bit Digital Attenuetor: The ATN provides an amplitude taper across the beam signals to reduce the sidelobes (sidelobe going to null direction shown in Figure 1a on page 5)
- 6-bit Digital Phase Shifter: The PHS electronically shapes and steers the antenna beam to sharpen the shape of the main lobe, hence 'Phased Array Module' (main lobe picking up smartphone intended target clients shown in Figure 1a page 5).
- SPDT RF Switch: mm-wave pulse intermediary for switching between transmit and receive mode so that the number of antennae needed is reduced.

- 2x2 Patch Antenna Phased Array: Propagates the signal beam lobes (both main and side) for spacial multiplexing to multiple clients and Beam signal directivity.
- AVNET ZU Development Microcontroller Board: Performs the necessary mathematics to calibrate the phase shift angles between individual patch antennae components emitting/absorbing signal for beam steering while introducing as little noise as possible.

The sub-assembly of focus for this report is the Master Control Interface layout and MMIC control operation implementation through the Microcontroller selected.

2.5 Electronic Design Specifications

2.5.1 Group Specifications

The next logical step in the design process after gathering specifications was for each member to get a list of available industry-standard specifications for their sub-assembly that were realistic for our budget constrained prototype but keep it competitive with what the ADAR 1000™ could offer.

2.5.2 Technology Medium

The MMIC design of all components is tailored for the 65nm commercial CMOS process as it gives the best available power consumption management of the available medium while still being within the 'affordable' threshold for the team to make PCBs.

2.5.3 Bit Error Rate

The BER is a measure of how many bits the digital implementation of IC designs get corrupted die to factors ranging from wiring connection heat loss to noise input. The beam steering capabilities of the prototype rely heavily on this metric so much effort was devoted into finding industry standard mechanisms to achieve a BER of 10^{12} for this project.

2.5.4 Modulation Type

Describes the segmentation between digital data signals transmitted from a Microcontroller. The choice between Pulse-Amplitude Modulation (PAM) and Unipolar Non-Return-to-Zero (NRZ) used noise margin buffer as the criteria for which NRZ is the choice given the SPI master-slave operations of the Microcontroller and the MMIC sub components.

2.5.5 Power Supply

The supply will dictate the max and min voltage rails of the system. Due to absence of a strict low power consumption requirement, the supply will be 3V for this project

Range	Medium	Modulation	Supply
8.5 -10.5 GHz	65nm CMOS	NRZ	3.0V

Figure 13: Proposed System Specifications

2.5.6 Final Specifications

As the team member responsible for this projects RF Tx and Rx systems design, It falls onto me to ensure that the schematics and layouts of my team members working on the sub-assemblies that I will interfacing, via SPI, for the specifications fall in line with these set here. I made rigorous efforts to identify experimental MMICs strategies for integration and have proceeded with this:

Where my AVNET ZU Development Microcontroller Board will serve as the

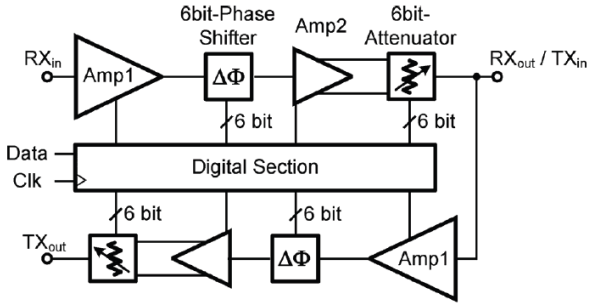


Figure 14: Adapted Integration strategies[9]

digital master control interface for this project.

2.6 Relevant Publications

The team researched and recovered a lost of various CMOS technology media and I have picked 3 that my project report will reference heavily:

- 'Development of a computationally efficient antenna beamforming algorithm and its implementation using FPGA'[10] by Mini P.R
- 'FPGA methodology for power analysis of embedded adaptive beamforming'[11] by O.T Waheed, A. Shabra, I.M Elfadel
- 'Performance Comparison and FPGA Synthesis of MNLMSNCMA Adaptive Beamforming Algorithms'[12] by Research India Publications

Office meetings with Dr. Amaya on average twice a week (predominately every Sunday and Friday as a backup if the Sunday session wasn't held). During these meetings, every group member shared their computer screens to showcase individual schematic issues, progress updates, and design breakthroughs that week and what they intend to accomplish in the following weeks. The purpose of this meeting is to enforce deadlines each week to keep the project progression owing, while also providing group members the opportunity to showcase their current work for possible questions and guidance from other members and the supervising professor.

- **3.3.3.3 Leadership, Initiative, and Mentoring Teammates**
  Given the added task of being the project prime, I was there to take the initiative to ask and get the response regarding the team's ADAR 1000™ delayed shipping request.

4 Theory and Techniques

4.1 Alternative Designs and Assessments

The most fundamental 'issue-to-solution' conundrum in the field of spacial filtering is that there is are sensor antennae positioned together, whether linearly or in a planar orientation, to give the main lobe beam constructive interference in a certain angle while simultaneously making the side lobes experience destructive interference[17].
Because this project wholly worries about being 'adaptive', conventional non-adaptive beamformers will be mentioned only in name but not looked into to for analysis. There are 6 main branches of modern adaptive beamforming algorithms, the most common and notable architecture choices in the articles found to be MVDR[18] and LCMV[19]

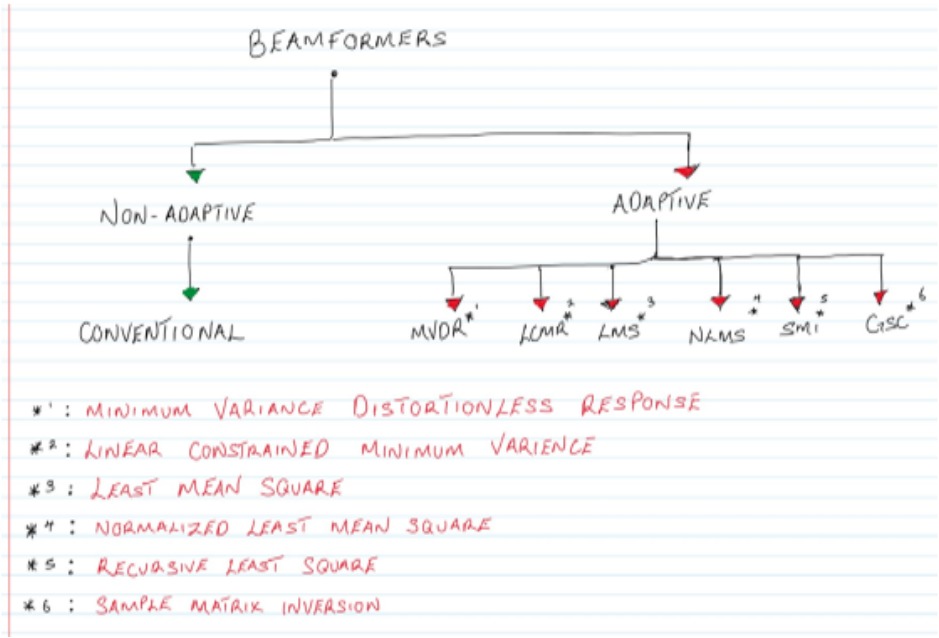


Figure 17: Beamforming tree

```
subplot(212)
plot(t,abs(yLCMV))
axis tight
title('LCMV (Adaptive) Beamformer')
xlabel('Seconds')
ylabel('Magnitude')
```

Figure 32: Step 6: MATLAB plot setup[20]

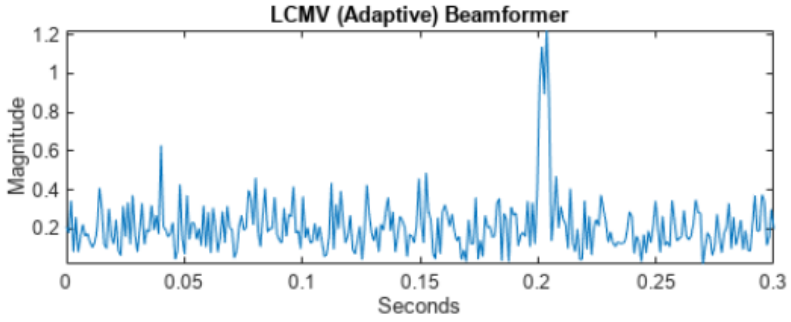


Figure 33: Step 7: LCMV beamformer Magnitude Plot.[20]

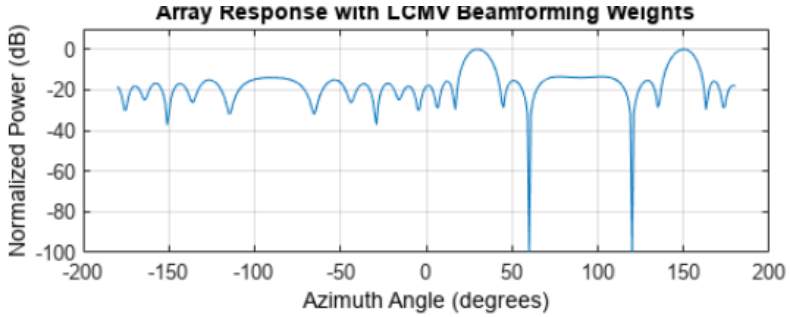


Figure 34: Step 8: LCMV beamformer Normalized Array Plot[20]

4.2 Chosen Design Details and Verification

4.2.1 LMS

The following section will provide structured detailing for the choice of this algorithm for the prototype, making reference to a list of proposed control signals from the 3 sub assembly components that the mirco-controller will be interfacing.

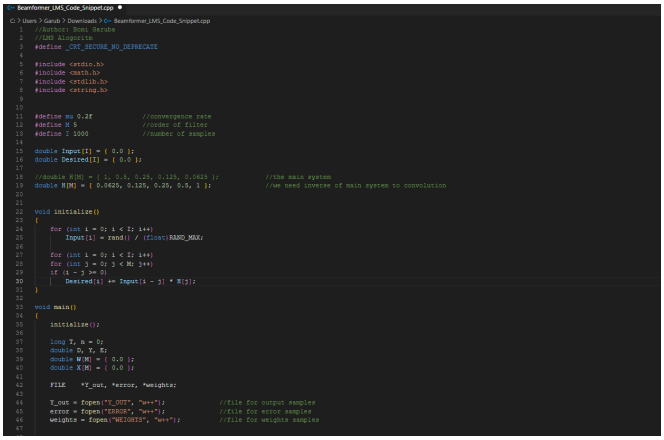
An LMS adjusts the weights of the antenna modules with respect to the environment elevation changes and is very popular as of all the options from the adaptive algorithms branch it over the most intuitive and robust computational quality of all options. It does have a slow rate of convergence if a requirement goal were rapid fire calibration.
The 2 main processes it makes use of are the estimation of a Y_n output compared with the desired gain response $Y_{n(\theta_d)}$ augmented by the estimation error (e_n) and the re-calibration of the beamformer weights in accordance with (e_n).

There is an alteration of the estimated gradient based on weight vector

update:

$$W_{(n+1)} = W_{(n)} + \mu \mathbf{X}_n e*_n \tag{2}$$

e_n is as a result of $Y_n - Y_{n(\theta_d)}$
The output is computed as: $Y_n = W_H \mathbf{X}_n$

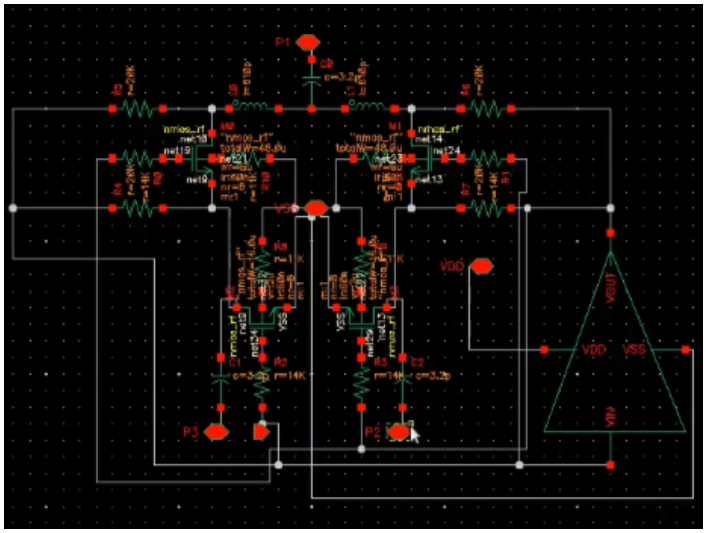


```
//Author: Bomi Garuba
//LMS Algorithm
#define _CRT_SECURE_NO_DEPRECATE

#include <stdio.h>
#include <math.h>
#include <stdlib.h>
#include <string.h>


#define mu 0.2f             //convergence rate
#define M 5                 //order of filter
#define I 1000              //number of samples

double Input[I] = { 0.0 };
double Desired[I] = { 0.0 };

//double H[M] = { 1, 0.5, 0.25, 0.125, 0.0625 };          //the main system
double H[M] = { 0.0625, 0.125, 0.25, 0.5, 1 };          //we need inverse of main system to convolution


void initialize()
{
    for (int i = 0; i < I; i++)
        Input[i] = rand() / (float)RAND_MAX;

    for (int i = 0; i < I; i++)
    for (int j = 0; j < M; j++)
    if (i - j >= 0)
        Desired[i] += Input[i - j] * H[j];
}

void main()
{
    initialize();

    long T, n = 0;
    double D, Y, E;
    double W[M] = { 0.0 };
    double X[M] = { 0.0 };

    FILE    *Y_out, *error, *weights;

    Y_out = fopen("Y_OUT", "w++");          //file for output samples
    error = fopen("ERROR", "w++");          //file for error samples
    weights = fopen("WEIGHTS", "w++");      //file for weights samples
```

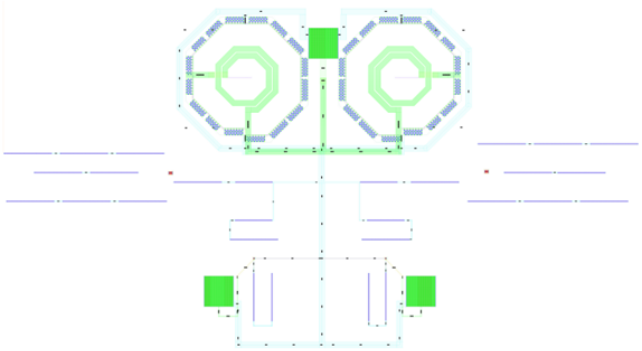
(a) C++ LMS beamformer code snippet 1

```
void main()
{
    initialize();

    long T, n = 0;
    double D, Y, E;
    double W[M] = { 0.0 };
    double X[M] = { 0.0 };

    FILE    *Y_out, *error, *weights;

    Y_out = fopen("Y_OUT", "w++");          //file for output samples
    error = fopen("ERROR", "w++");          //file for error samples
    weights = fopen("WEIGHTS", "w++");      //file for weights samples


    for (T = 0; T < I; T++)
    {
        for (int m = T; m > T - M; m--){
            if (m >= 0)
                X[M + (m - T) - 1] = Input[m];          //X new input sample for LMS filter
            else break;
        }

        D = Desired[T];                     //desired signal
        Y = 0;                                  //filter output set to zero

        for (int i = 0; i < M; i++)
            Y += (W[i] * X[i]);                 //calculate filter output

        E = D - Y;                              //calculate error signal

        for (int i = 0; i < M; i++)
            W[i] = W[i] + (mu * E * X[i]);      //update filter coefficients

        fprintf(Y_out, "\n % 10g % 10f", (float)T, Y);
        fprintf(error, "\n % 10g % 10f", (float)T, E);
    }

    for (int i = 0; i < M; i++)
        fprintf(weights, "\n % 10d % 10f", i, W[i]);

    fclose(Y_out);
    fclose(error);
    fclose(weights);
}
```

(b) C++ LMS beamformer code snippet 2



(a) Schematics from Maciek



(a) Virtuoso Layout from Maciek

Maciek's manual implementation of custom TSMC 65nm PDK – DETFF topology shown in figure 33 above with lumped components and NMOS as switch levels.

4.2.3 ADAR 1000™ EVAL kit

The section for testing the ADAR 1000™ had to be scraped but the software that would have been used is shown here

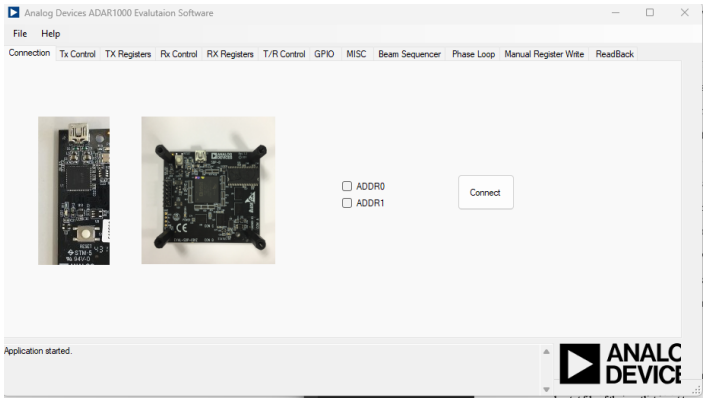


Figure 45: ADAR 1000™ control software interface: Connection

4.3 Experiment Design and Setup

4.3.1 Case 1 Scenario: IN Transmit Mode – Steering Beam – Controlling Phase Shifter with Microcontroller

The high level serial operation between the AVNET board and the Phase shifter module is done through a writing a digital byte word to a DAC to set an output voltage of logical HIGH(1.8V) or Logical Low(0V) to this the Phase Shifter peripheral.
An electrical specification and bias truth table for the phase shifter is shown below to understand what flags on the SPI control console will be set for accurate steering:

PARAMETER	CONDITIONS	MIN	TYPICAL	MAX	UNITS
Operating Range		8.5		10.5	GHz
RMS Phase Error	An N-bit has 2^N Phase States		<2.5		○
RMS Amplitude Error	An N-bit has 2^N Phase States		<0.45		dB

Table 1: 6-bit Phase Shifter Electrical Specifications for Prototype

Test conditions: 25° C; Control Voltage (REF, 5.625 °, 11.25 °,22.5°, 45°,90°,180°) = 0/+1.8V.
Features: 360° Coverage, LSB = 5.625°

SHIFTER	5.625°	11.25°	22.5°	45°	90°	180°	REF
0°(REF)	**0**	**0**	**0**	**0**	**0**	**0**	**1**
5°	**1**	**0**	**0**	**0**	**0**	**0**	**1**
11°	**0**	**1**	**0**	**0**	**0**	**0**	**1**
22°	**0**	**0**	**1**	**0**	**0**	**0**	**1**
45°	**0**	**0**	**0**	**1**	**0**	**0**	**1**
90°	**0**	**0**	**0**	**0**	**1**	**0**	**1**
180°	**0**	**0**	**0**	**0**	**0**	**1**	**1**

Table 2: 6-bit Phase Shifter Bias Truth Table for Prototype

Logic "0"= 0V , Logic "1"= +1.8V ; Voltage for Logic "1" of Vctrl (5.625°, 11.25°,22.5°,45°,90°,180°) must be the same as Vref

To try a case scenario for setting the phase shift to 45° offset from boresight, the voltage set in those should look like this:

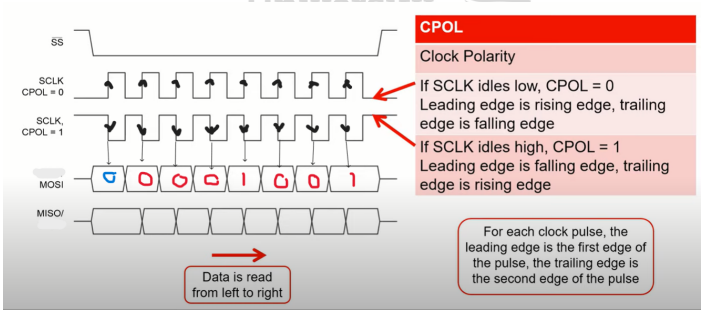


Figure 60: SPI data transfer from Master to Slave via DAC[21]

the Master out, Slave in is all that is needed to be observed as there is no need to get data back from the Peripheral (MISO) here of '**0001001**' to achieve a 45o steering. The Verilog code to implement this and feed into the LMS C++ file is:

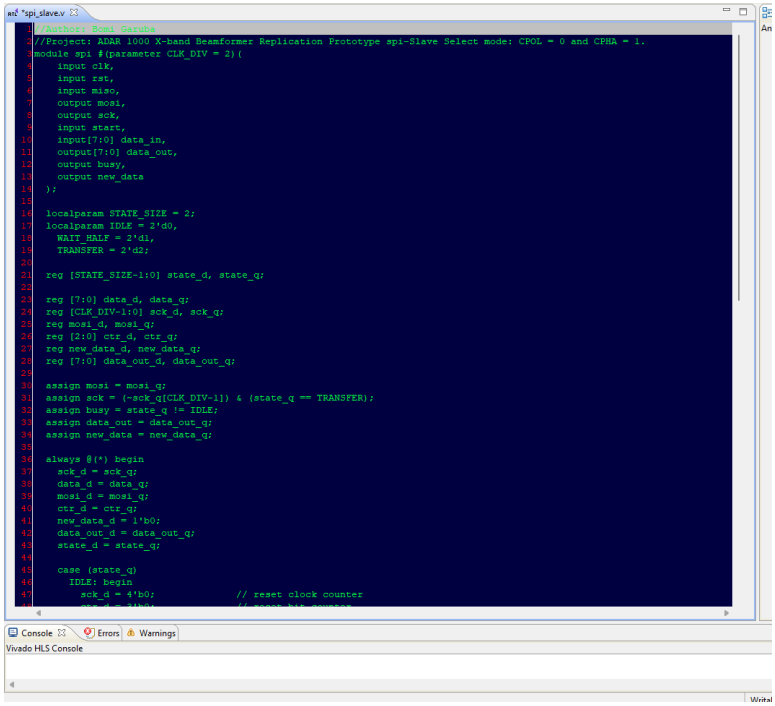


Figure 61: Verilog Code: Spi-Master.v

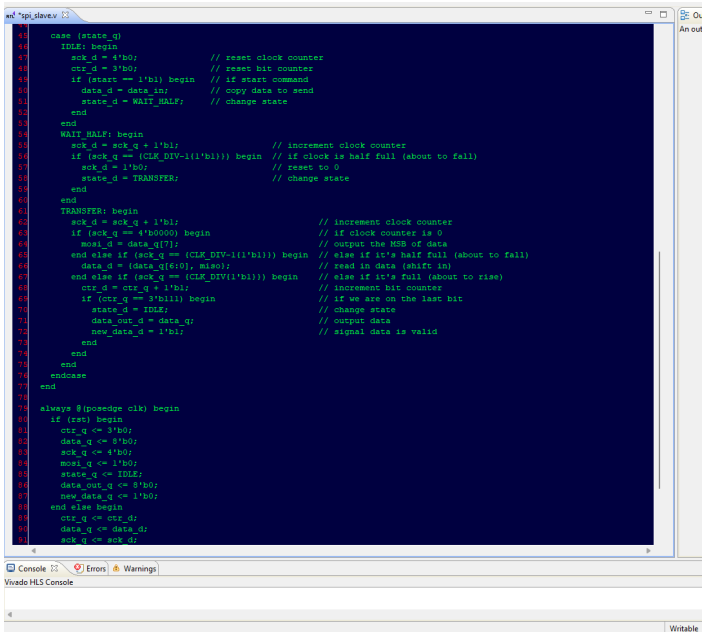


Figure 62: Verilog Code: Spi-Master.v

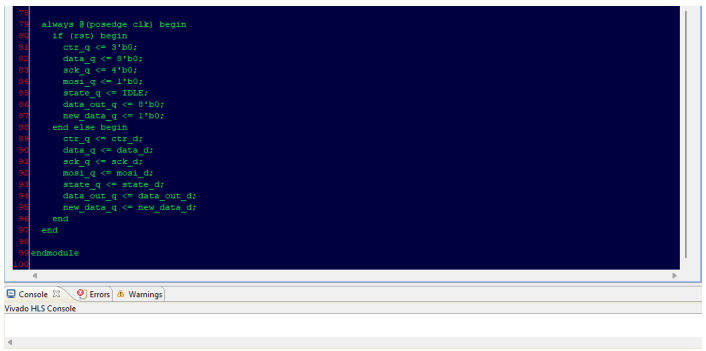


Figure 63: Verilog Code: Spi-Master.v

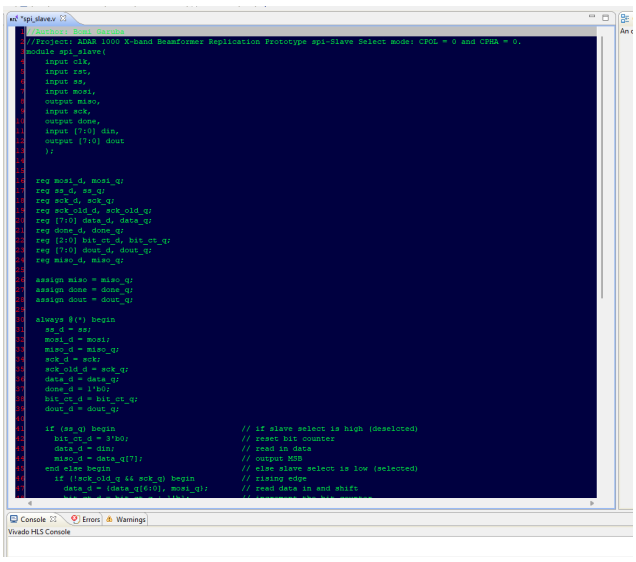
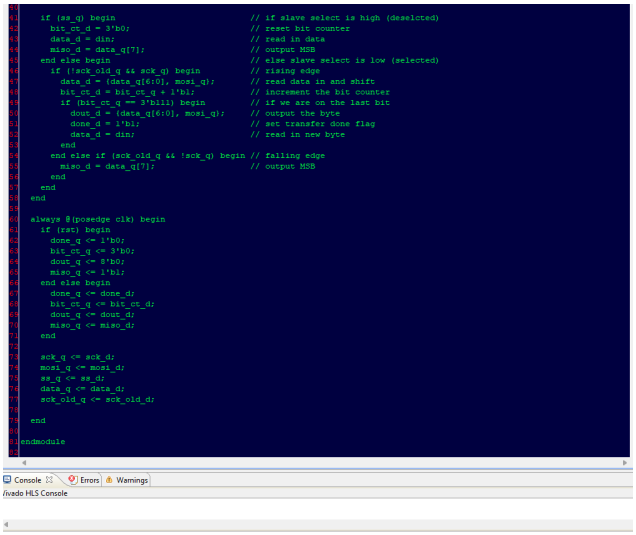


Figure 64: Verilog Code: Spi-Slave.v



```
  if (ss_q) begin                       // if slave select is high (deselcted)
    bit_ct_d = 3'b0;                    // reset bit counter
    data_d = din;                       // read in data
    miso_d = data_q[7];                 // output MSB
  end else begin                        // else slave select is low (selected)
    if (!sck_old_q && sck_q) begin      // rising edge
      data_d = {data_q[6:0], mosi_q};   // read data in and shift
      bit_ct_d = bit_ct_q + 1'b1;       // increment the bit counter
      if (bit_ct_q == 3'b111) begin     // if we are on the last bit
        dout_d = {data_q[6:0], mosi_q}; // output the byte
        done_d = 1'b1;                  // set transfer done flag
        data_d = din;                   // read in new byte
      end
    end else if (sck_old_q && !sck_q) begin // falling edge
      miso_d = data_q[7];               // output MSB
    end
  end
end

always @(posedge clk) begin
  if (rst) begin
    done_q <= 1'b0;
    bit_ct_q <= 3'b0;
    dout_q <= 8'b0;
    miso_q <= 1'b1;
  end else begin
    done_q <= done_d;
    bit_ct_q <= bit_ct_d;
    dout_q <= dout_d;
    miso_q <= miso_d;
  end

  sck_q <= sck_d;
  mosi_q <= mosi_d;
  ss_q <= ss_d;
  data_q <= data_d;
  sck_old_q <= sck_old_d;

end

endmodule
```

Console Errors Warnings

/ivado HLS Console

Figure 65: Verilog Code: Spi-Slave.v

The expectation from the implementation below is that the control voltages variables (Vctrl and NotVctrl) on the 6 phase shifter topologies will be set in this oversimplified orientation that should activate the 45° model only:

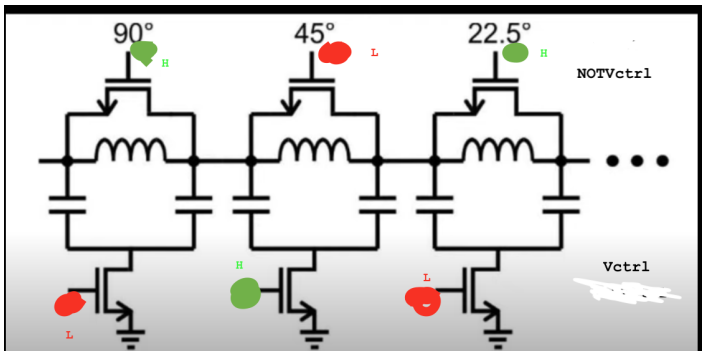


Figure 66: 45°(Vctrl = H, NotVctrl = L);
all others(Vctrl = L, NotVctrl = H)

4.4 Evaluation Measurement Technique

This is where the impact of the missing ADAR 1000™ module is felt the most for this project. The lack of a module to gauge and compare with makes it unwise to go straight into the fabrication initial intended for this prototype endeavour.
I had modelled a Planar Patch Antenna Calculator into Microsoft excel with the aim of simulating the orientation and showing close to matching theoretical results with the real world performance of the ADAR 1000™:

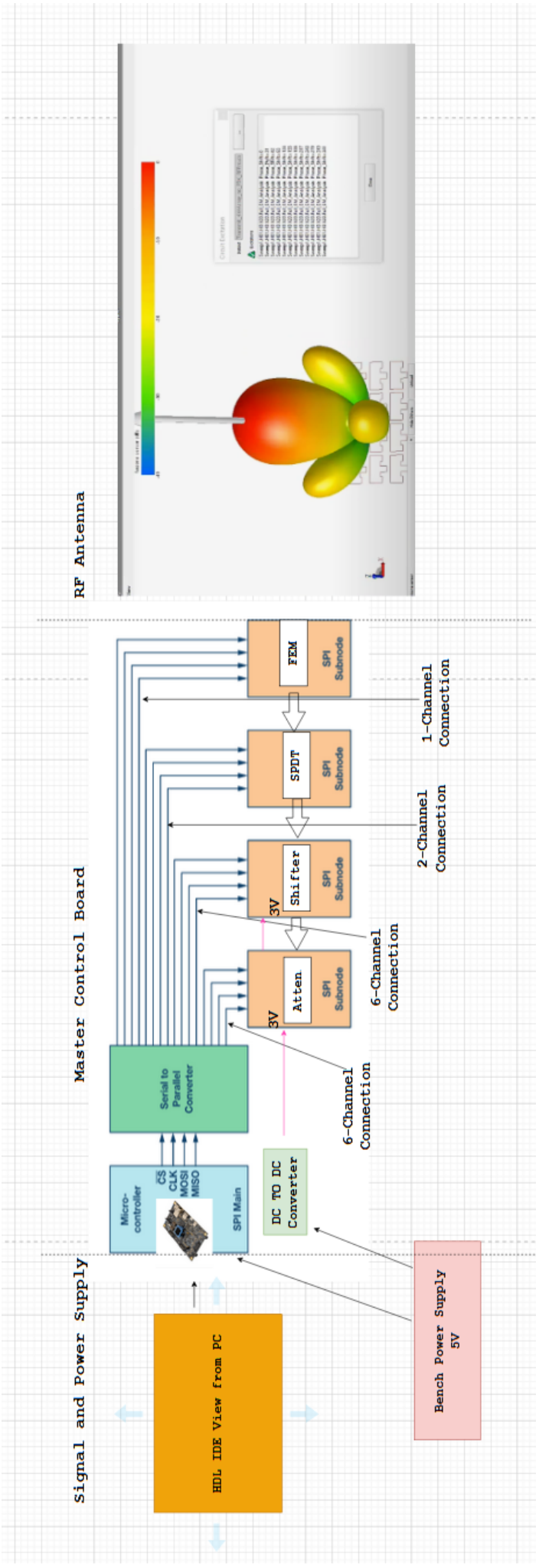


Figure 72: Final Overall Microcontroller based Interface Prototype [6]