Design and analysis of the building blocks of a Phase-Locked Loop(PLL) in TSMC 45nm process

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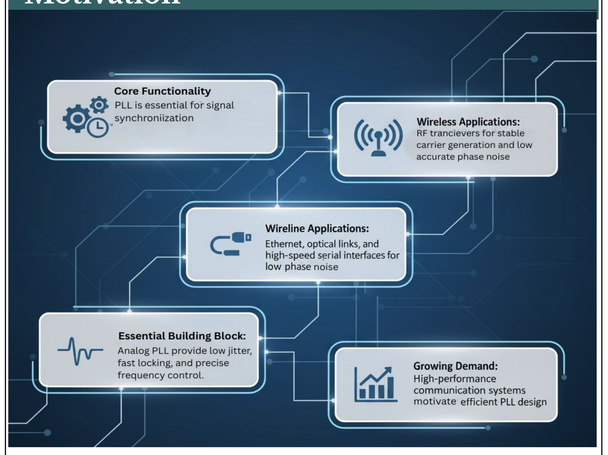
Abstract

An analog phase-locked loop (PLL) operating at 2.45 GHz is designed and implemented in a TSMC 45 nm CMOS process. The PLL consists of four key building blocks: a Gilbert-cell phase detector, a second-order passive RLC low-pass filter, an LC-tank voltage-controlled oscillator (VCO), and a balanced pi-attenuator for output signal conditioning.
The measured phase noise is −97.21 dBc/Hz at a 1 MHz offset, and the average output DC power consumption is 8.5 mW. The PLL achieves a fast lock time of 220 ns and demonstrates one of the lowest reported phase-noise performances among PLLs operating in a similar frequency range.

Motivation



Specifications

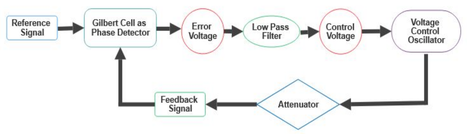
Lock Range (GHz)	Capture Range (GHz)	Power Consumption (mW)	Center Frequency (GHz)	Technology (nm)
2.42 - 2.47	2.43 - 2.46	8.5	2.45	45

Key References

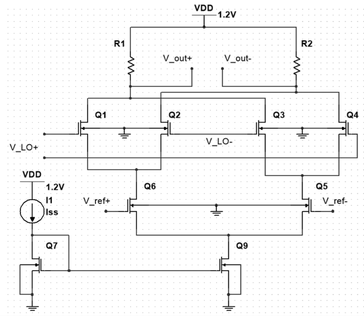
[1] Fatma M. Mahmoud, “Low Flicker-Noise RF CMOS Gilbert-Cell Mixer for 2.4GHz Wireless Communication Systems”, ICEEOT, 2016
[2] H.Ghayvat, “A 2.4GHz CMOS Gilbert Mixer in 180nm Technology”, 2015 Fifth International Conference on Communication Systems and Network Technologies
[3] Rafael Magerramov, “Research Parameters of a PLL System Based on Active and Passive Low-Pass Filter in 0.25-um CMOS Technology”, IEEE Conference of Russian Young Researchers in Electrical and Electronic Engineering (ElConRus), 2021
[4] Shrabanti Das, “Performance Comparison of 2.5-GHz LC Voltage-Controlled Oscillator for Three Different Technology Nodes”, 2019 Devices for Integrated Circuit (DevIC), 23-24 March, 2019, Kalyani, India
[5] Alexander Schure, “Filters and Attenuators”, John F. Rider Publisher, INC., New York
[6] B. Razavi, “CMOS Phase Locked Loop”, RF Microelectronics, Wiley, 2011

Methodology

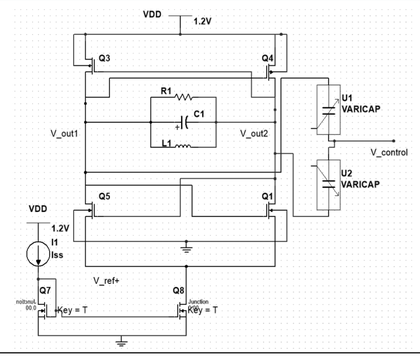
Proposed Design of PLL



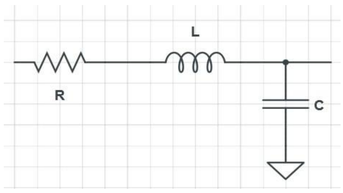
Gilbert Cell



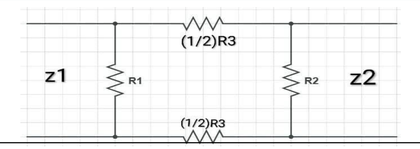
LC VCO



Low Pass Filter

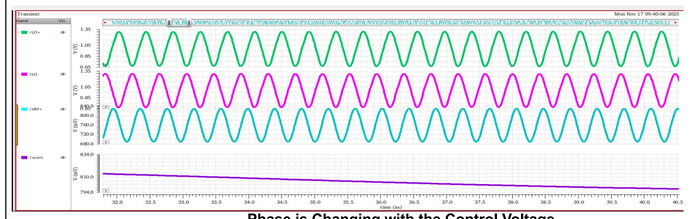


Attenuator

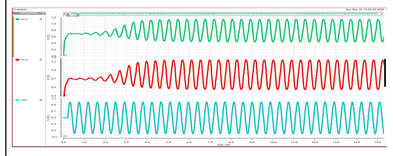


Simulation Results

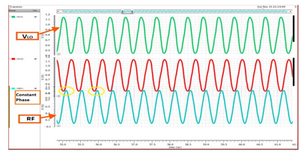
Phase Locked Loop



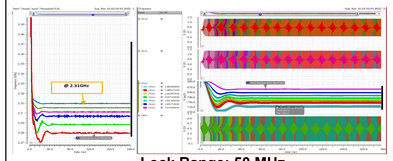
Phase is Changing with the Control Voltage



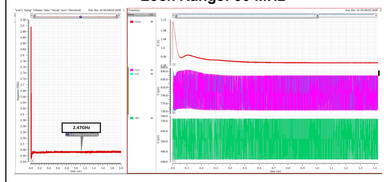
Phase Before Settling



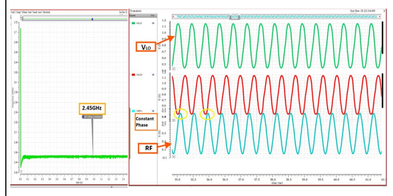
Phase After Settling



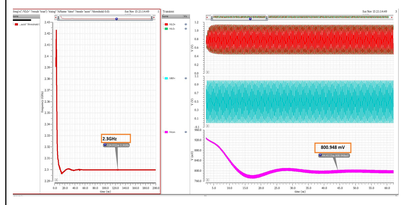
Lock Range: 50 MHz



PLL Locked to 2.47 GHz Reference Signal & Generated Output = 2.47 GHz Signal

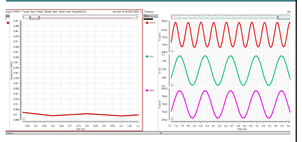


PLL Locked to 2.45 GHz Reference Signal & Generated Output = 2.45 GHz Signal



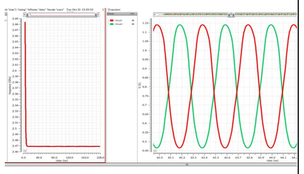
PLL Locked to 2.3 GHz Reference Signal & Generated Output = 2.3 GHz Signal

Gilbert Cell



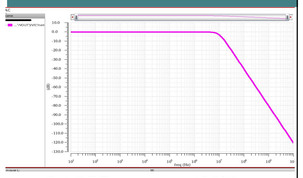
Input: f_{LO} = 2.45 GHz , f_{RF} = 2.45 GHz
Output: fout= 4.9 Ghz

LC VCO



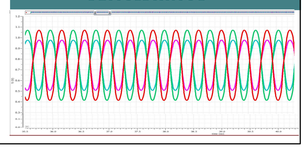
The Output of VCO at Vcont = 940 mv
Output Frequency = 2.47 GHz

Low Pass Filter



Cut Off Frequency = 10 MHz

Attenuator



Comparison

Reference	CMOS Technology (nm)	Frequency (GHz)	Lock Range (GHz)	Capture Range (GHz)	PN @1MHz (dBc/Hz) As Oscillator	Power Consumption (mW)	Supply Voltage (V)	Locking Time
This Work	45	2.45	2.47 - 2.42	2.46 - 2.43	- 97.21	8.5	1.2V	220 nS
[10]	90	1	-	-	-86.21	11.9	1.8V	280.6 ns
[11]	180	10.08			-113.47	39	1.8V	< 3 us
[12]	130 nm BiCMOS	92.7 - 100.2			-102	570	3.5V	
[13]	Bang-bang DPLL - 65 nm	3.7-4.1	52MHz		-163.3	5.28		5.6 us

Metric	Improvement
Power Consumption	⭐ Yes
Locking Time	⭐ Major improvement
Phase Noise	✔ Reasonable

Future Direction

- Lower phase noise / improve spectral purity
- Reduce power further
- Widen tuning/lock/capture range and add fractional control
- Implementation at the layout level

Conclusion

We present a 45-nm PLL operating at 2.45 GHz that achieves 8.5 mW power consumption, 220 ns lock time, and −97.21 dBc/Hz phase noise at a 1 MHz offset, with measured lock and capture ranges of 50 MHz and 30 MHz, respectively, at a 1.2 V supply, demonstrating an excellent balance of power efficiency, speed, and spectral performance compared to prior work.

Acknowledgements

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