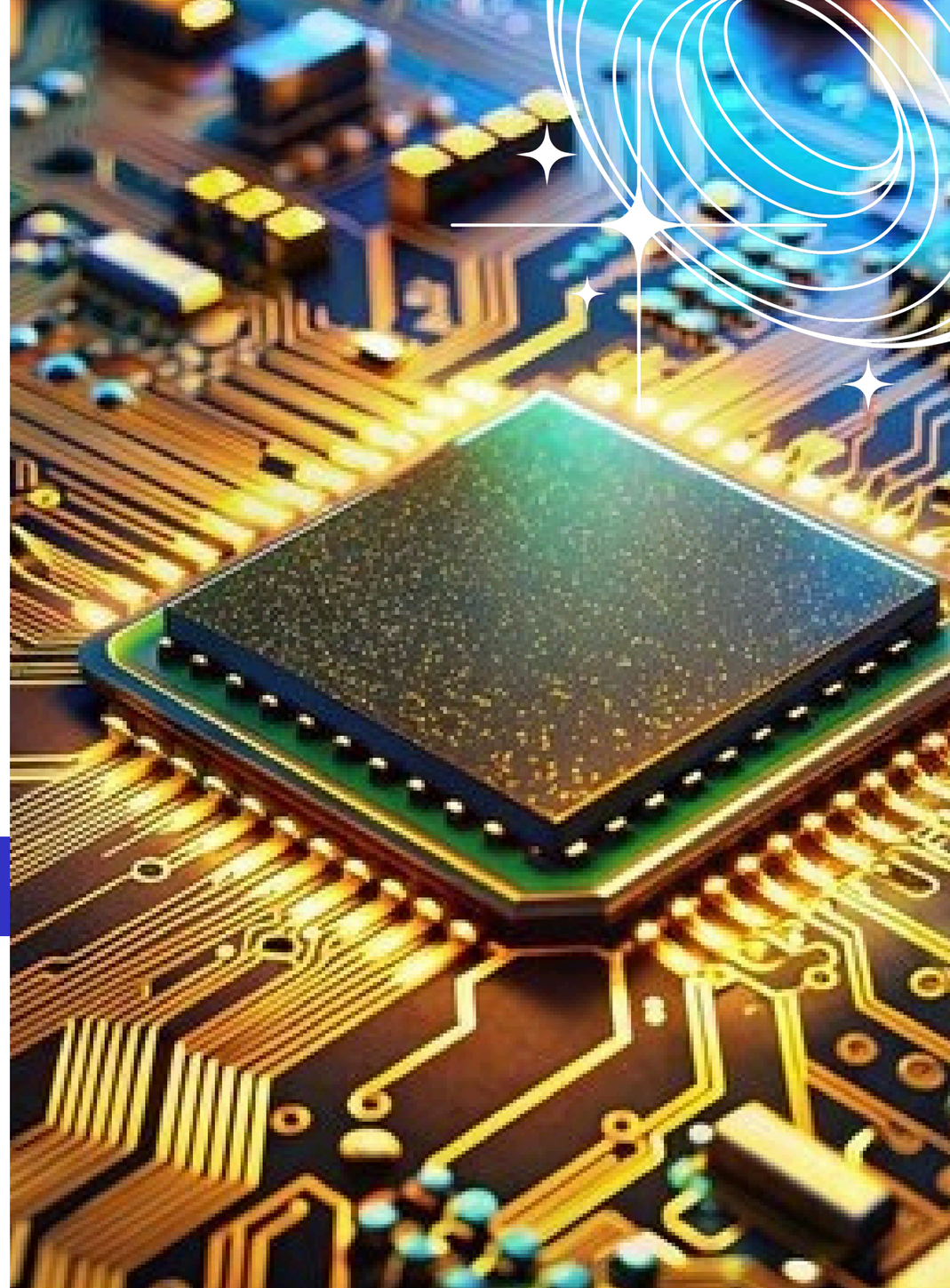
CATR
Centre for Advanced Training and Research
Govt. Registered & ISO-IAF Certified

# Job-Oriented VLSI Design Training with Live Project

## Master VLSI in 10 Days – Skills That Industry Demands

**25 June-05 July 2026 | 7:00 PM Daily | Online-Google Meet**

🇮🇳India – 7:00 PM | 🇸🇦 Saudi Arabia – 4:30 PM |🇦🇪Dubai – 5:30 PM |
🇲🇾Malaysia – 9:30 PM | 🇬🇧 London – 2:30 PM |🇺🇸New York – 9:30 AM

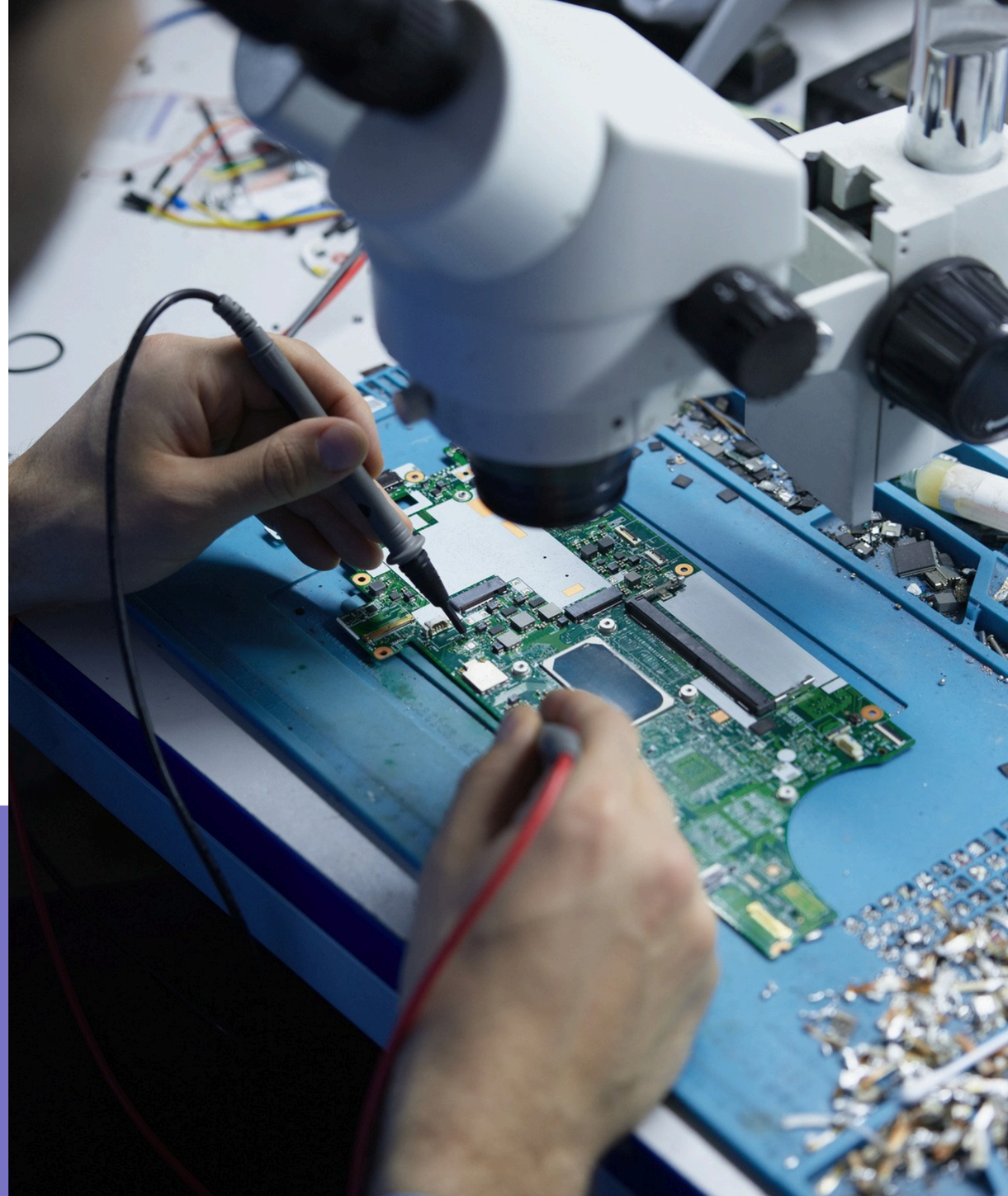


# Training Overview

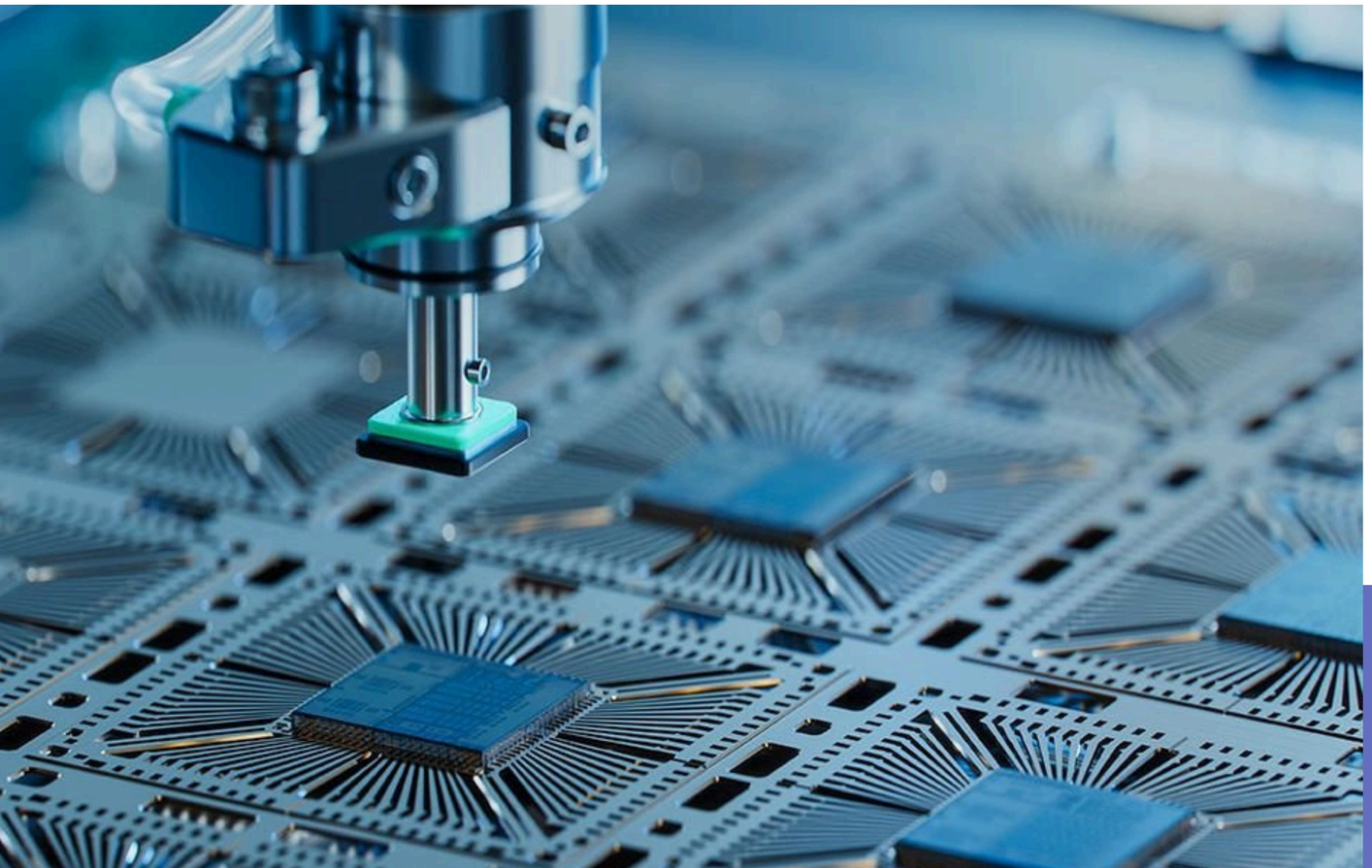
Thisintensive 10-day onlineVLSIDesign trainingcourse is designedto provide a completeunderstanding of the semiconductor chip design flow—from RTL coding to physical design and verification. The course combines theoretical concepts with hands-on exposure to industry tools such as Cadence, Synopsys, and Mentor Graphics. Learners will gain practical skills in Verilog HDL, synthesis, timing analysis, and backend design, making them job-ready at a beginner level. Whether you aim to enter the semiconductor industry or strengthen your electronics design skills, this course provides a strong foundation aligned with real industry workflows.

**VLSI powers modern electronics and enables applications in:**

- 📱 Smartphones & consumer devices
- 💻 Microprocessors & computer systems
- 🚗 Automotive & EV electronics
- 📡 5G & IoT communication
- 🏥 Medical & embedded systems
- 🤖 AI chip design & hardware accelerators



# Industry & Job Relevance of this training



The semiconductor industry is one of the fastest-growing sectors globally, with increasing demand for skilled VLSI engineers. After completing this course, learners can explore roles such as:

- VLSI Design Engineer
- Verification Engineer
- Physical Design Engineer
- RTL Design Engineer
- Timing/STA Engineer

**Top hiring companies:**

Intel, Qualcomm, NVIDIA, AMD, TSMC, Samsung, Texas Instruments, etc

# Training Module

**Day1:Introductionto VLSI & IndustryFlow**
· Overview of VLSIdesign and applications
· Moore's Law, scaling trends
· Full chip design flow (Spec → RTL → GDSII → Fabrication)
· Frontend vs Backend
· Introduction to tools (Cadence, Synopsys, Mentor Graphics)

**Day 2: CMOS Technology Basics**
· MOSFET operation (NMOS, PMOS)
· CMOS inverter and logic gates
· Switching characteristics & Power dissipation (dynamic, static)
· Process technology nodes (7nm, 14nm, etc.)

**Day 3: Digital Design Fundamentals**
· Combinational circuits
· Sequential circuits (flip-flops, latches)
· Timing concepts (setup, hold, propagation delay)
· Clocking strategies

**Day 4: Verilog HDL (RTL Design)**
· Verilog syntax and constructs
· Behavioral vs structural modeling
· Writing RTL for combinational & sequential circuits
· Testbench basics & Simulation using tools (ModelSim / VCS)

**Day 5: Advanced RTL & Design Practices**
· FSM design (Moore & Mealy) & Coding guidelines for synthesis
· Blocking vs non-blocking assignments
· Parameterization and reusable RTL

**Day 6: Synthesis (RTL to Gate-Level)**
· Introduction to synthesis flow
· Constraints (SDC – timing constraints)
· Area vs speed trade-offs & Netlist generation
· Tools: Synopsys Design Compiler / Cadence Genus

**Day 7: Static Timing Analysis (STA)**
· Timing paths (setup & hold analysis)
· Clock skew and uncertainty
· Timing violations and fixes
· Tools: PrimeTime basics

**Day 8: Physical Design (Backend Flow)**
· Floorplanning &Placement
· Clock Tree Synthesis (CTS)
· Routing
· Introduction to tools (Cadence Innovus)

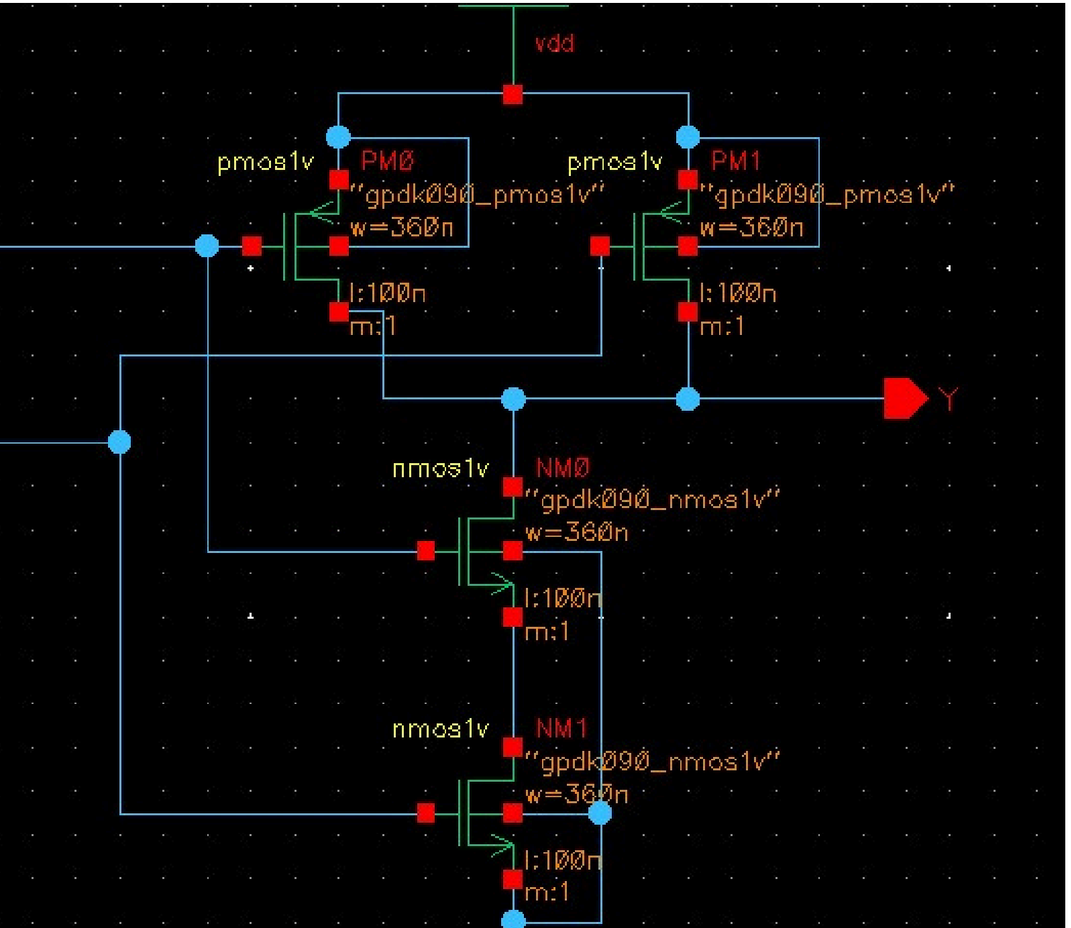
**Day 9: Physical Verification & Signoff**
· DRC (Design Rule Check)
· LVS (Layout vs Schematic)
· Power integrity (IR drop, EM)
· Signal integrity basics & Tape-out process

**Day 10: Industry Project & Career Exploration**
· Mini project: RTL → Synthesis → Basic PD flow
· Debugging real design issues
· Career paths (Design Engineer, Verification Engineer, Physical Design Engineer)

# Key Benefits of the Training Course

- Learn complete VLSI design flow (Frontend + Backend)
- Hands-on experience with Verilog RTL coding & simulation
- Exposure to industry-standard EDA tools
- Understand timing analysis & synthesis concepts
- Work on a mini industry-based project
- Get career guidance for VLSI roles
- Learn industry-relevant design methodologies
- Improve problem-solving and debugging skills
- Understand real chip design challenges & workflows
- Build a strong foundation for VLSI interviews
- Enhance your resume with project experience
- Network with peers and mentors
- Step-by-step guidance from beginner to industry level
- Boost confidence to apply for internships & jobs in VLSI

# Who can Join?

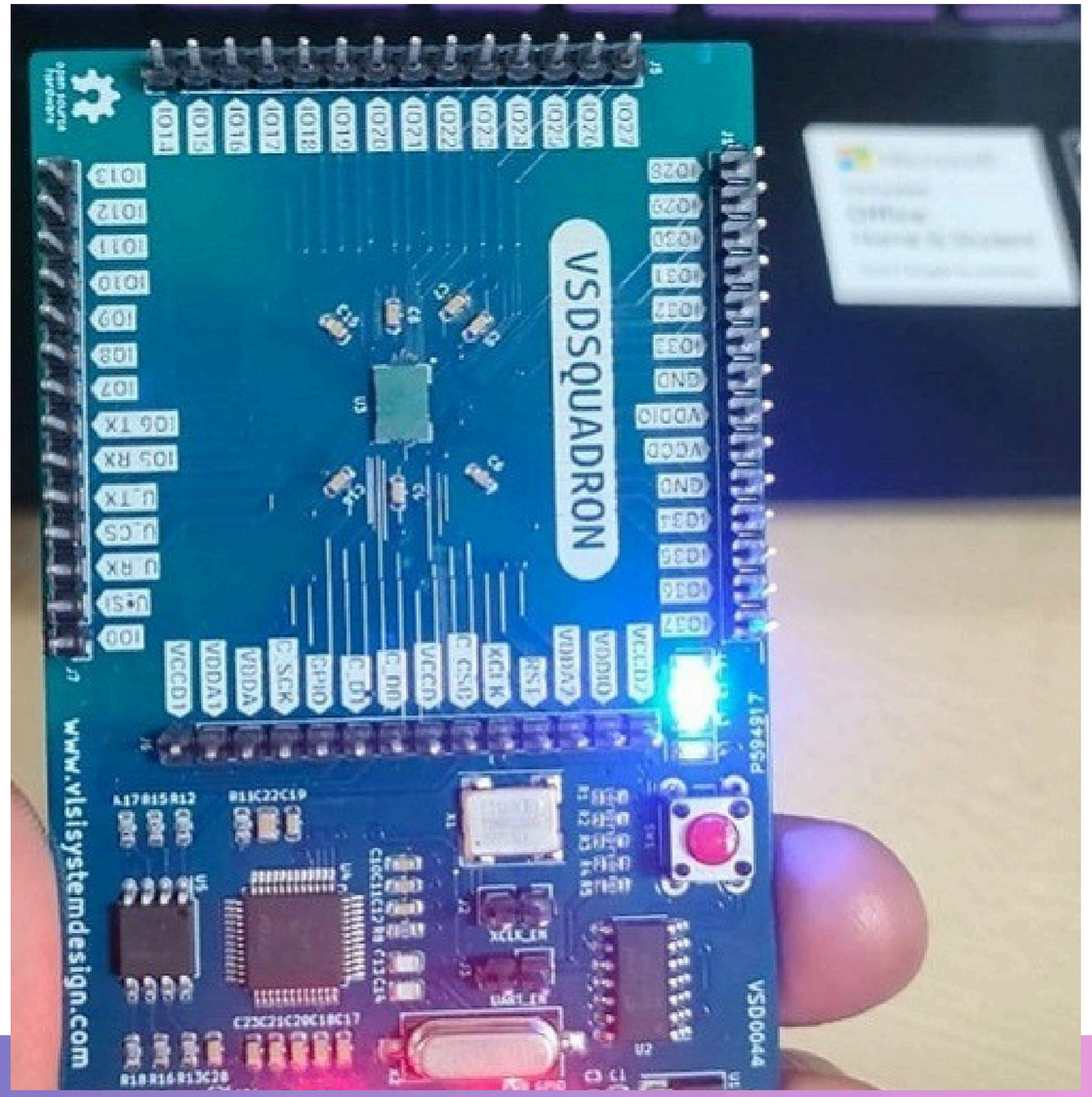



**This course is ideal for**

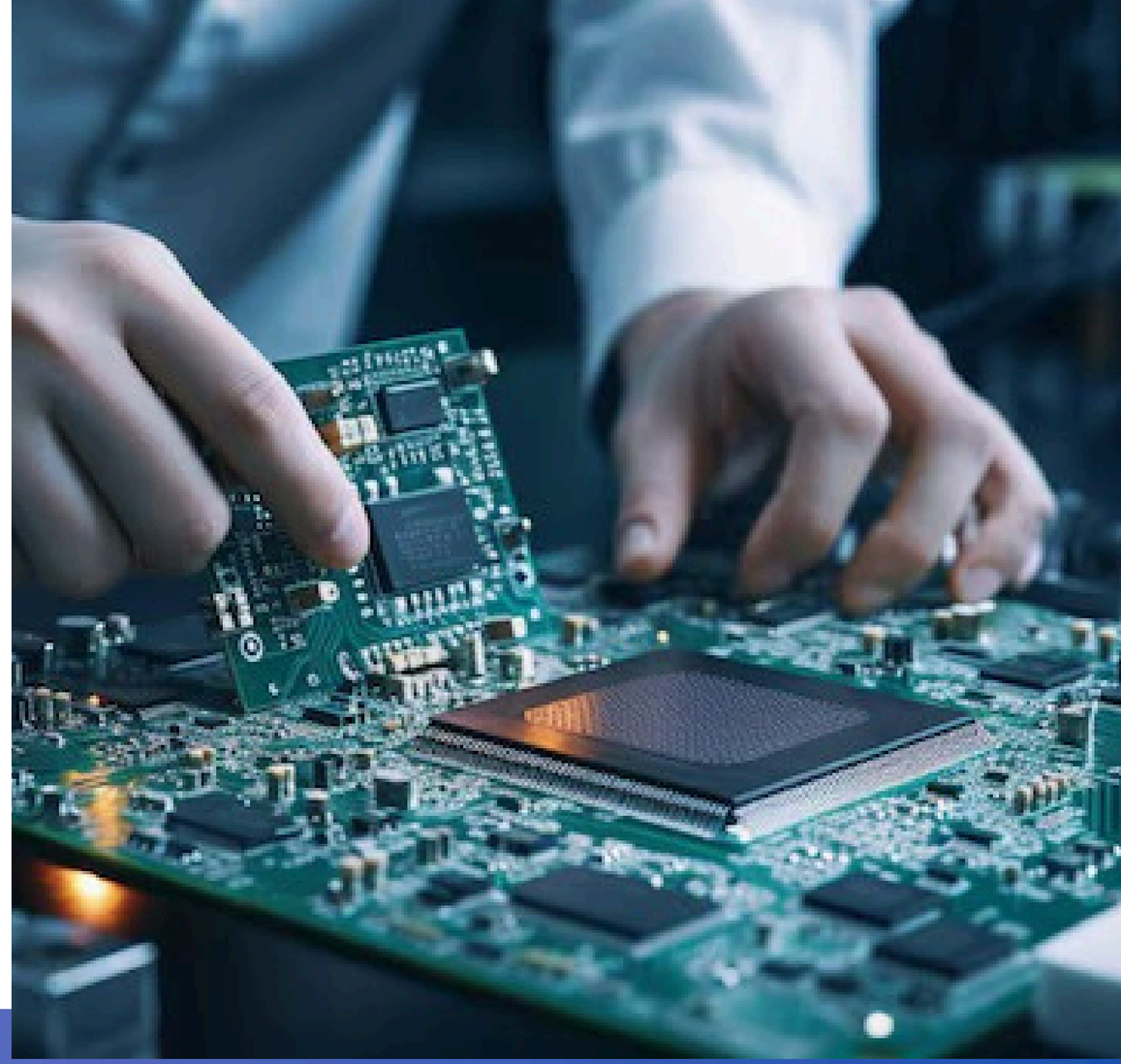
- B.Tech / B.E students (Electronics, Electrical, ECE, EE, EEE)
- Diploma students in electronics-related fields
- M.Tech students in VLSI / Embedded Systems
- Beginners interested in semiconductor industry
- Professionals looking to switch into VLSI domain

# Training Features & Fee

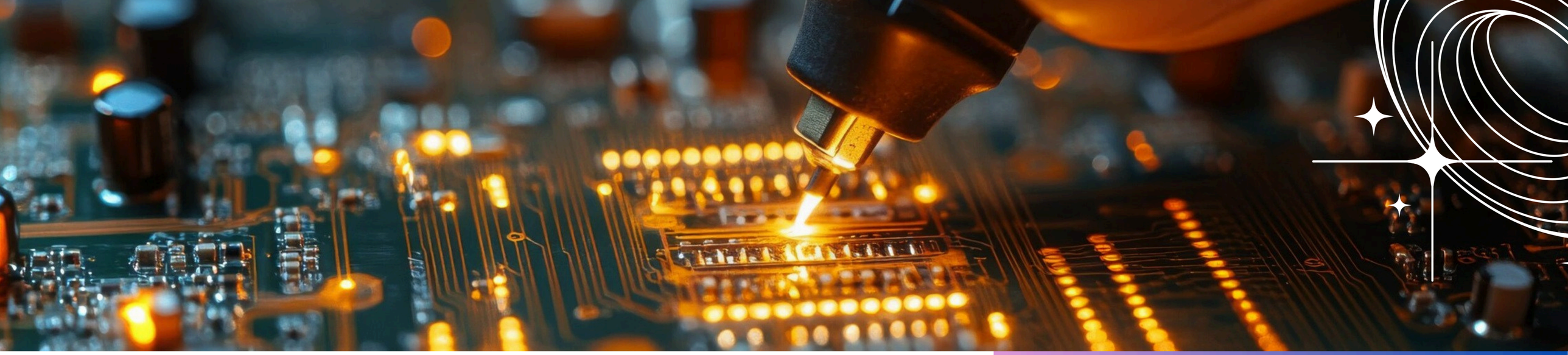
- **Certificate of completion**
- **Live interactive sessions**
- Recorded lectures access
- Lecture PPTs & study material
- Hands-on project experience
- Career guidance session




- 🇮🇳**Indian Students : ₹2499**
- 🌍**International Participants: $ 100**

# Design the Future of Chips-Learn VLSI from Experts



# Centre For Advanced Training and Research

(Govt. Registered and ISO-IAF certified)

## Bringing Excellence to the Students

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