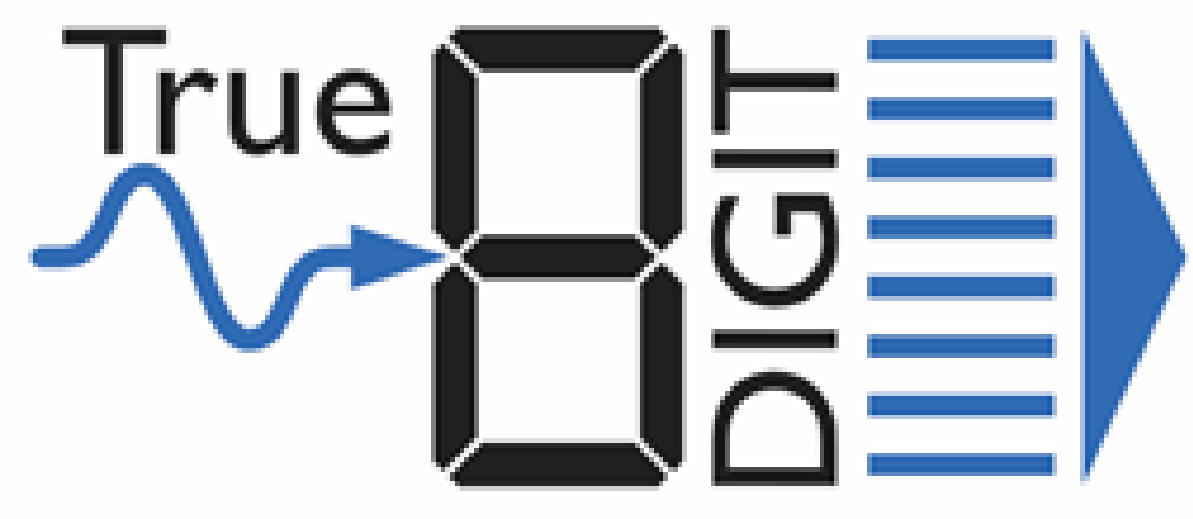
Ultra-low jitter timing platform for high-precision composite ADCs



Ricardo Iuzzolino (INTI)

M36 meeting Workshop, 14th-15th May 2026

Why a low jitter timing platform ?

Project requirement: tj < 50 ps

Clock jitter affects full scale sine wave input ADC performance directly by degrading the total signal-to-noise ratio:

$$SNR_{\text{Total}} = 10\log_{10}\left(10^{\frac{-SNR_{\text{ADC}}}{10}} + 10^{\frac{-SNR_{\text{jitter}}}{10}}\right) \qquad SNR_{\text{jitter}} = -20\log_{10}(2\pi f\sigma_{\text{j}})$$

$$ENOB = \frac{SNR_{Total}(dB) - 1.76\,dB}{6.02}$$

Timing Platform Concept

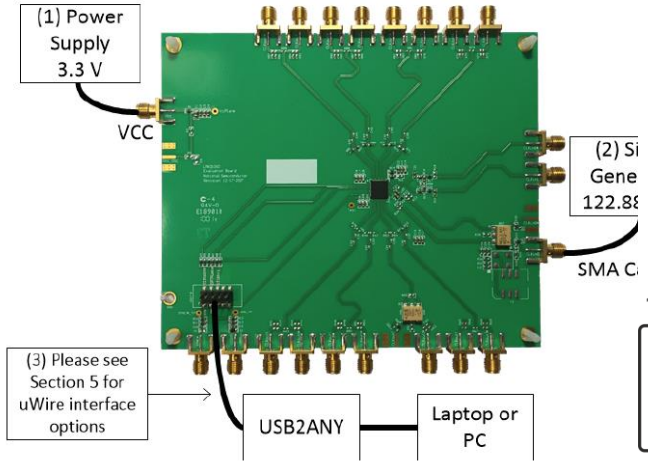


Figure 2. LMK01000 EVM Set Up

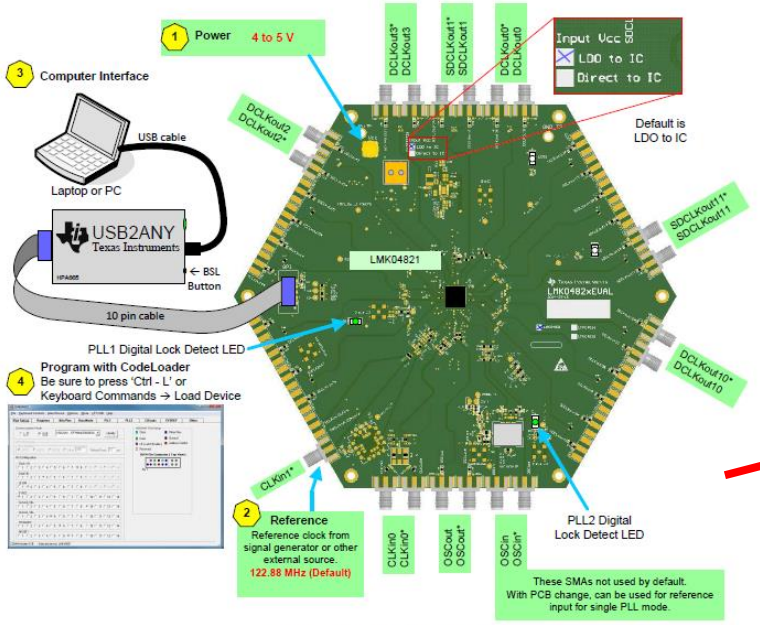
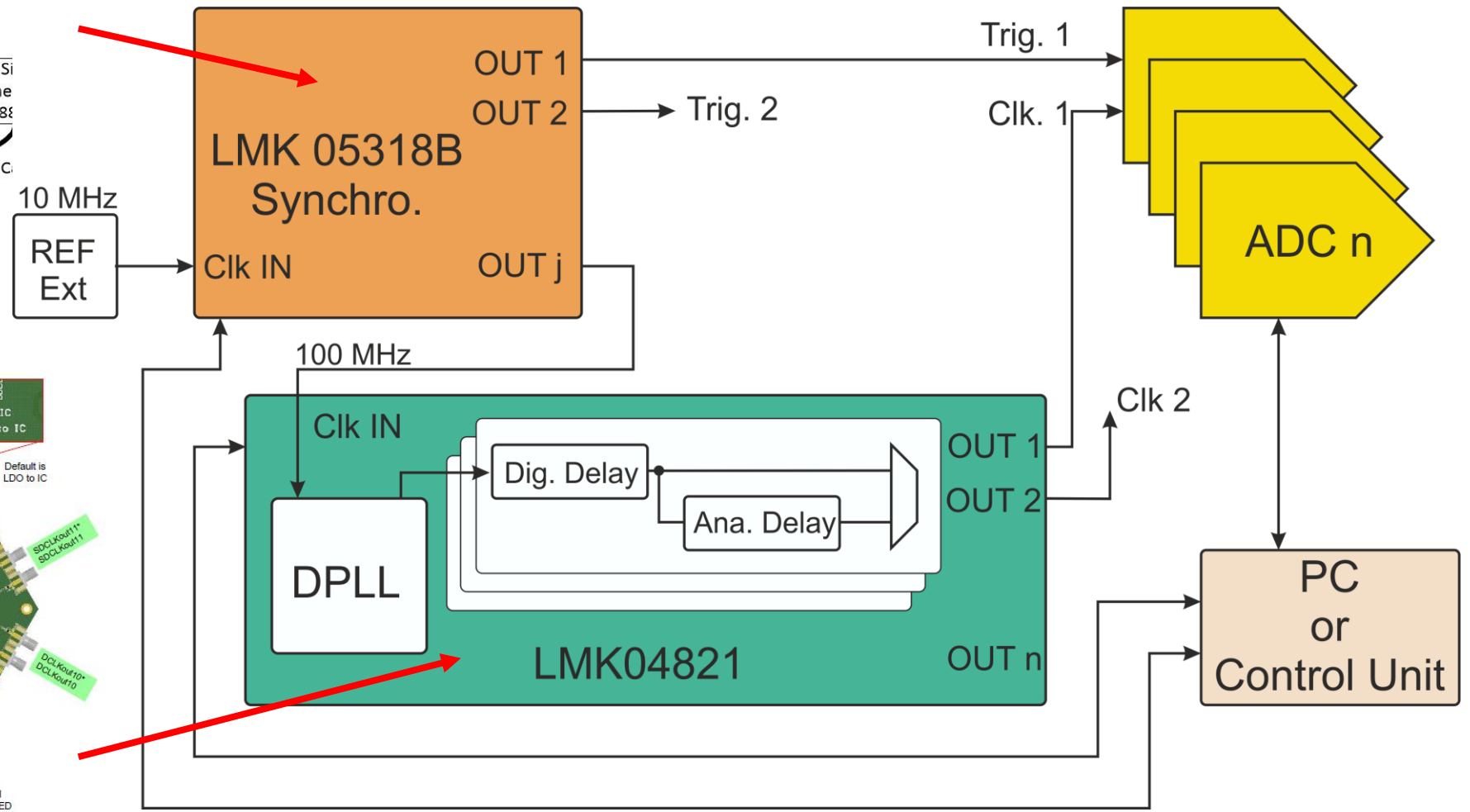
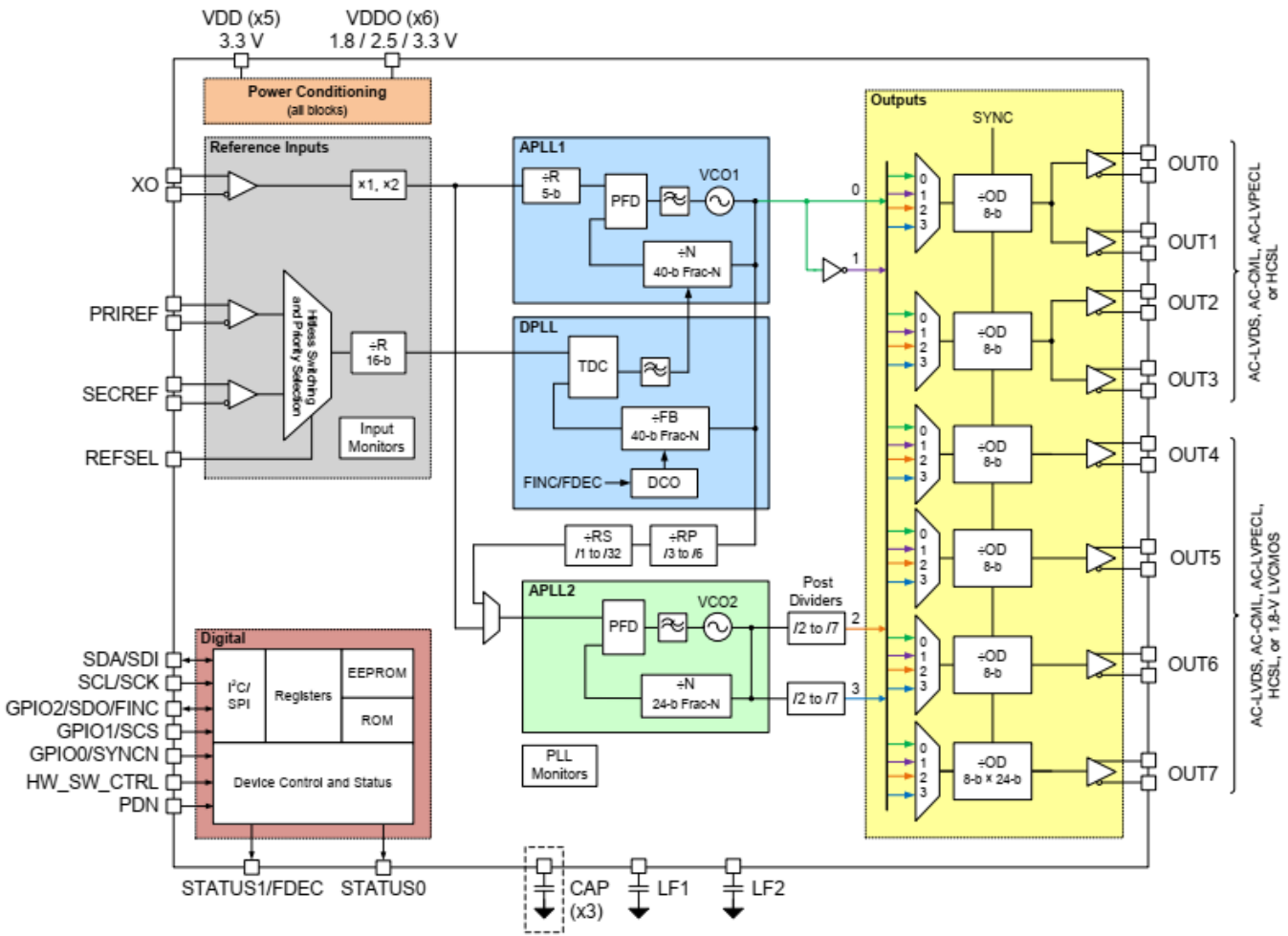


Figure 1. Quick Start Diagram



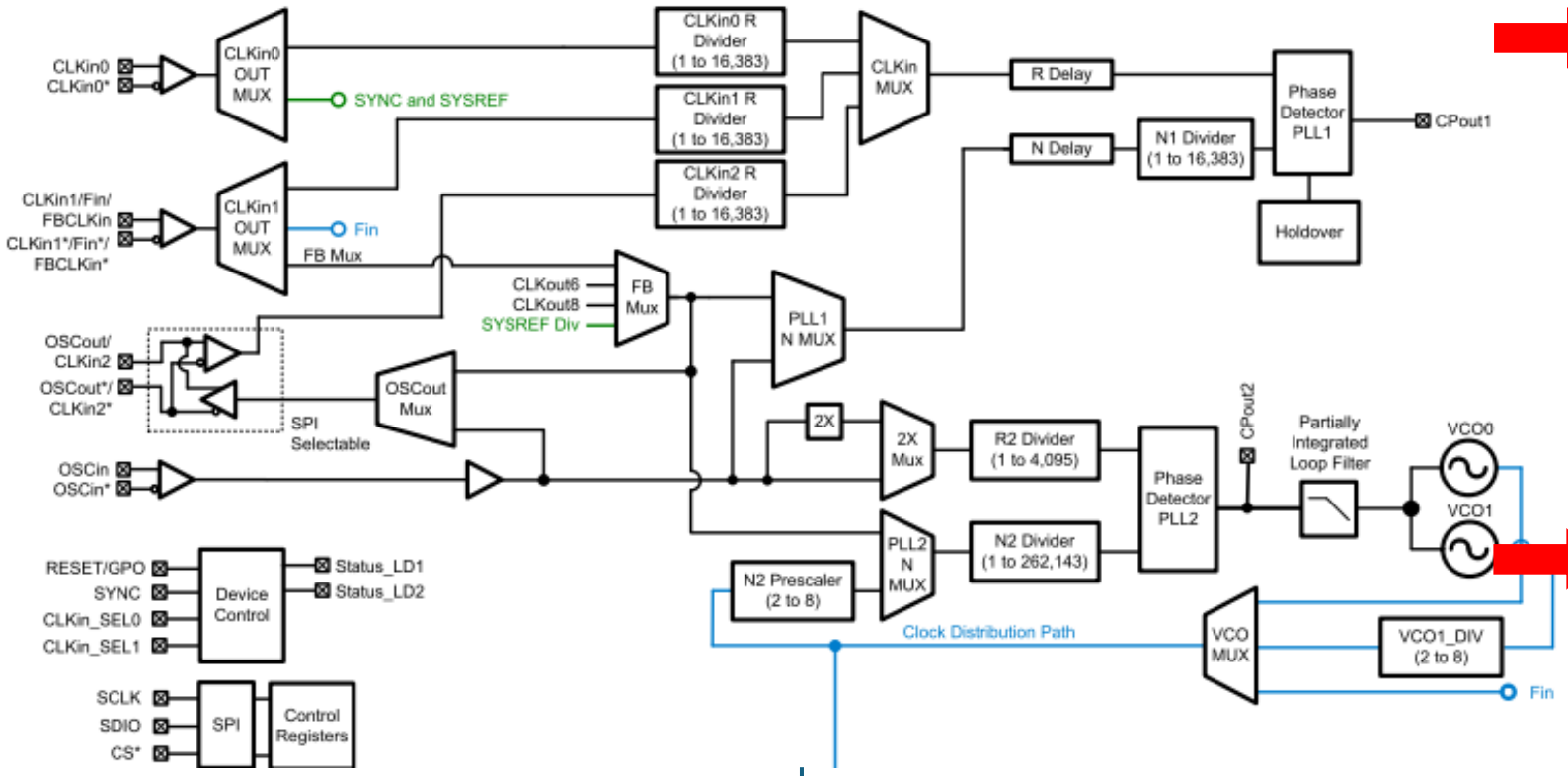
LMK05318B Functional Block diagram



1 Features

- One Digital Phase-Locked Loop (DPLL) With:
  - Hitless Switching: ±50-ps Phase Transient
  - Programmable Loop Bandwidth With Fastlock
  - Standards-Compliant Synchronization and Holdover Using a Low-Cost TCXO/OCXO
- Two Analog Phase-Locked Loops (APLLs) With Industry-Leading Jitter Performance:
  - 50-fs RMS Jitter at 312.5 MHz (APLL1)
  - 125-fs RMS Jitter at 155.52 MHz (APLL2)
- Two Reference Clock Inputs
  - Priority-Based Input Selection
  - Digital Holdover on Loss of Reference
- Eight Clock Outputs With Programmable Drivers
  - Up to Six Different Output Frequencies
  - AC-LVDS, AC-CML, AC-LVPECL, HCSL, and 1.8-V LVCMOS Output Formats
- EEPROM / ROM for Custom Clocks on Power-Up
- Flexible Configuration Options
  - 1 Hz (1 PPS) to 800 MHz on Input and Output
  - XO/TCXO/OCXO Input: 10 to 100 MHz
  - DCO Mode: < 0.001 ppb/Step for Precise Clock Steering (IEEE 1588 PTP Slave)
  - Advanced Clock Monitoring and Status
  - I^2C or SPI Interface

LMK04821 Functional Block diagram (I)

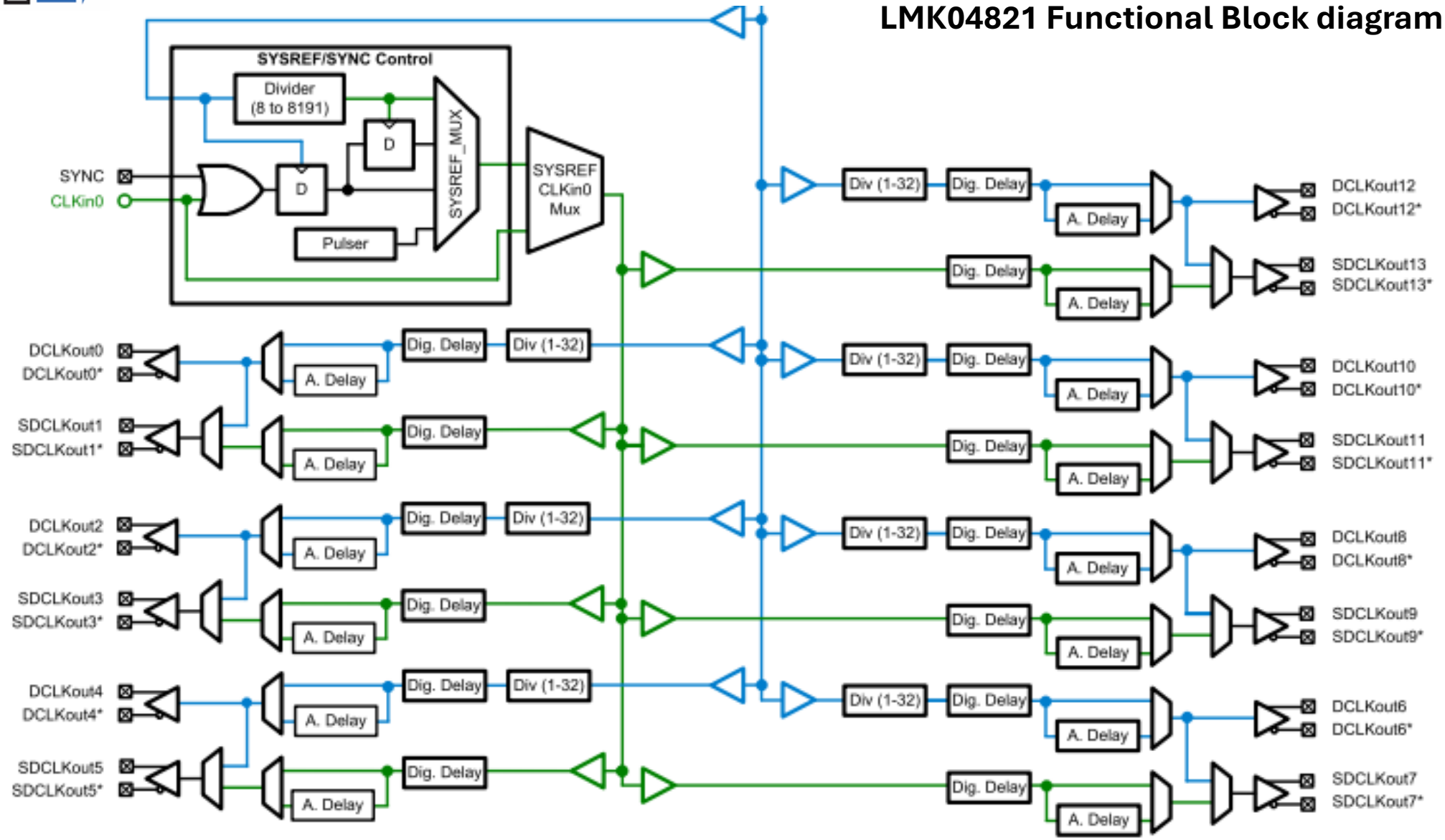


Continue in following slide

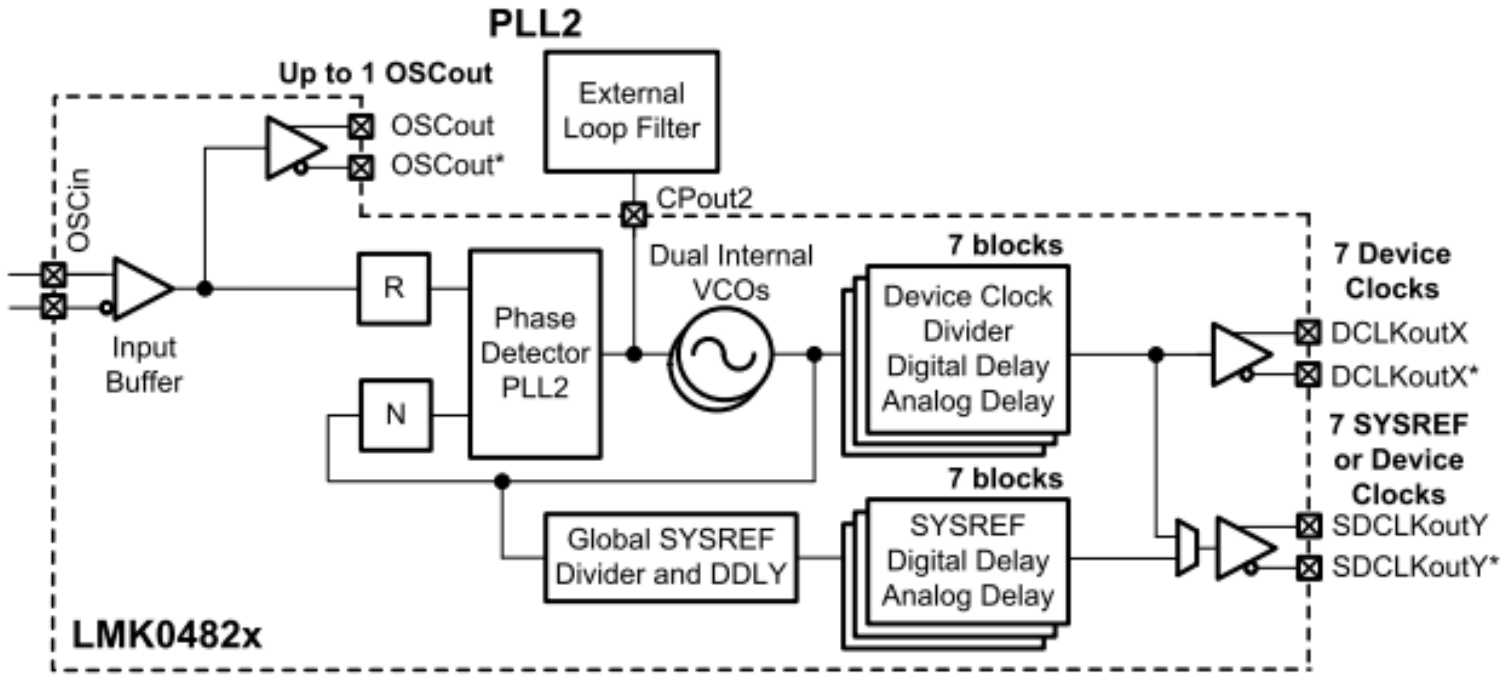
1 Features

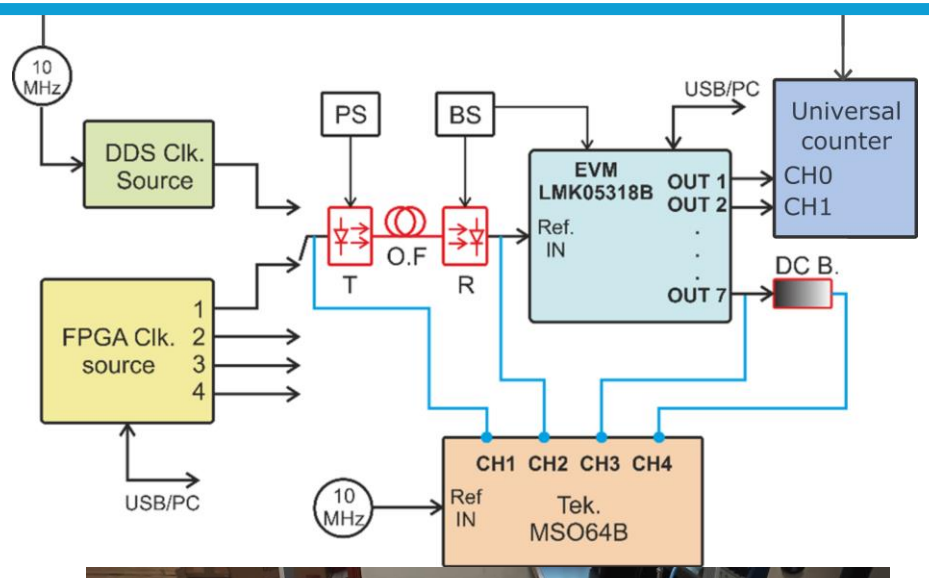
- JEDEC JESD204B Support
- Ultra-Low RMS Jitter
  - 88 fs RMS Jitter (12 kHz to 20 MHz)
  - 91 fs RMS Jitter (100 Hz to 20 MHz)
  - –162.5 dBc/Hz Noise Floor at 245.76 MHz
- Up to 14 Differential Device Clocks from PLL2
  - Up to 7 SYSREF Clocks
  - Maximum Clock Output Frequency 3.1 GHz
  - LVPECL, LVDS, HSDS, LCPECL Programmable Outputs from PLL2
- Up to 1 Buffered VCXO/Crystal Output from PLL1
  - LVPECL, LVDS, 2xLVCMOS Programmable
- Dual Loop PLLatinum™ PLL Architecture
- PLL1
  - Up to 3 Redundant Input Clocks
    - Automatic and Manual Switch-Over Modes
    - Hitless Switching and LOS
  - Integrated Low-Noise Crystal Oscillator Circuit
  - Holdover Mode When Input Clocks are Lost
- PLL2
  - Normalized [1 Hz] PLL Noise Floor of –227 dBc/Hz
  - Phase Detector Rate up to 155 MHz
  - OSCin Frequency-Doubler
  - Two Integrated Low-Noise VCOs
- 50% Duty Cycle Output Divides, 1 to 32 (even and odd)
- Precision Digital Delay, Dynamically Adjustable
- 25-ps Step Analog Delay
- Multi-Mode: Dual PLL, Single PLL, and Clock Distribution

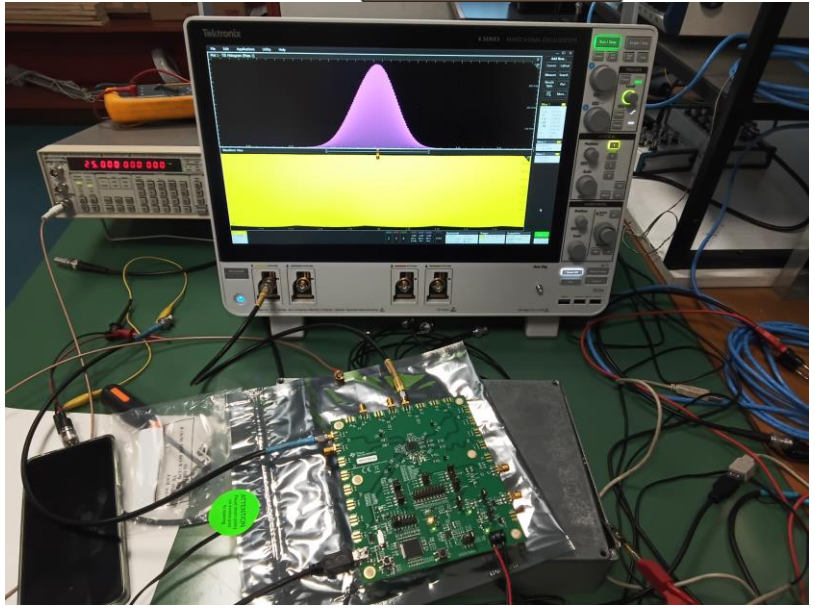
LMK04821 Functional Block diagram (II)

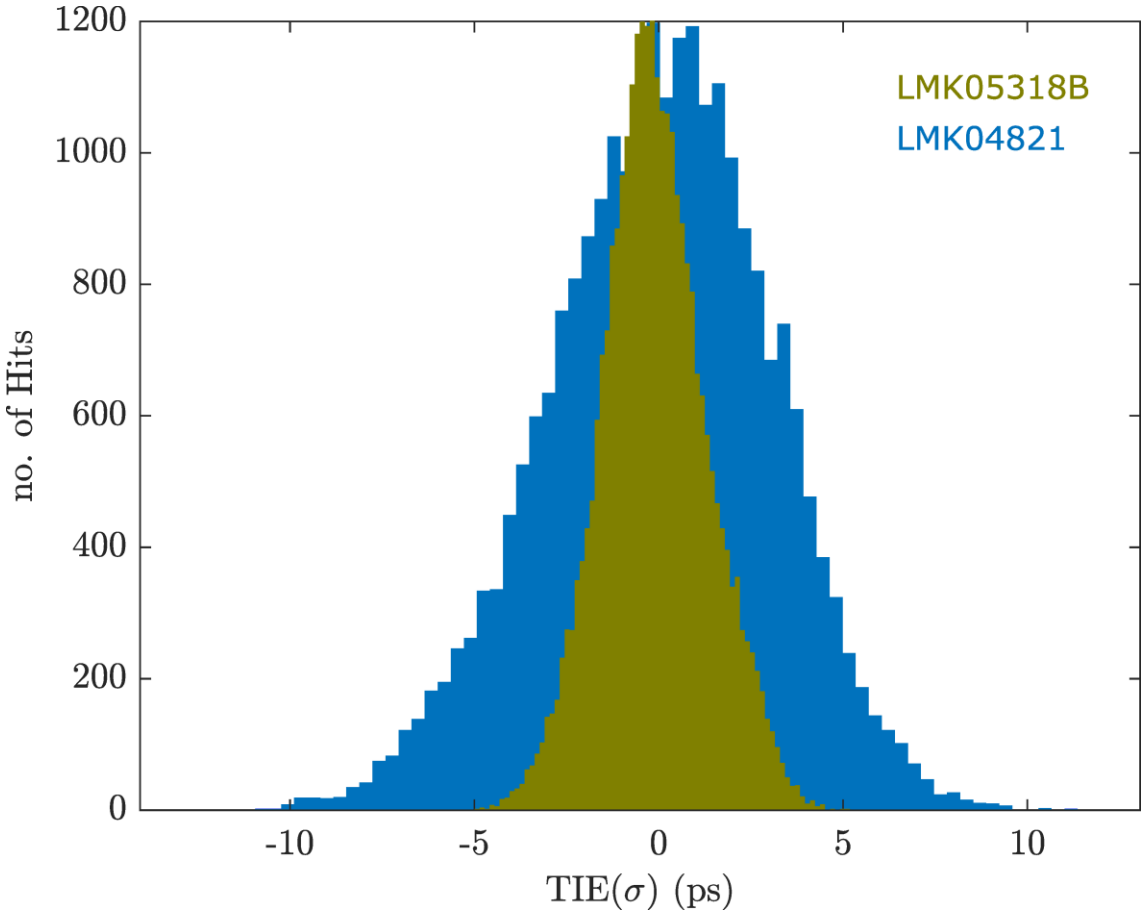


Single loop mode

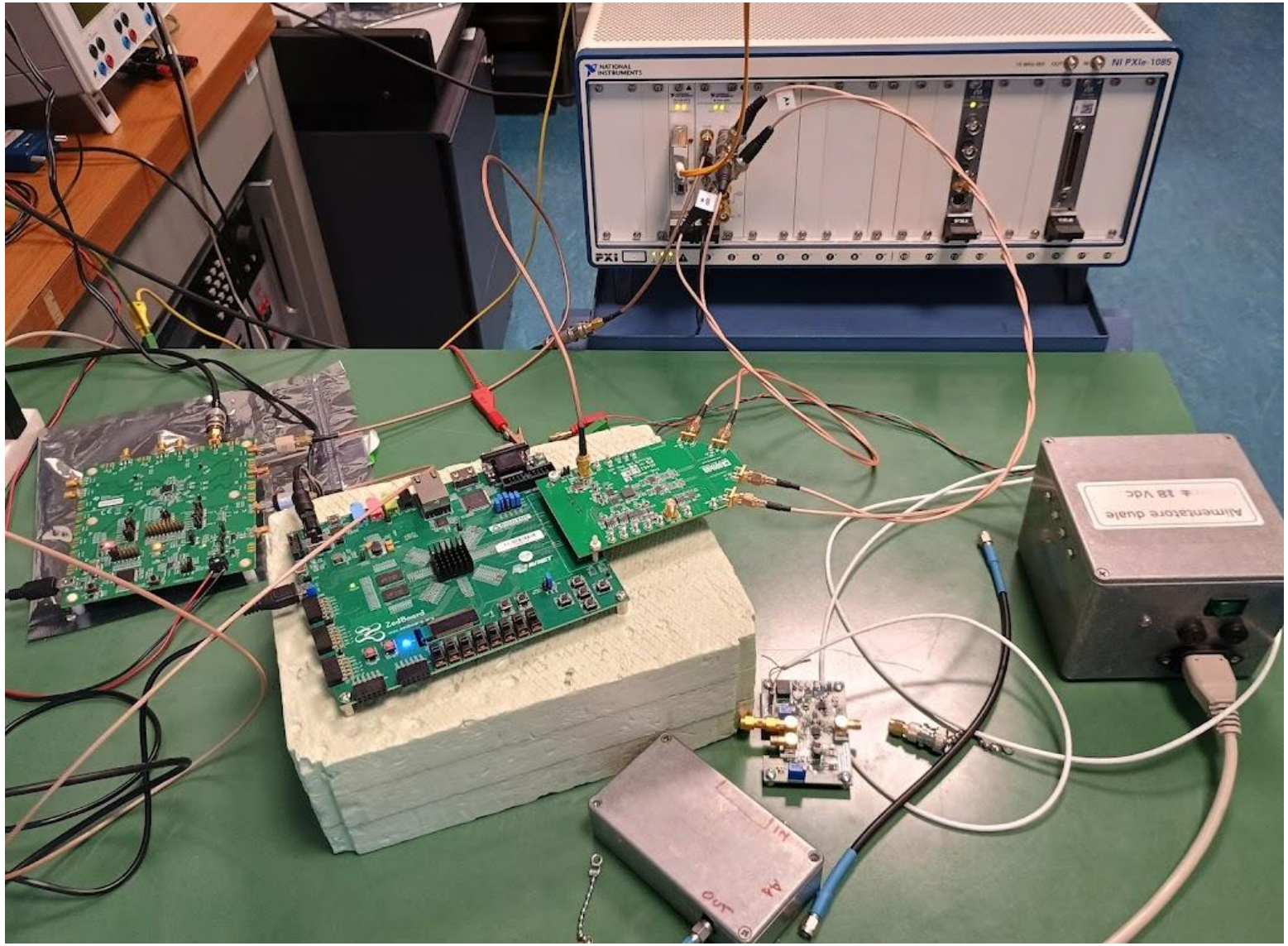



10 MHz
DDS Clk. Source
PS
BS
USB/PC
Universal counter
CH0
CH1
EVM LMK05318B
Ref. IN
OUT 1
OUT 2
OUT 7
O.F
T
R
DC B.
FPGA Clk. source
1
2
3
4
USB/PC
10 MHz
CH1 CH2 CH3 CH4
Ref IN
Tek. MSO64B

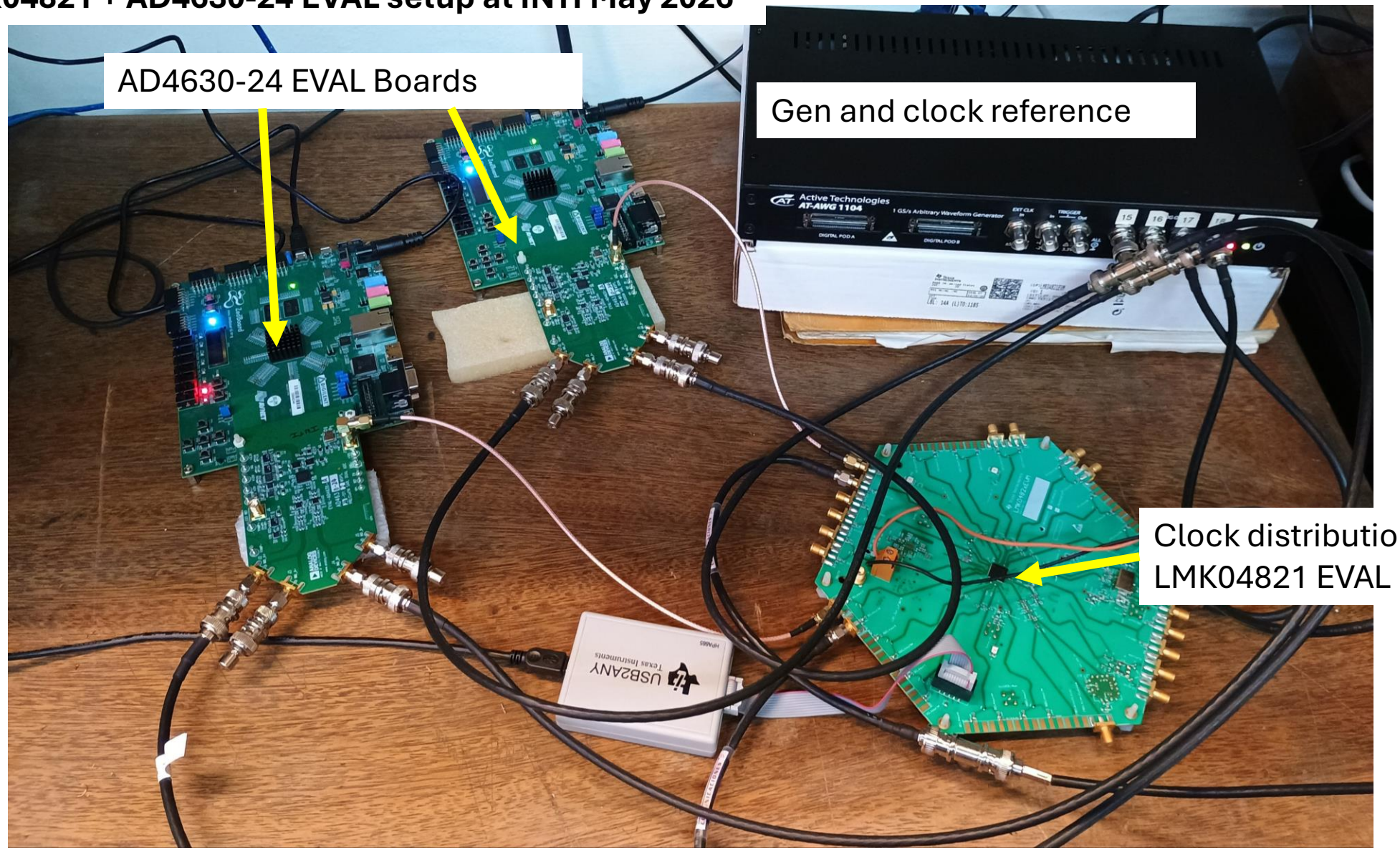



LMK05318B
LMK04821
no. of Hits
TIE(σ) (ps)
1200
1000
800
600
400
200
0
-10
-5
0
5
10

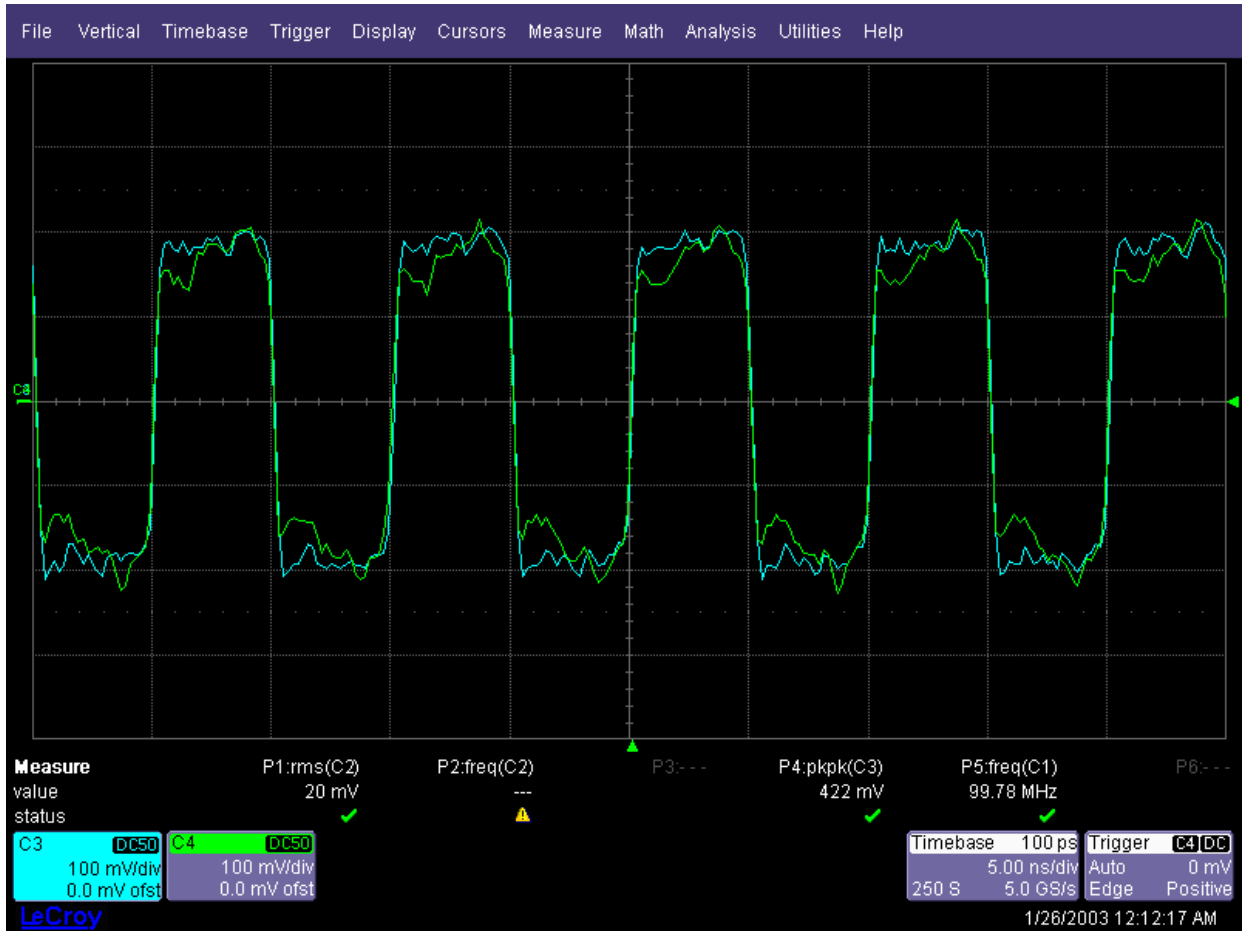
LMK05318B + AD4630-24 EVAL setup at INRiM (INTI-INRiM Dec. 2025)

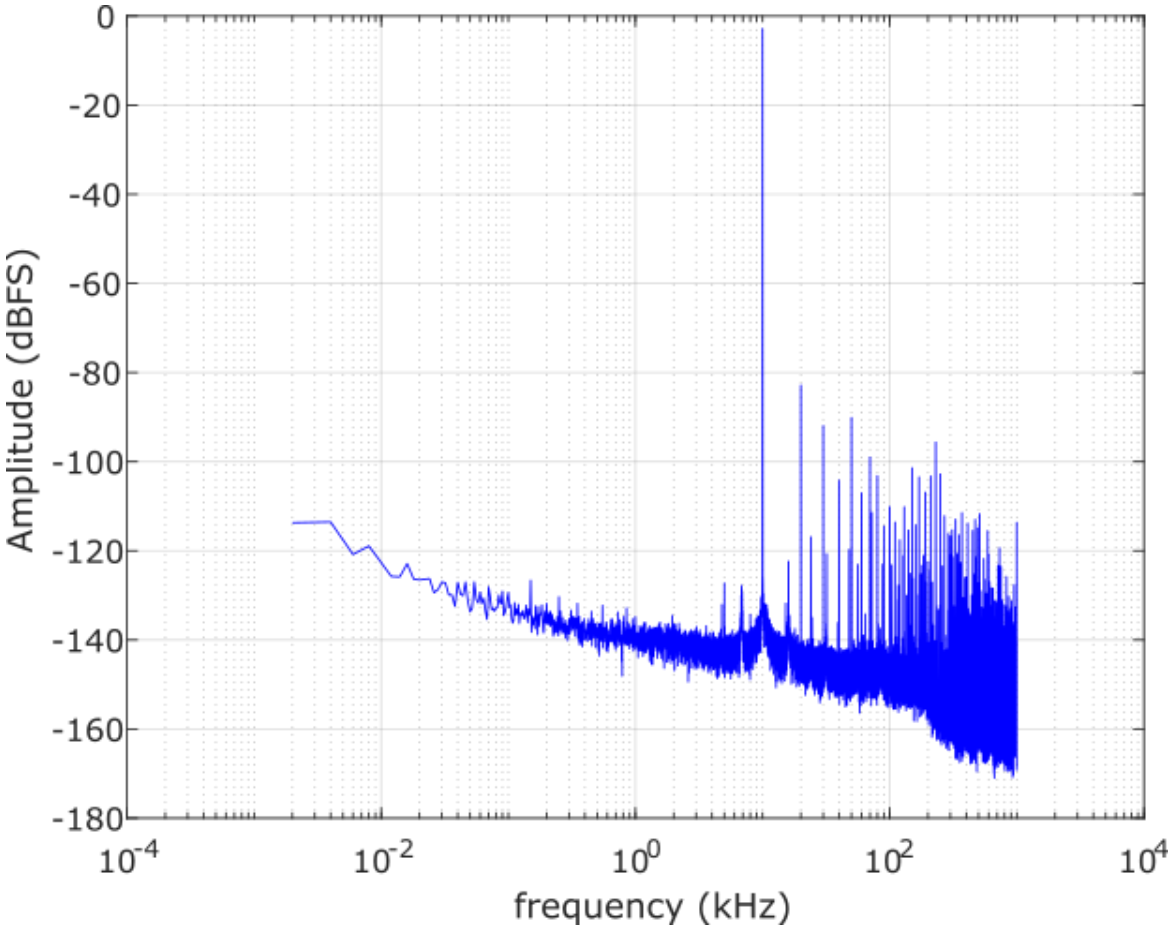


LMK04821 + AD4630-24 EVAL setup at INTI May 2026



2 ADCs - Averaged



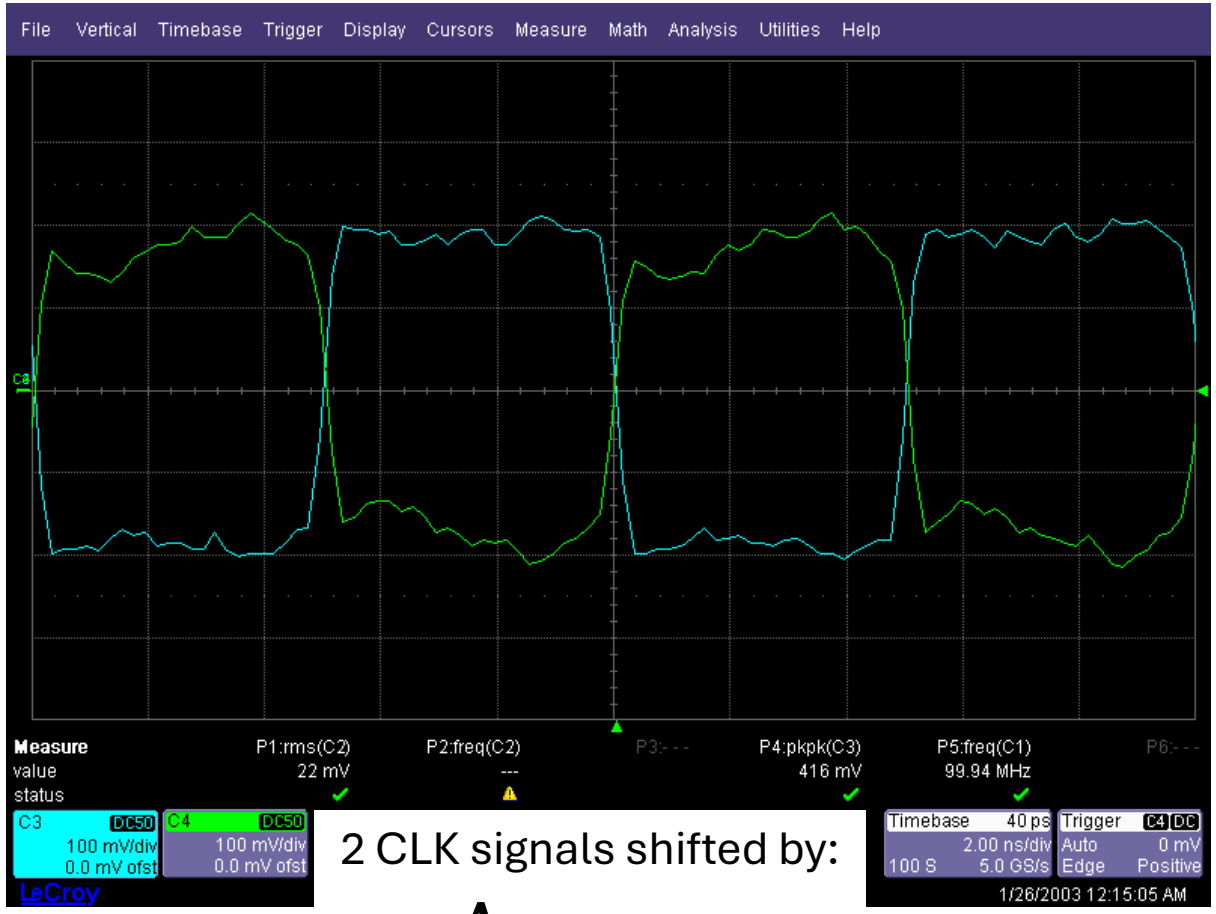


Δt a few ps

ADCs – Interleaved (I)

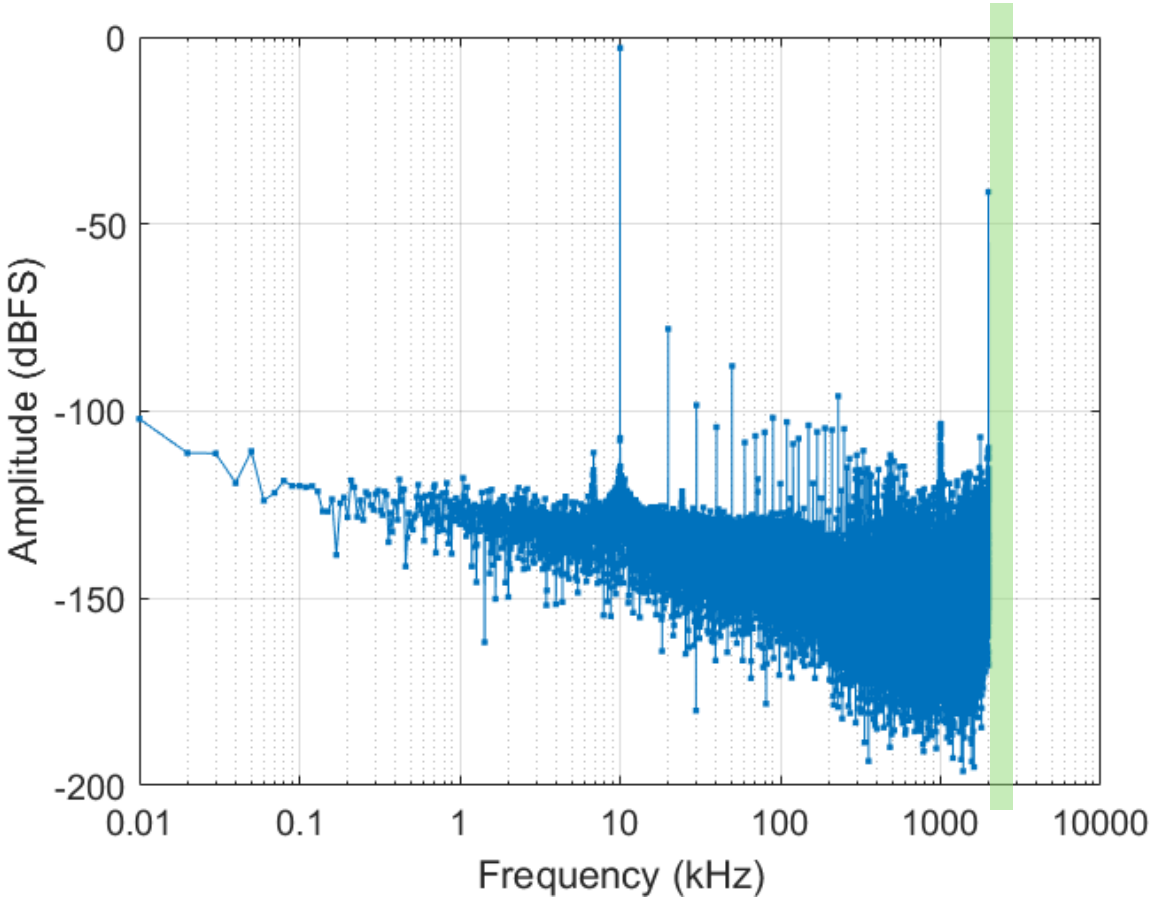
2 ADCs - Interleaved

The sampling rate is increased by ADC number



2 CLK signals shifted by:

$$\Delta\varphi = \pi$$



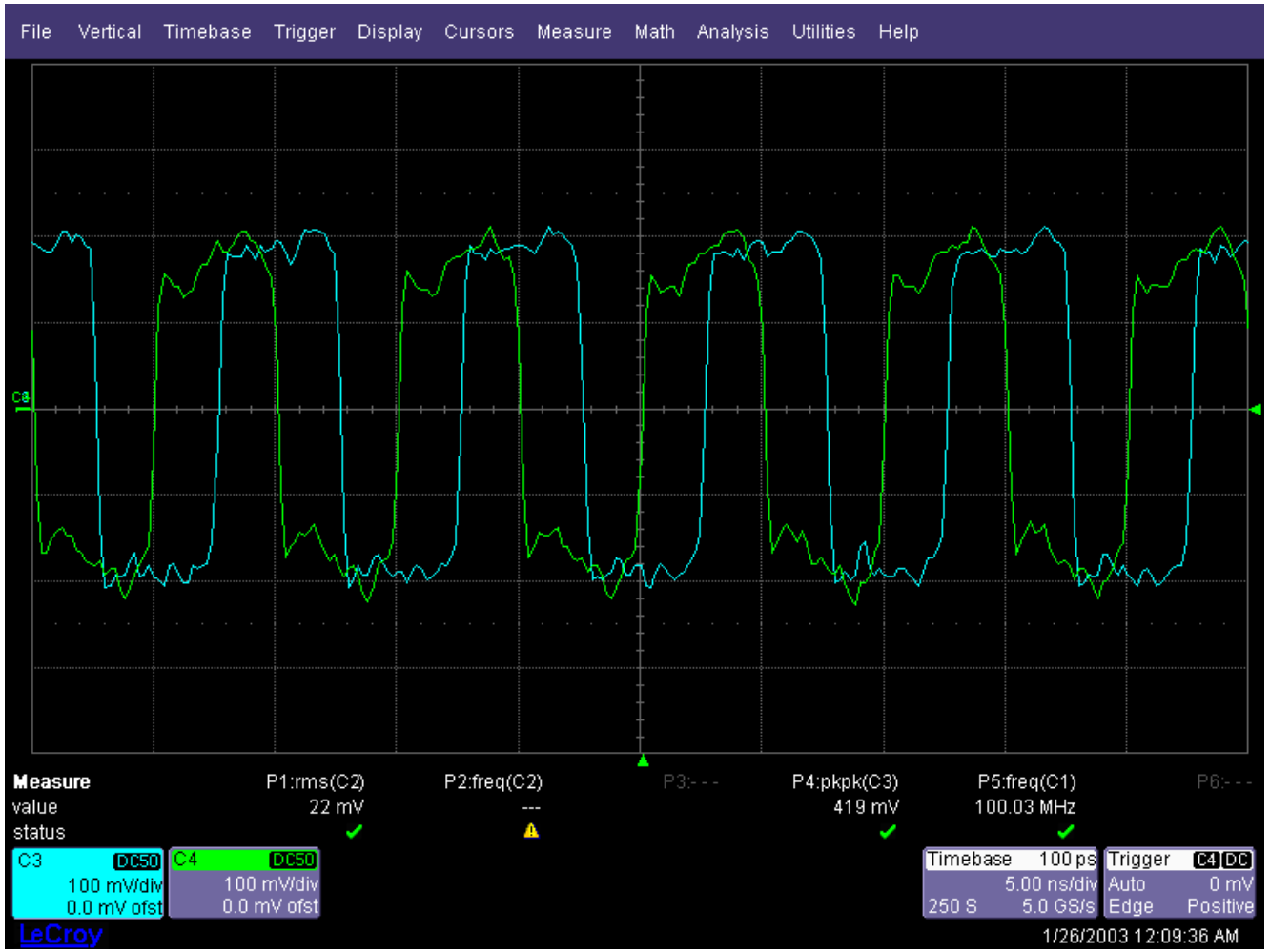
ADCs – Interleaved (II)

4 ADCs – Interleaved:

4 CLK signals shifted by:

$$\Delta\varphi = 2\pi\left(\frac{m-1}{4}\right)$$

m: ADC no.



CPEM 2026 abstract

Ultra-Low Jitter Timing Platform for High-Precision ADC Architectures

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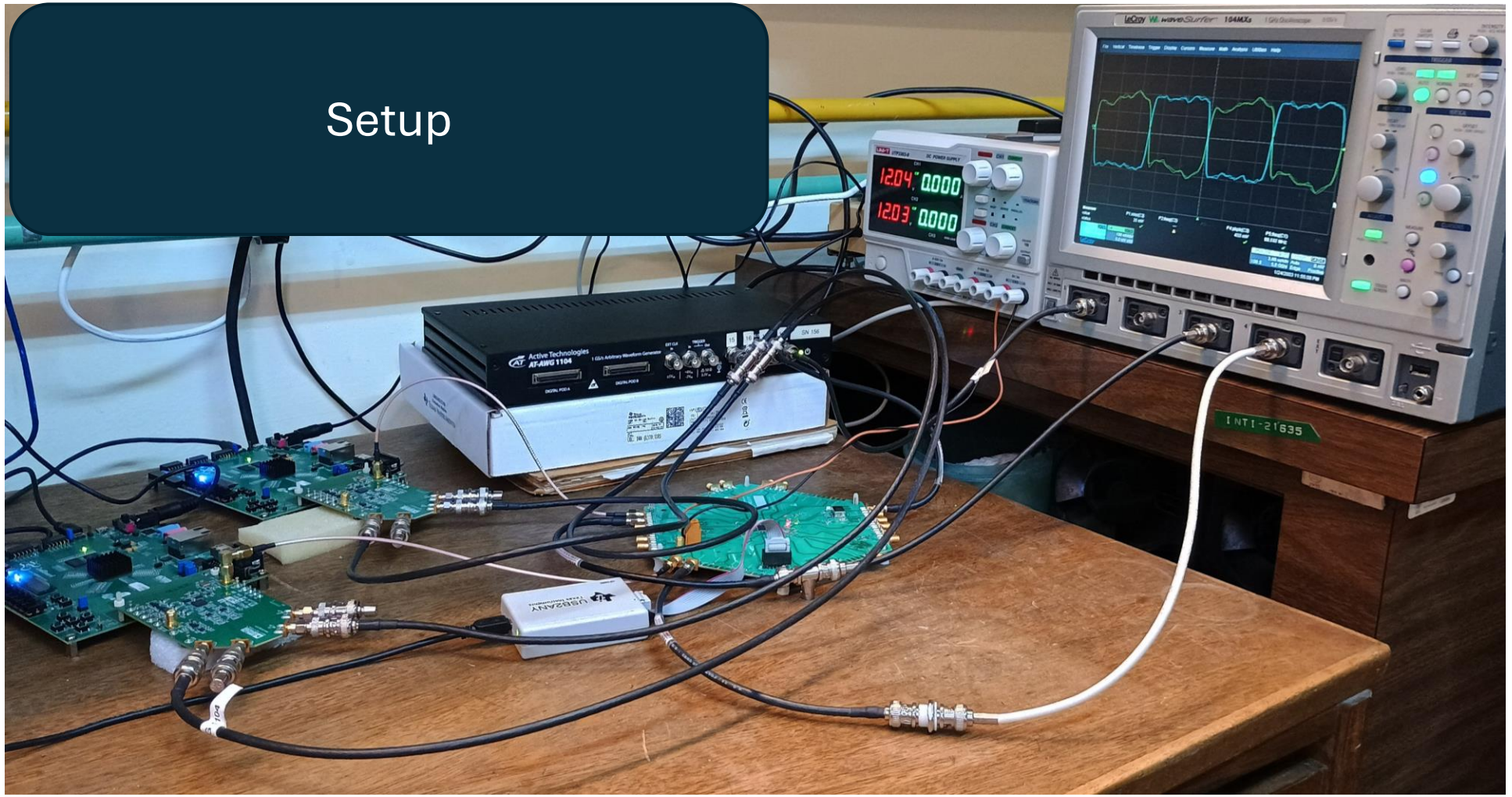
Now we go to INTI's LAB

Setup



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Thank you for your attention!

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