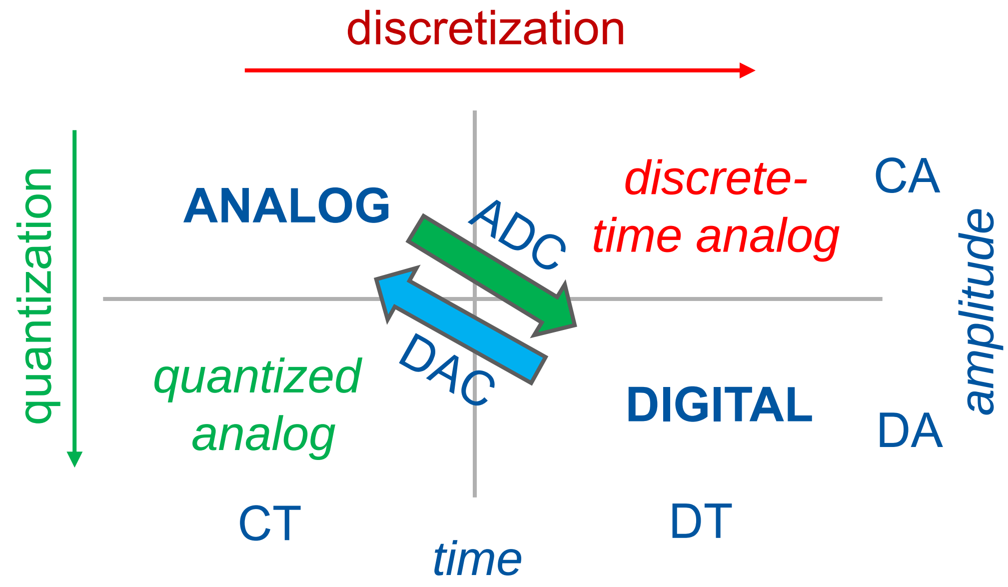
Precision ADCs
current state of the art

True8Digit Workshop
Lisbon, 15 May 2026

Analog-to-digital conversion



Discretization

$$x(t) \rightarrow x[nT_S]$$

Shannon-Nyquist sampling theorem:

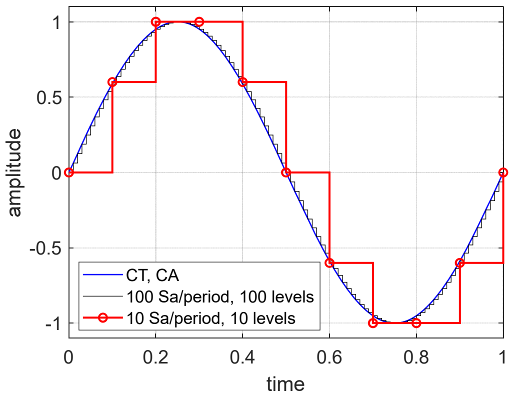
$$f_S > 2f_{\max(signal)}$$

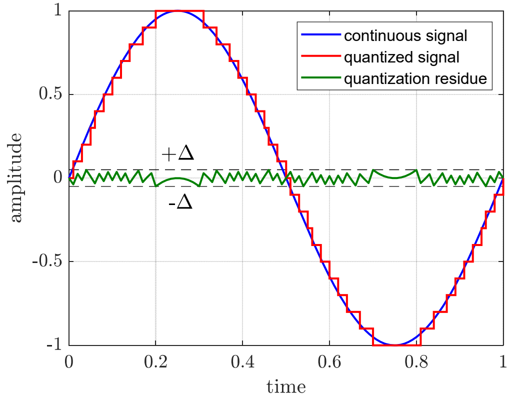
Quantization

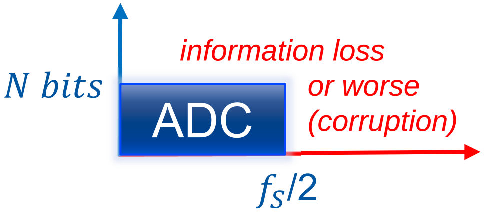
$$Q(x) = \Delta \left\lfloor \frac{x}{\Delta} + \frac{1}{2} \right\rfloor$$

$$\sigma_q = \frac{\Delta}{\sqrt{12}}$$

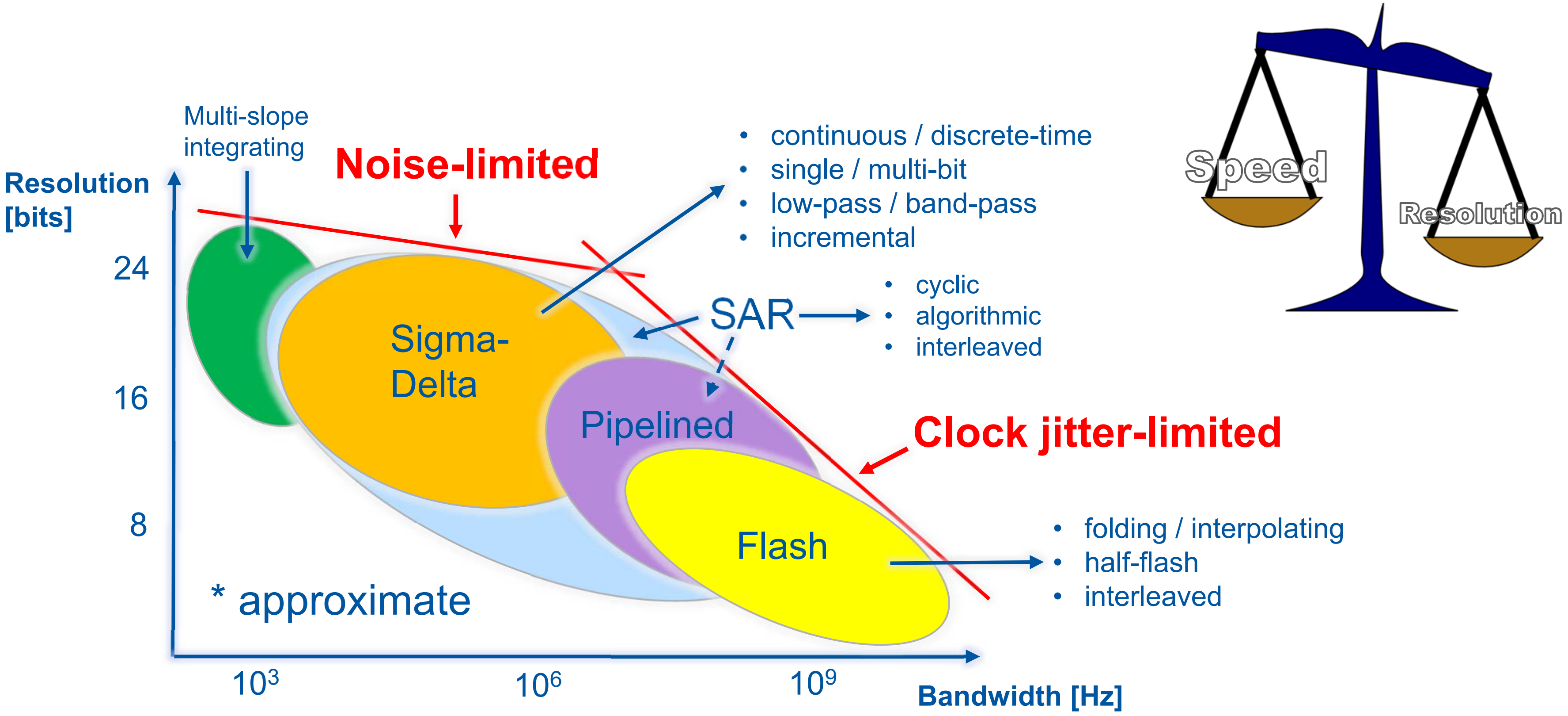
(a.k.a. "quantization noise")







ADC architectures

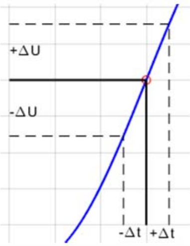


- continuous / discrete-time
- single / multi-bit
- low-pass / band-pass
- incremental

- cyclic
- algorithmic
- interleaved

- folding / interpolating
- half-flash
- interleaved

ADC limitations



Sampling and aperture jitter worst case: Nyquist sampling, middle of sine wave

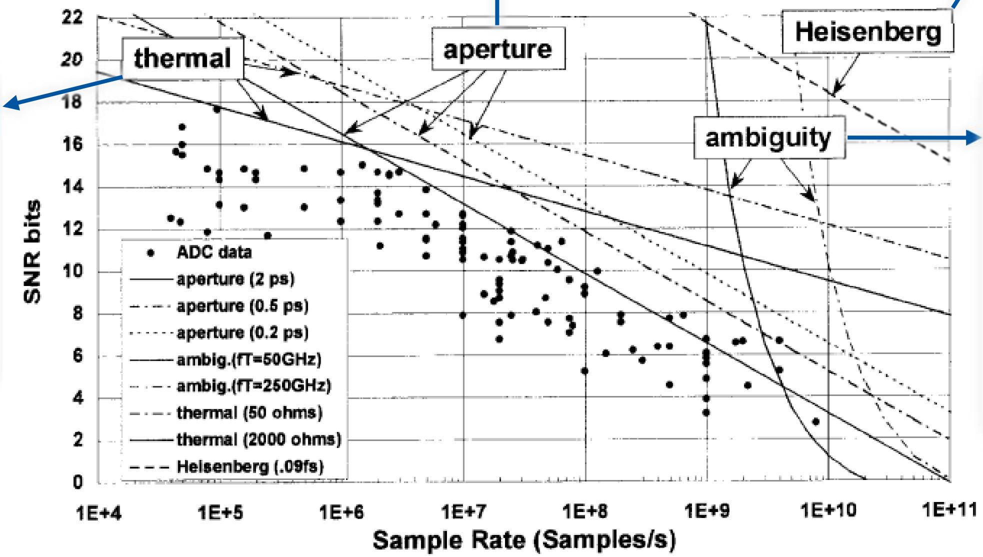
$$B_{\text{aperture}} = \log_2\left(\frac{2}{\sqrt{3}\pi f_{\text{samp}}\tau_a}\right) - 1$$

$$\Delta E \cdot \Delta t = \frac{1}{R}\left(\frac{LSB \cdot T}{4}\right)^2 \geq \hbar$$

uncertainty principle

$$B_{\text{thermal}} = \log_2\left(\frac{V_{FS}^2}{6kTR_{\text{eff}}f_{\text{samp}}}\right)^{1/2} - 1$$

In reality: multiple sources of white noise (thermal, shot noise, etc.) lumped together into a single input-referred ***effective noise resistance***



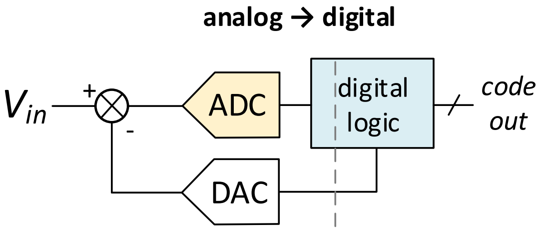
$$B_{\text{ambiguity}} = \frac{\pi f_T}{6.93 f_{\text{samp}}} - 1.1.$$

f_T – transition frequency (transistor technology)

ambiguity – how fast a comparator responds to a ½ LSB step

From R. H. Walden's 1999 ADC survey

High resolution ADCs

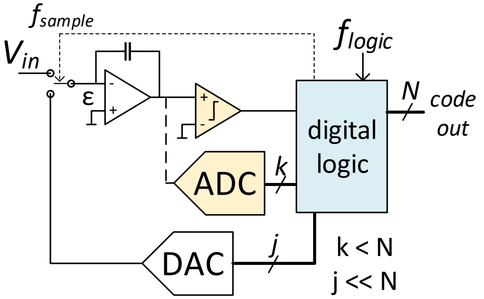


basic structure

Common features

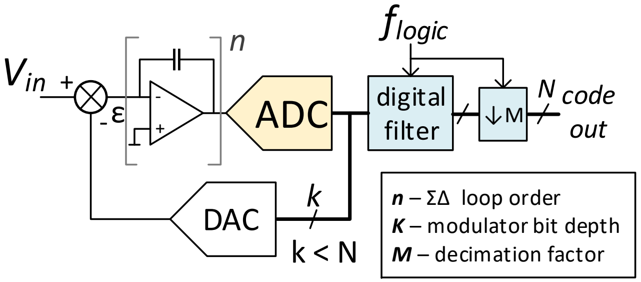
- closed-loop topology
- low-resolution ADC (or comparator) in the loop
- DAC in the feedback path
- requires $f_{logic} >> f_{sample}$

Multislope integrating ADC



High-end DVMs

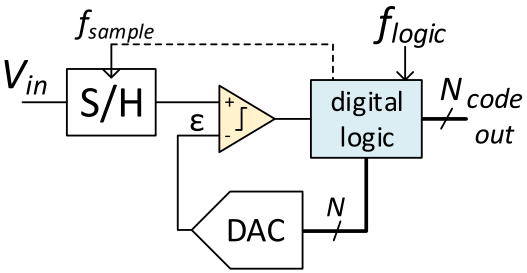
Sigma-Delta ADC



n – ΣΔ loop order
K – modulator bit depth
M – decimation factor

Very wide range of ICs

SAR ADC



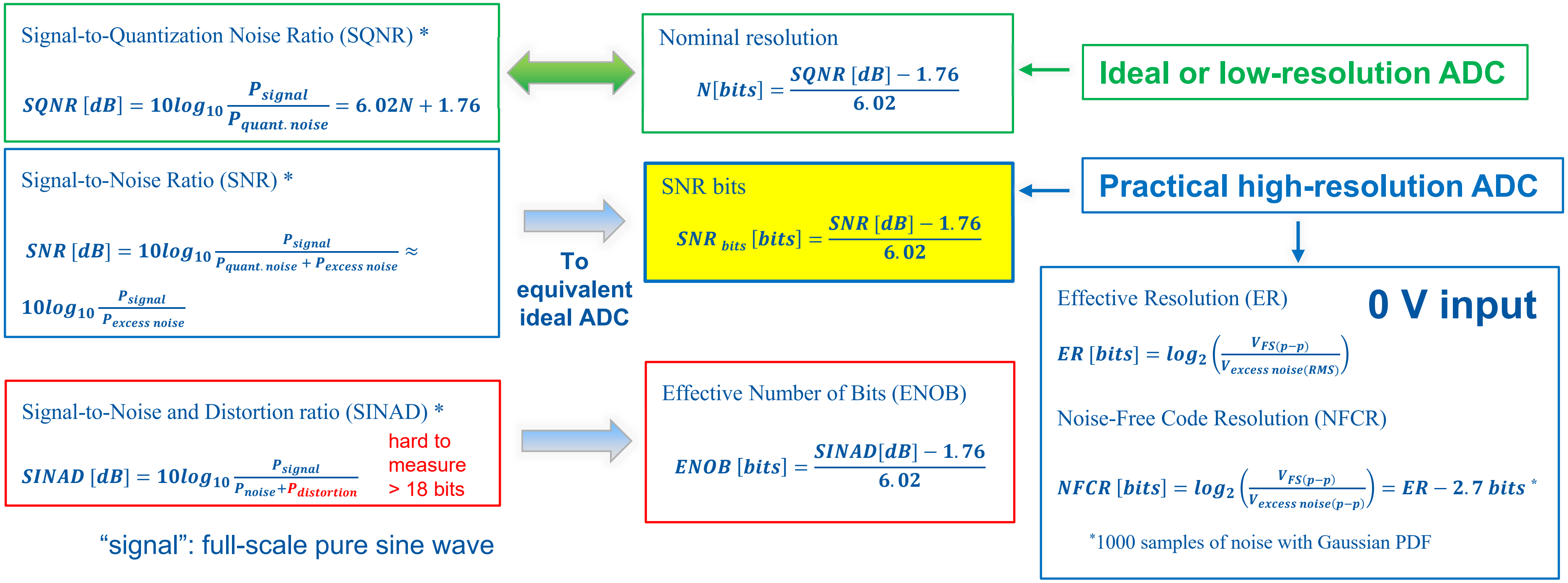
Increasing number of devices with N>20 bits

High-resolution ADC applications

- Digital audio
- Industrial instrumentation & automation
  - force / position / torque measurement
- Sensor readout
  - photometry, magnetometry
  - geophysics / seismology / surveying
- Instrumentation
  - multimeters, data acquisition systems
  - automated test equipment
- Scientific
  - high-precision voltage / current sources
  - electrochemistry, spectroscopy, etc.

Resolution and SNR metrics

- **Nominal resolution** – number of bits at the ADC output interface for a single conversion
- **Digital code resolution** – log_2(*number of digital codes*) ⟶ can be arbitrarily high



Signal-to-Quantization Noise Ratio (SQNR) *

$$SQNR\,[dB] = 10log_{10}\frac{P_{signal}}{P_{quant.\,noise}} = 6.02N + 1.76$$

Nominal resolution

$$N[bits] = \frac{SQNR\,[dB] - 1.76}{6.02}$$

Ideal or low-resolution ADC

Signal-to-Noise Ratio (SNR) *

$$SNR\,[dB] = 10log_{10}\frac{P_{signal}}{P_{quant.\,noise} + P_{excess\,noise}} \approx 10log_{10}\frac{P_{signal}}{P_{excess\,noise}}$$

To equivalent ideal ADC

SNR bits

$$SNR_{bits}\,[bits] = \frac{SNR\,[dB] - 1.76}{6.02}$$

Practical high-resolution ADC

Signal-to-Noise and Distortion ratio (SINAD) *

$$SINAD\,[dB] = 10log_{10}\frac{P_{signal}}{P_{noise} + P_{distortion}}$$

hard to measure > 18 bits

Effective Number of Bits (ENOB)

$$ENOB\,[bits] = \frac{SINAD[dB] - 1.76}{6.02}$$

“signal”: full-scale pure sine wave

Effective Resolution (ER) **0 V input**

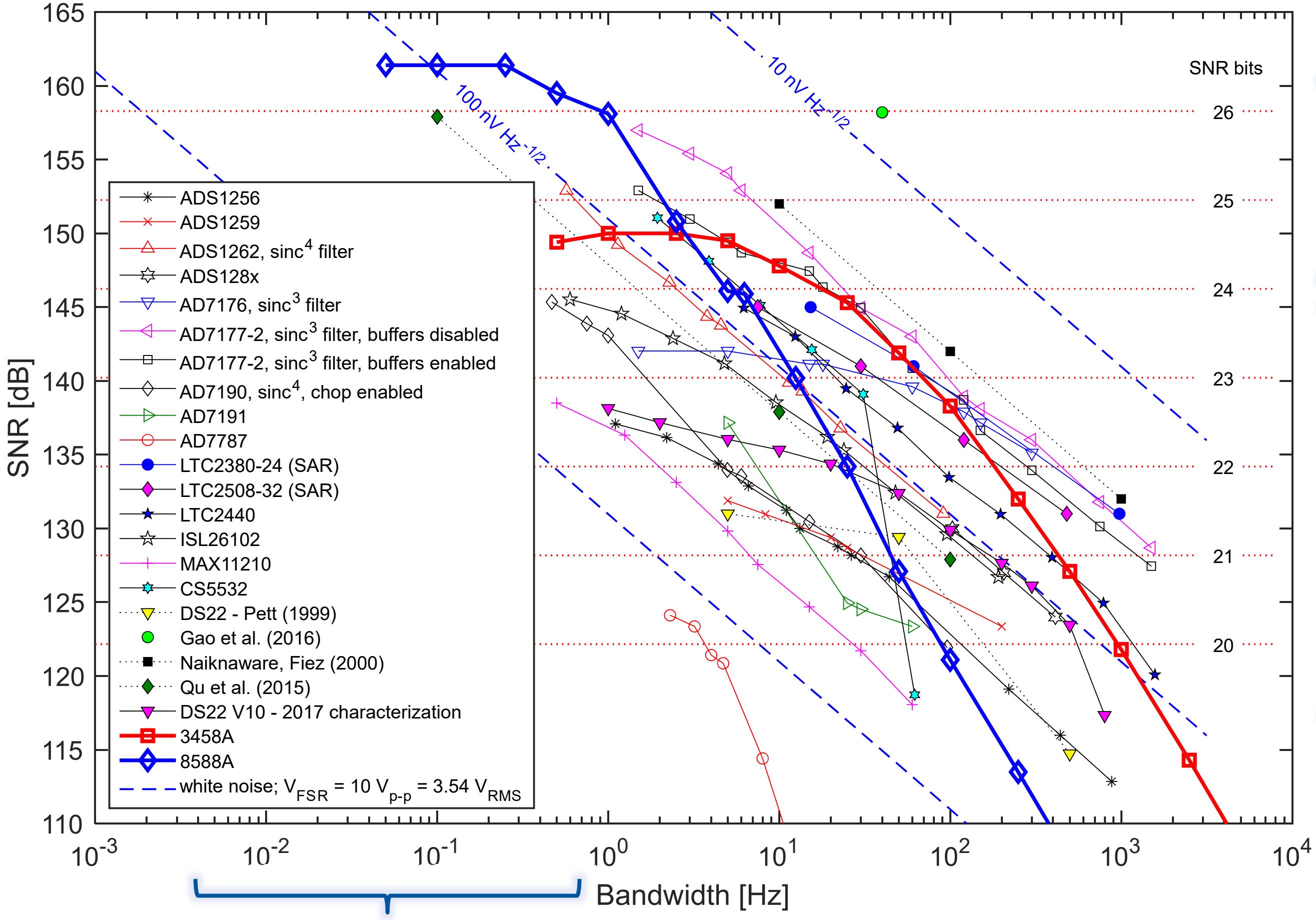
$$ER\,[bits] = log_2\left(\frac{V_{FS(p-p)}}{V_{excess\,noise(RMS)}}\right)$$

Noise-Free Code Resolution (NFCR)

$$NFCR\,[bits] = log_2\left(\frac{V_{FS(p-p)}}{V_{excess\,noise(p-p)}}\right) = ER - 2.7\,bits^{*}$$

[*] 1000 samples of noise with Gaussian PDF

Integrated ADCs – noise and SNR



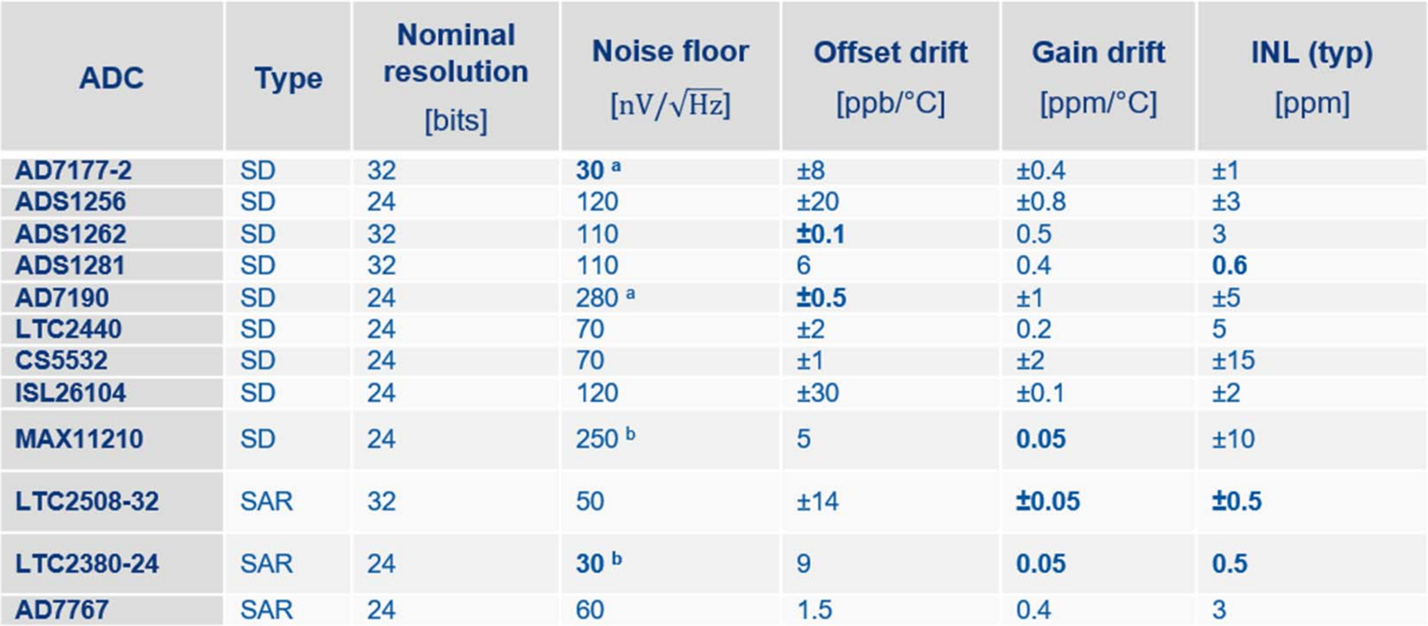
few having
> 24 SNR bits

$$SNR_{\,bits} = \frac{SNR\,[dB] - 1.76}{6.02}$$

big spread

typically no information for sub-Hz noise

Integrated ADCs - performance



ADC	Type	Nominal resolution [bits]	Noise floor $[\mathrm{nV}/\sqrt{\mathrm{Hz}}]$	Offset drift [ppb/°C]	Gain drift [ppm/°C]	INL (typ) [ppm]
AD7177-2	SD	32	**30** [a]	±8	±0.4	±1
ADS1256	SD	24	120	±20	±0.8	±3
ADS1262	SD	32	110	**±0.1**	0.5	3
ADS1281	SD	32	110	6	0.4	**0.6**
AD7190	SD	24	280 [a]	**±0.5**	±1	±5
LTC2440	SD	24	70	±2	0.2	5
CS5532	SD	24	70	±1	±2	±15
ISL26104	SD	24	120	±30	±0.1	±2
MAX11210	SD	24	250 [b]	5	**0.05**	±10
LTC2508-32	SAR	32	50	±14	**±0.05**	**±0.5**
LTC2380-24	SAR	24	**30** [b]	9	**0.05**	**0.5**
AD7767	SAR	24	60	1.5	0.4	3

Estimated, assuming [a] BW = ODR/3; [b] BW = ODR/2

ODR = output data rate

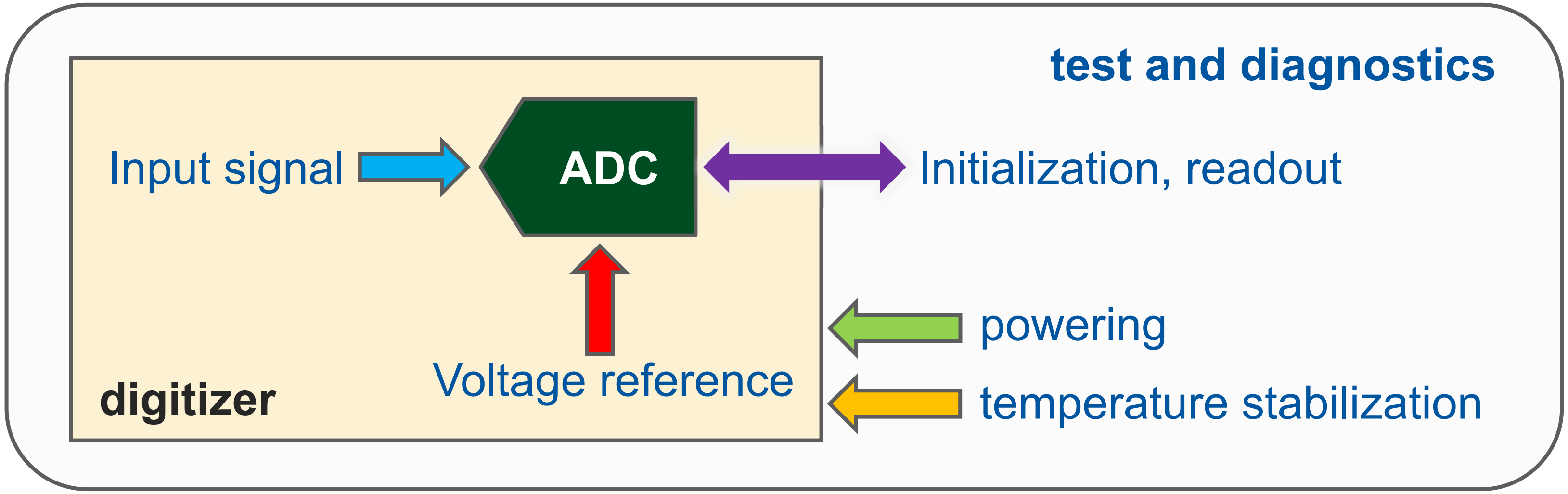
↓ ppb (!)

↓ < ppm

↓ ≈1 ppm

This is a summary from 2017. Since then, some new parts with better performance have appeared.

Building a digitizer around an ADC



- Matching of input signal to ADC range; input impedance, bandwidth
- Matching of external voltage reference to ADC range
- Low-noise, stable powering of ADC and analog circuits
- Digital logic: initialization and readout of ADC, control, diagnostics, data output, etc.
- Temperature stabilization / management (for TC << ppm/°C)
- Built-in test features to facilitate production and maintenance

Discrete or integrated ADC?

- Integrated ADCs:
  - very wide range of functions and performance parameters
  - reasonable cost
  - evaluation and integration infrastructure
- Reasons to develop discrete ADCs?
  - higher DC performance: noise, linearity, TC
  - special operating environments: radiation, temperature, extreme EMI
  - other (very special) system-level needs

Thank you!