METROLOGY PARTNERSHIP | EURAMET

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Measurement of charge injection of electronic switches

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INTI

True 8 DIGIT

Overview

This work → WP2 – Novel composite operational amplifiers and key components characterization "*Characterization of high-quality linear components and **switches** to improve ADC modelling and prediction*"

- Charge injection (Q_{inj}) in CMOS switches
- Modelling and simulation of Q_{inj} in common ADC circuits by INTI
- Q_{inj} traceable measurements at INRIM:
  - ❑ Experimental setup
  - ❑ Measurement methods
  - ❑ Data processing
  - ❑ Results and uncertainty analysis

Why Electronic Switches?

- **Electronic switches are key components in mixed electronics**

  Analog voltage-controlled device and essential for building op-amp circuits, integrators, sample & hold, peak detectors, etc.

  FET & CMOS- most used, JFET- less used

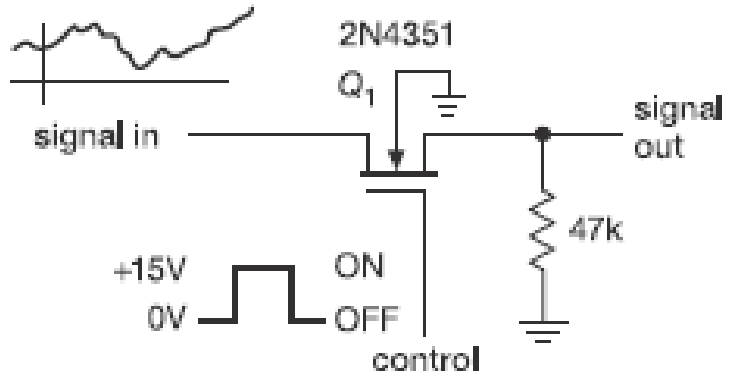
- **Precise applications require electronic switches**

  Ideally zero – ON resistance, without attenuation or nonlinearity

  Ideally ∞ – OFF resistance, open circuit

  Low leakage currents, negligible capacitance to GND

  Low capacitance, negligible coupling to the control digital input



- **Key parameters for switch selections**

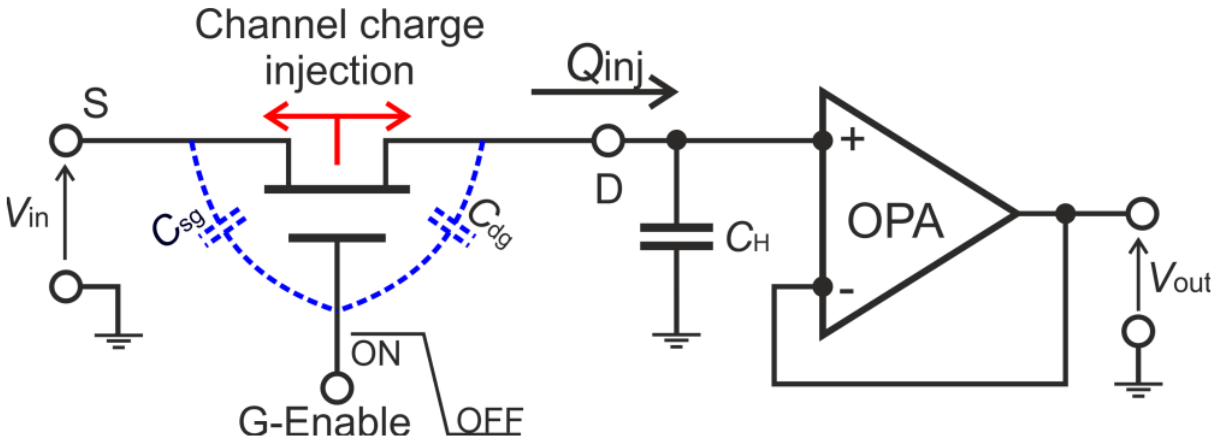
  Voltage range – ON Resistance – Switching speed/frequency – Capacitance

  Charge injection – Switching time(Rise/Fall time) – Settling time, etc.

  Break-before-make switching (BBM)

Charge injection in CMOS switches

Simplified sample-and-hold circuit



Closed → voltage on C_H tracks the input signal V_{in}

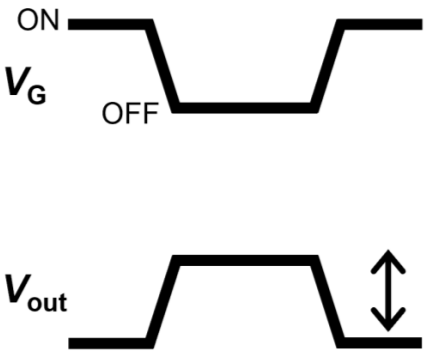
Open → C_H holds its voltage until the switch is closed

When the switch turns off → unwanted net charge transfer to C_H due to:

channel charge injection: charge within the channel has to go somewhere…

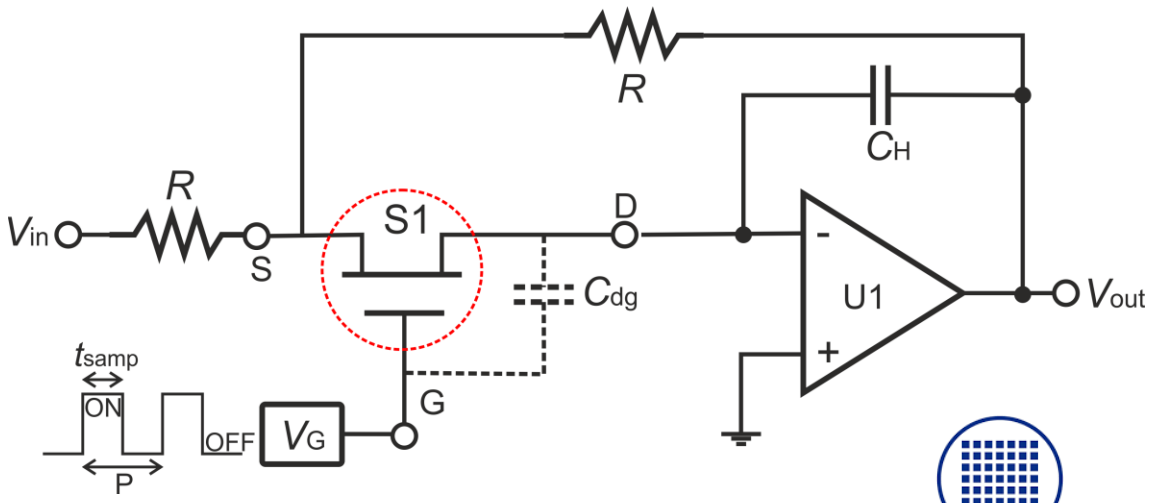
clock feedthrough: overlap capacitance C_{dg} between drain and gate

→ **pedestal voltage ΔV_{out} on the hold capacitor C_H**



Simulation of common circuits (1)

Closed-loop sample-and-hold circuit

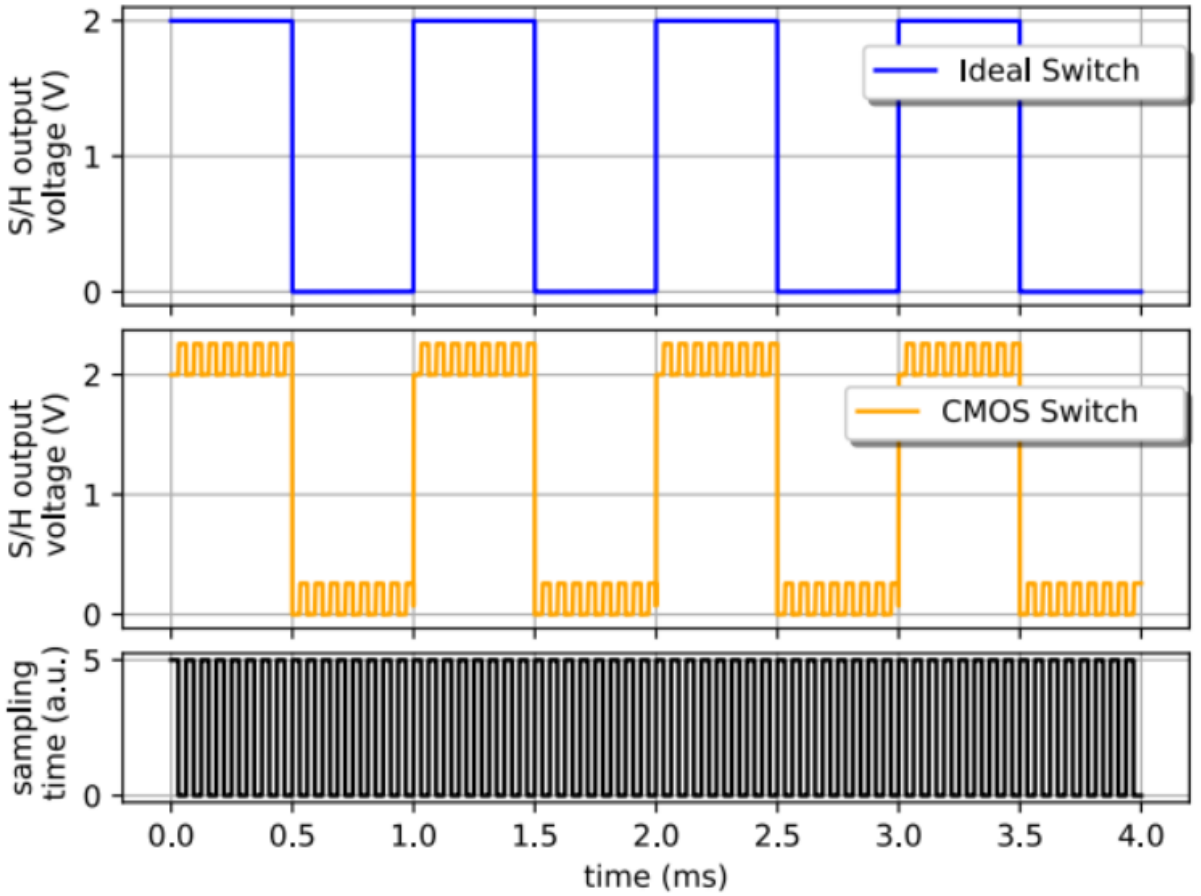


INTI

LTspice®

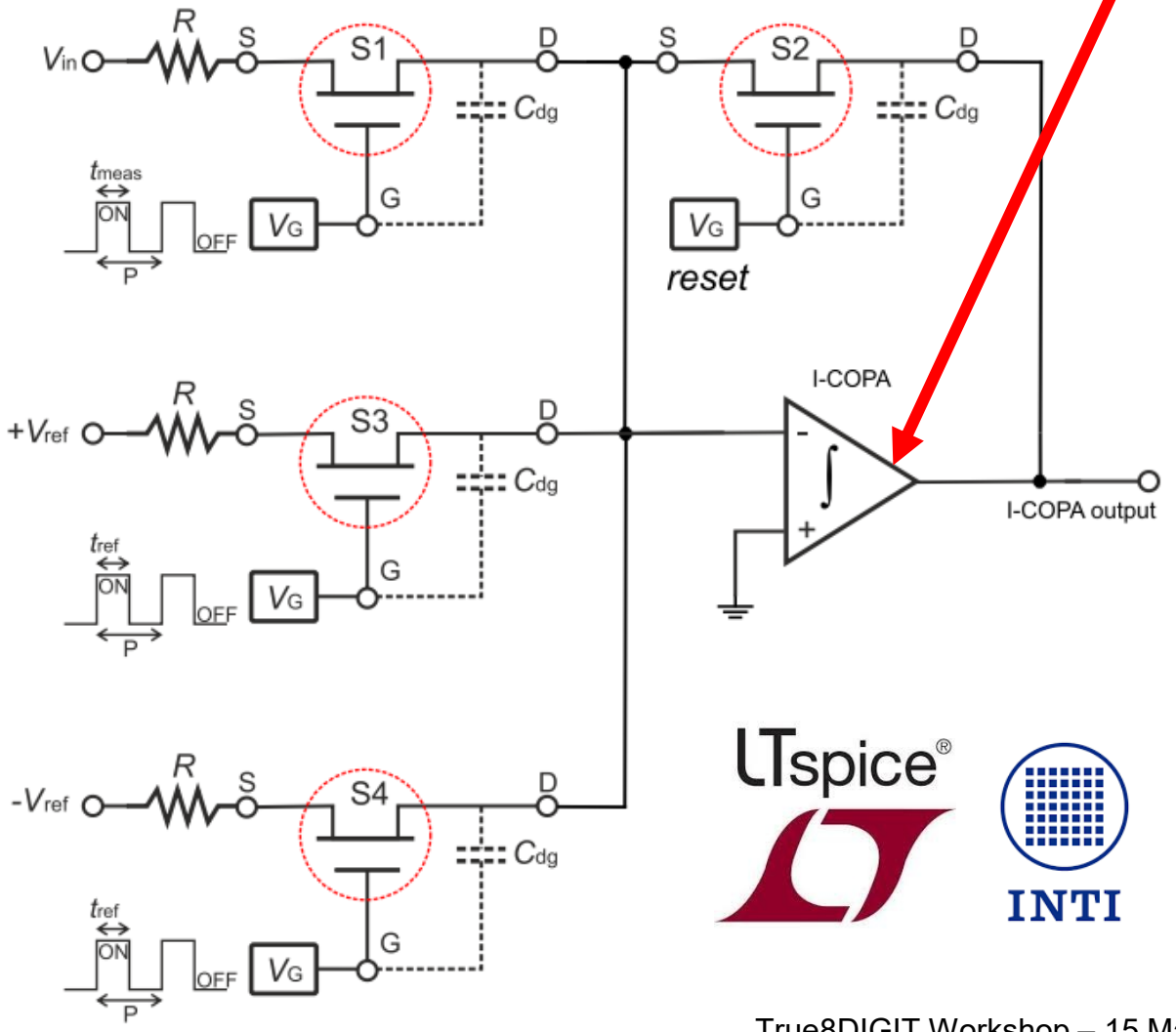
C_H = 100 pF
Ideal switch → C_{dg} = 0
CMOS switch → C_{dg}/ C_H = 0.1

Voltage deviation of 250 mV (Q_{inj} = 25 pC)



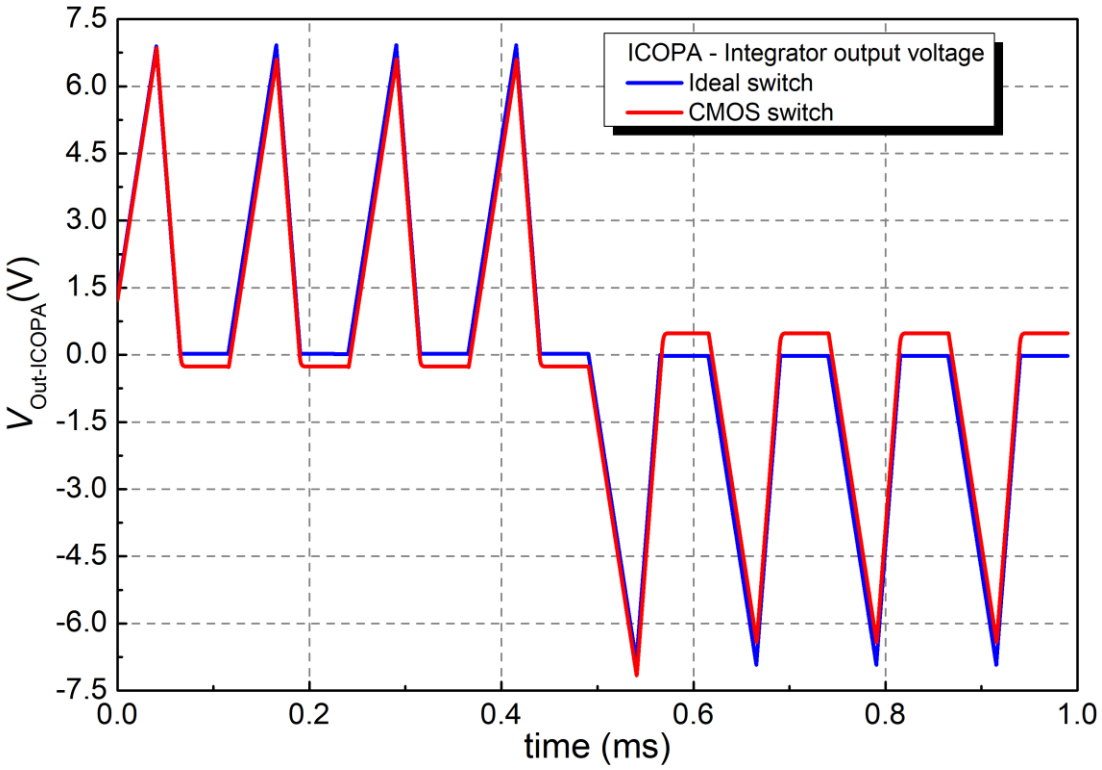
Simulation of common circuits (2)

Front-End Integrating ADC



Integrating Composite Operational Amplifier (**I-COPA**)

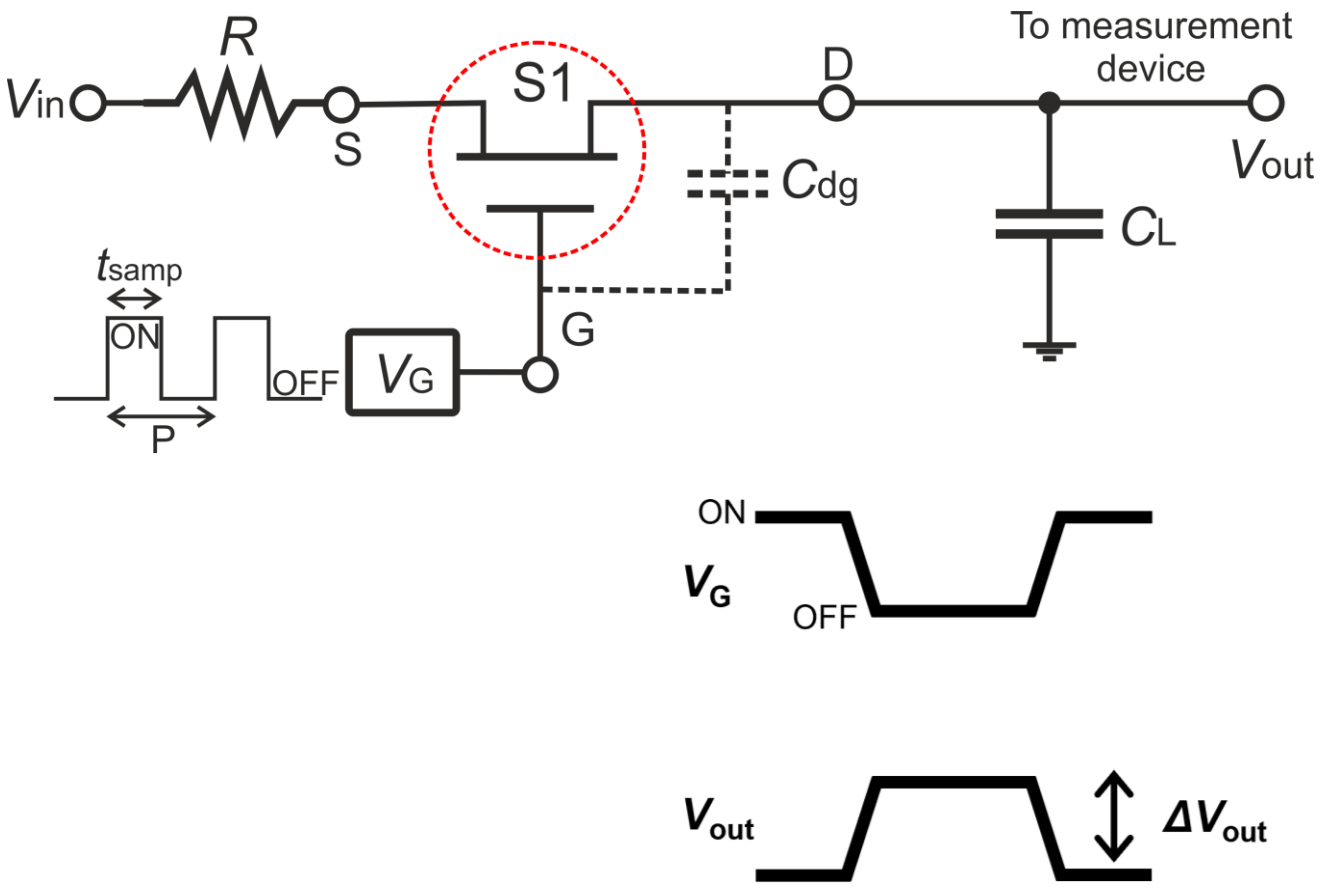
Input voltage: 5 $V_{pk\text{-}pk}$, 1 kHz square wave
8 samples per period



Voltage deviation up to 500 mV

Measurement of charge injection Q_{inj}

Typical measurement setup reported on switch data sheets



Load capacitor $C_L \geq 1$ nF

Parasitic capacitances (C_P) neglected:
$C_L >> C_P$

Full voltage V_{out} measured with voltmeter/sampler

$$Q_{inj} = C_L \times \Delta V_{out}$$

Q_{inj} measurement setup

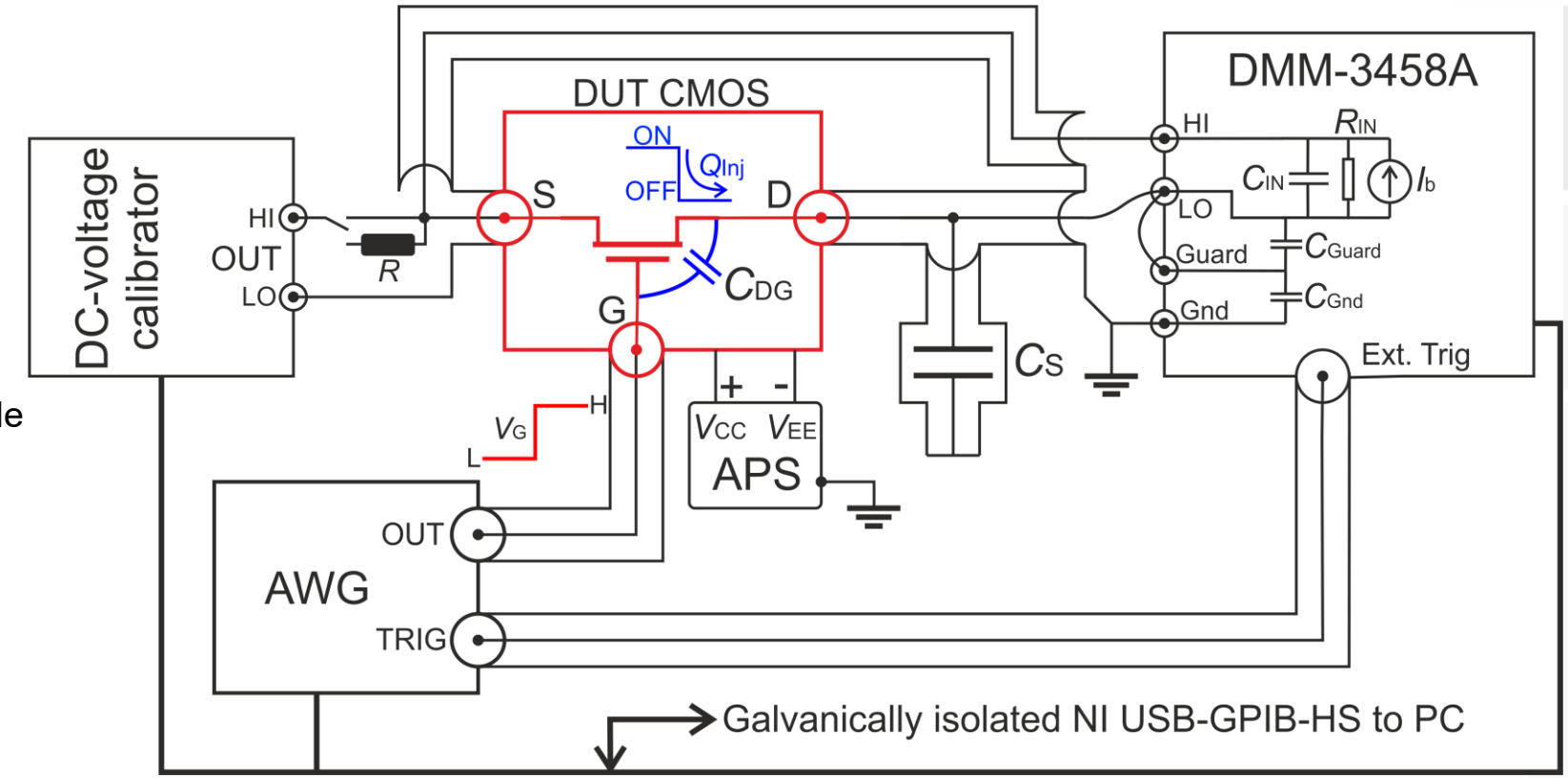
Similar setup, but…

- **Differential** → voltage measured between D and S, instead of D and ground (lower magnitude, better DMM resolution)

  Keysight 3458A as DMM in DCV digitizing mode (1 V range, 100 kS/s, aperture time 1.4 µs)

- **3 calibrated** in-gas standard capacitors C_S as load ($C_L = C_S$),

  → C_S = 10, 100, 1000 pF



AWG: 0-3 V square wave, 1 kHz, trigger to DMM;
Fluke 5730A calibrator to provide highly-stable DC input voltages

All traceable to primary standards!

Q_{inj} measurement setup

Similar setup, but…

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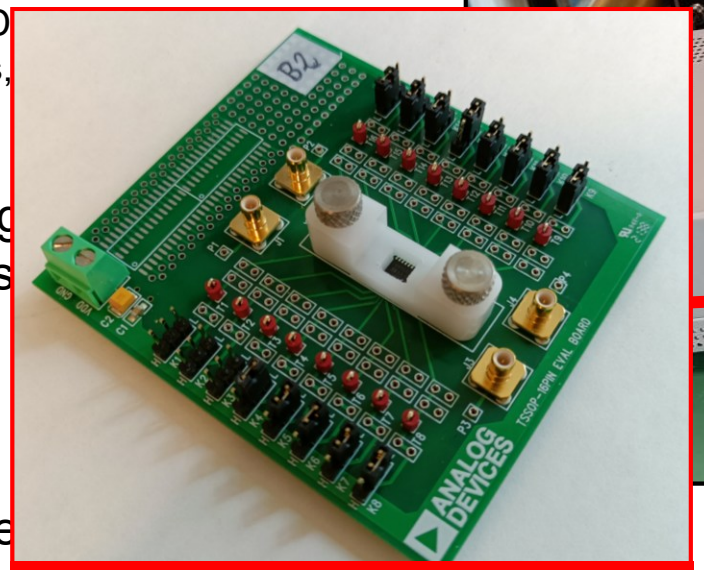
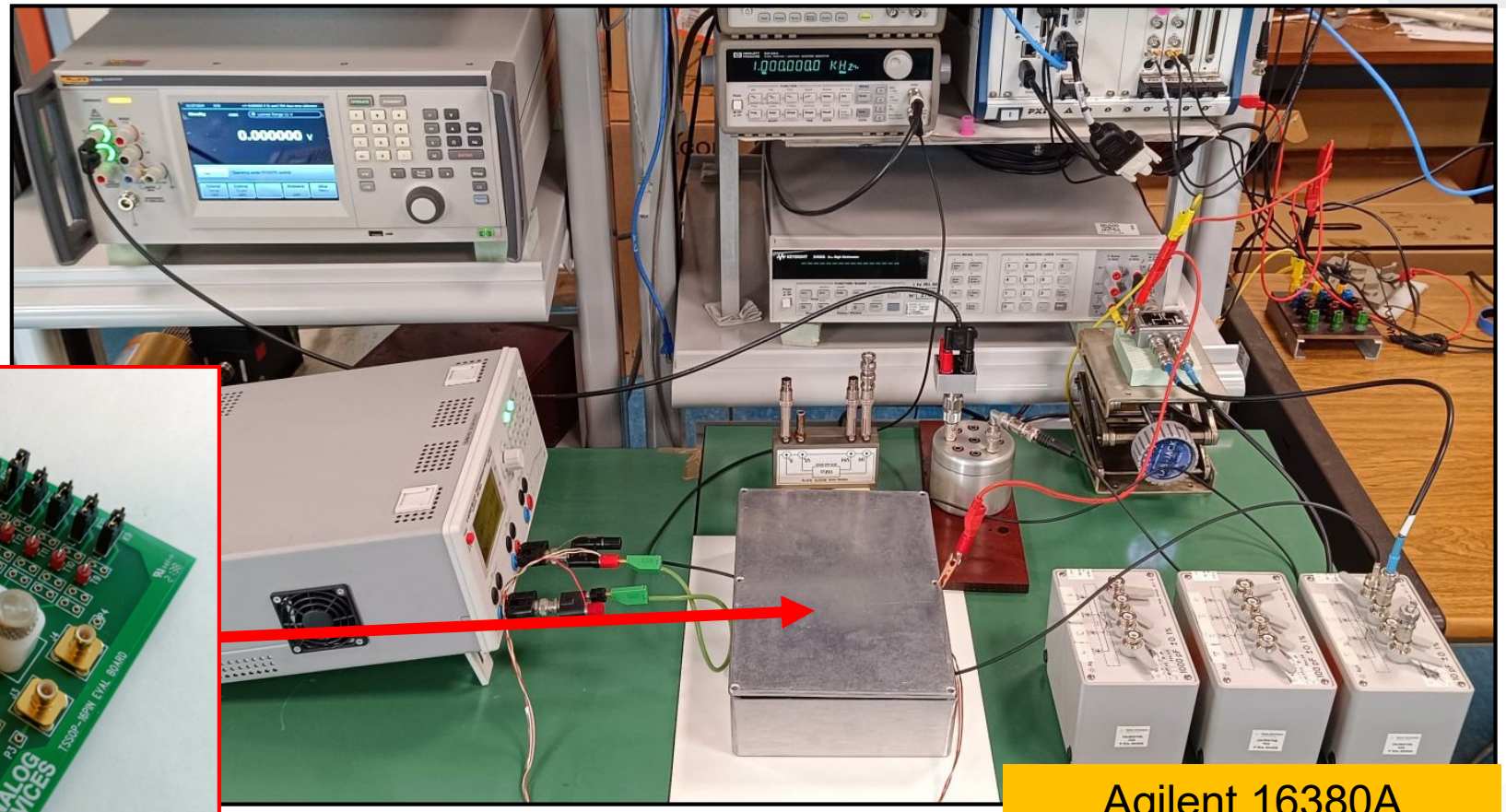


TSSOP-16 pin Eval board

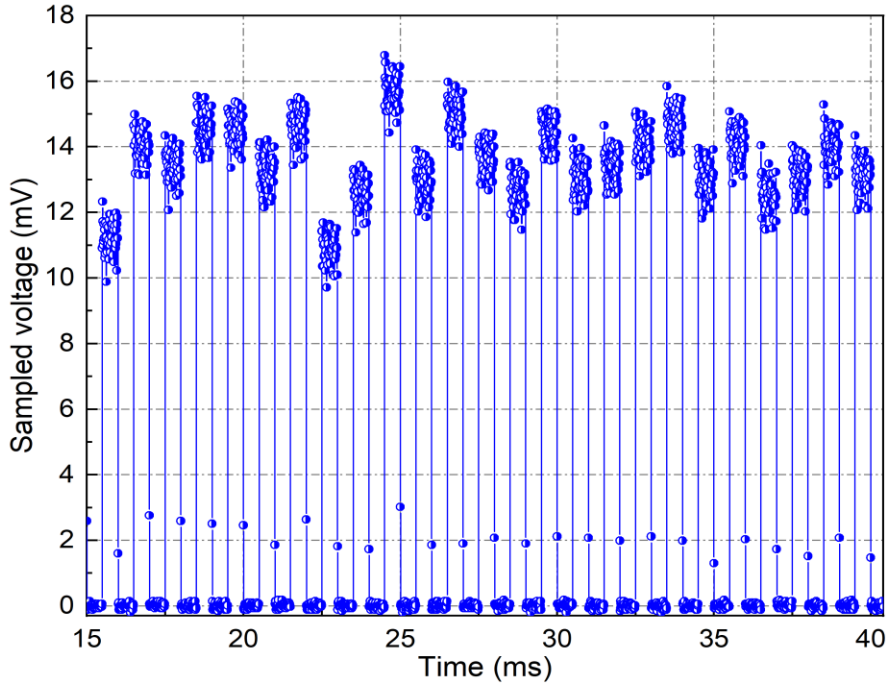


Agilent 16380A
standard air capacitors

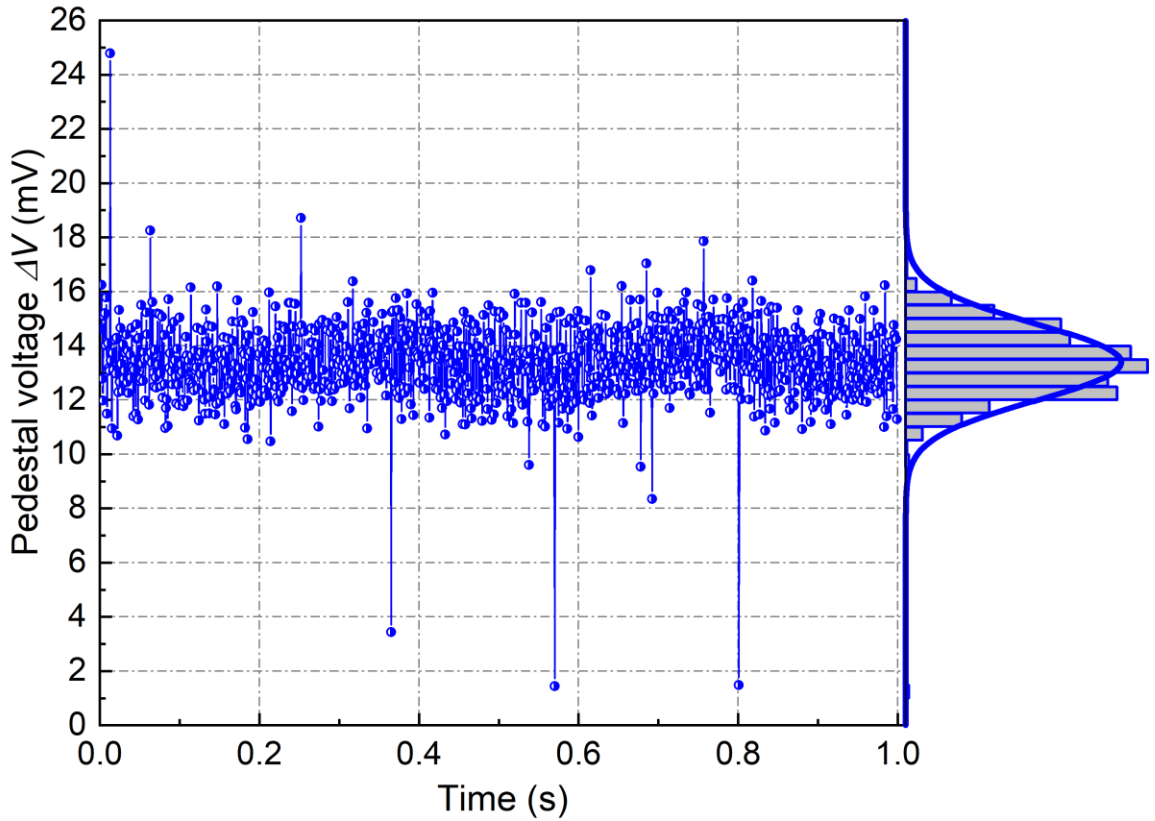
All traceable to primary standards!

Measurement strategy: pedestal voltage

1 kHz switch ON/OFF frequency → 1 s measurement → 1000 transitions → 1000 pedestal voltages



MATLAB algorithm to extract ΔV_{out} for each switch transition



Average and standard deviation of ΔV_{out} at fixed V_{in} and C_s

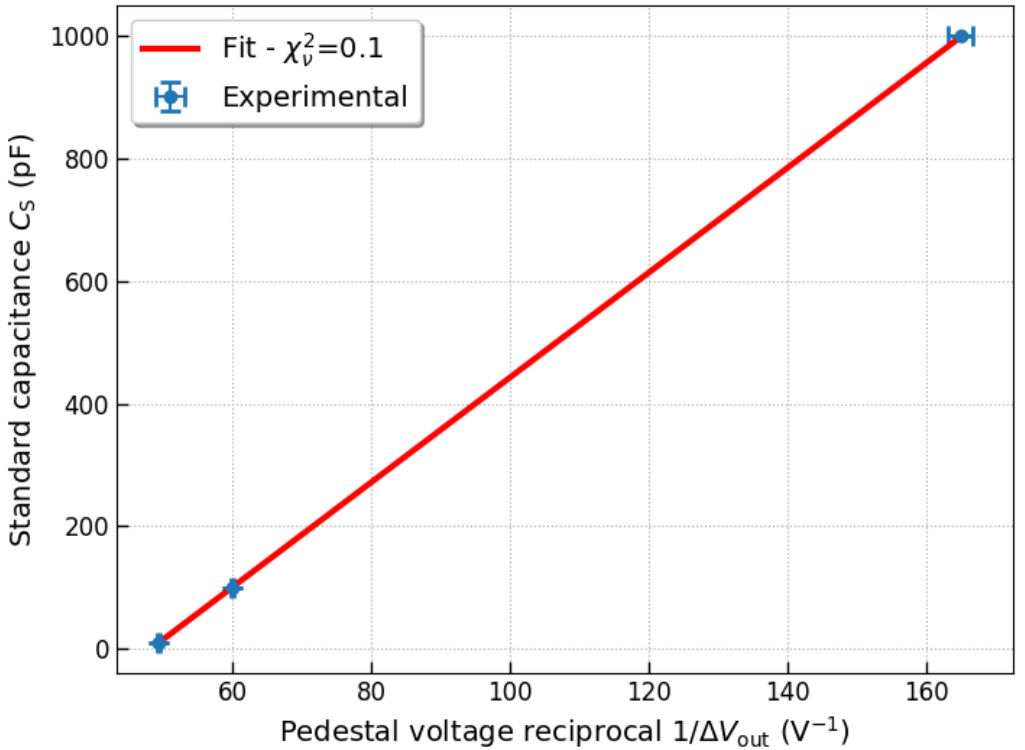
(V_{in} = 1 V and C_s = 10 pF)

Q_{inj} evaluation: 3-capacitance linear fit

Mathematical model → $Q_{inj} = (C_s + C_P) \cdot \Delta V_{out}$

$$C_s = Q_{inj} \cdot (\Delta V_{out})^{-1} - C_P \rightarrow y = a\,x + b$$

- Three $((\Delta V_{out})^{-1}, C_s)$ pairs → linear fit to extract Q_{inj} and C_P
- Orthogonal Distance Regression (ODR) with both x and y uncertainties
- **Q_{inj} and C_P and uncertainties from the regression**
- χ^2 to assess the goodness of the linear model

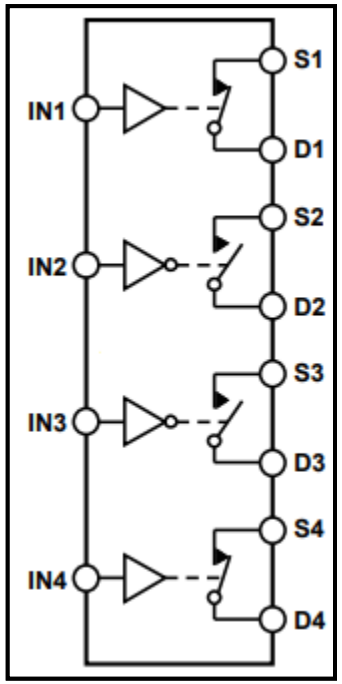


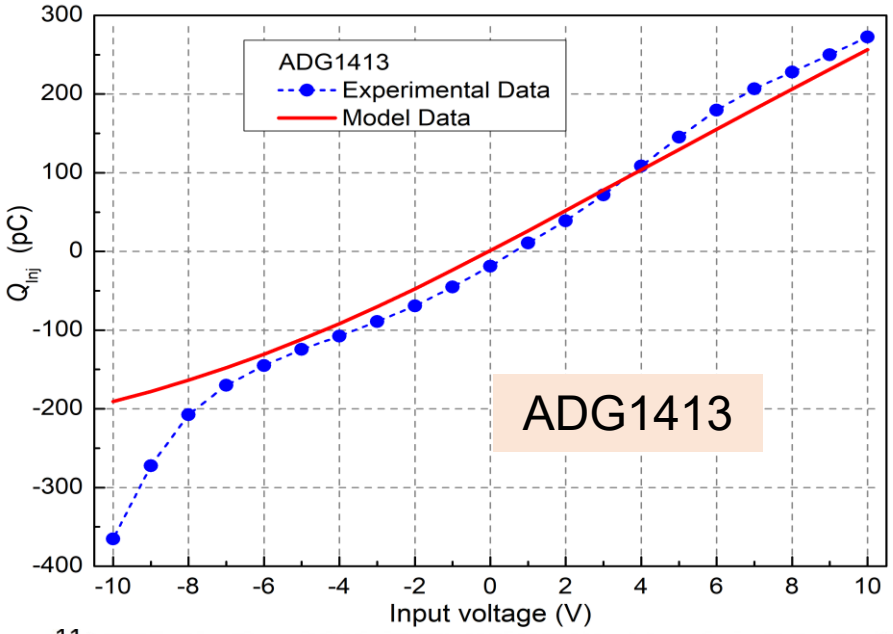
Q_{inj} of commercial CMOS switches (1)

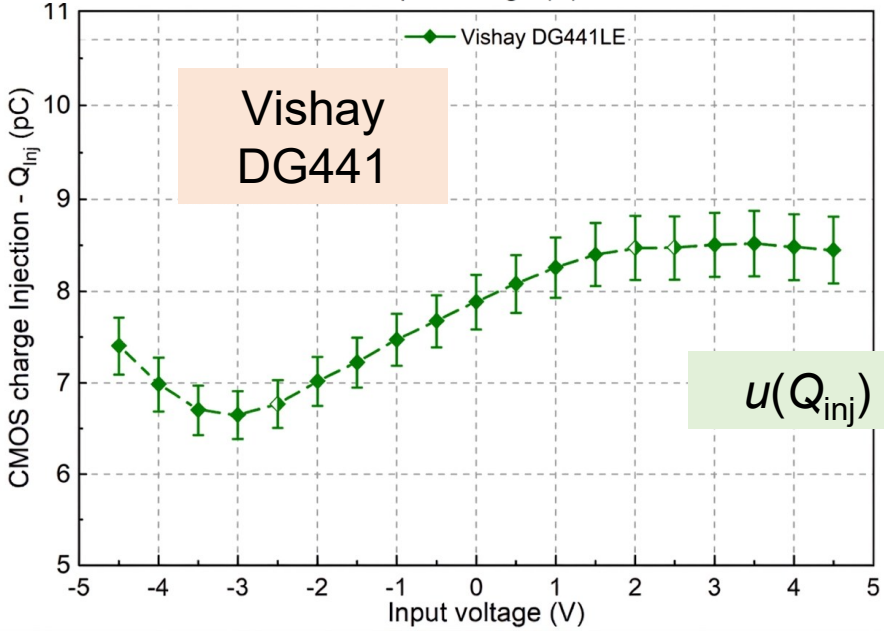
ADG1413 and **Vishay DG441**

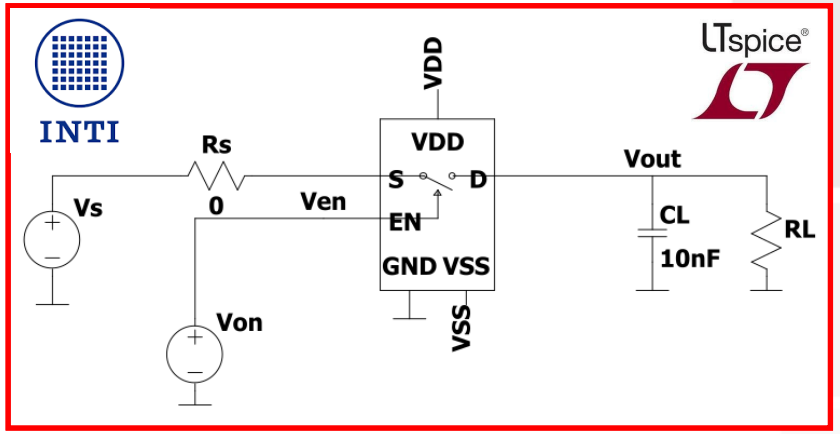
4 x **SPST** switches per IC

±15 V / ±5 V supply









$u(Q_{inj}) \approx 2$ pC @ $|Q_{inj}| < 50$ pC

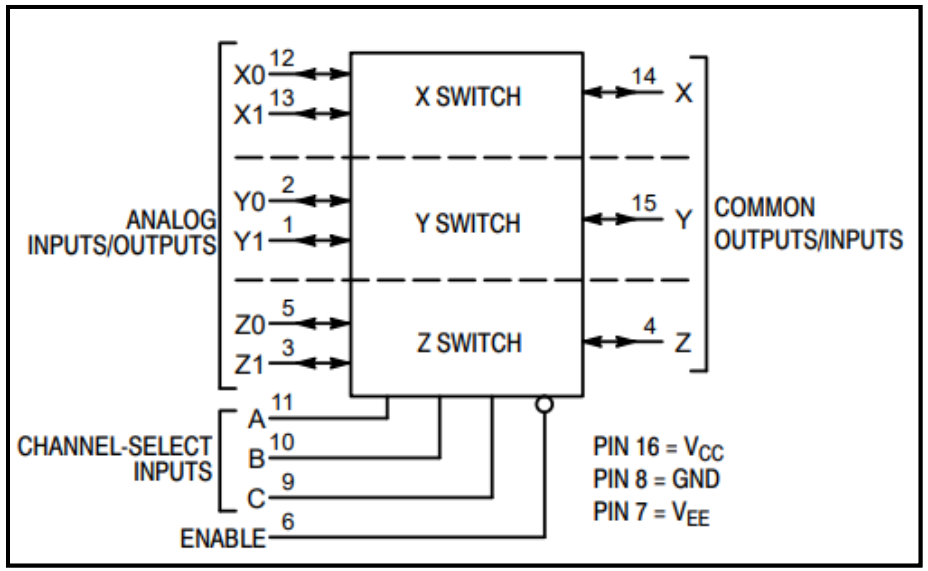
$u(Q_{inj}) \approx 20$ pC @ $|Q_{inj}| \approx 200$ pC

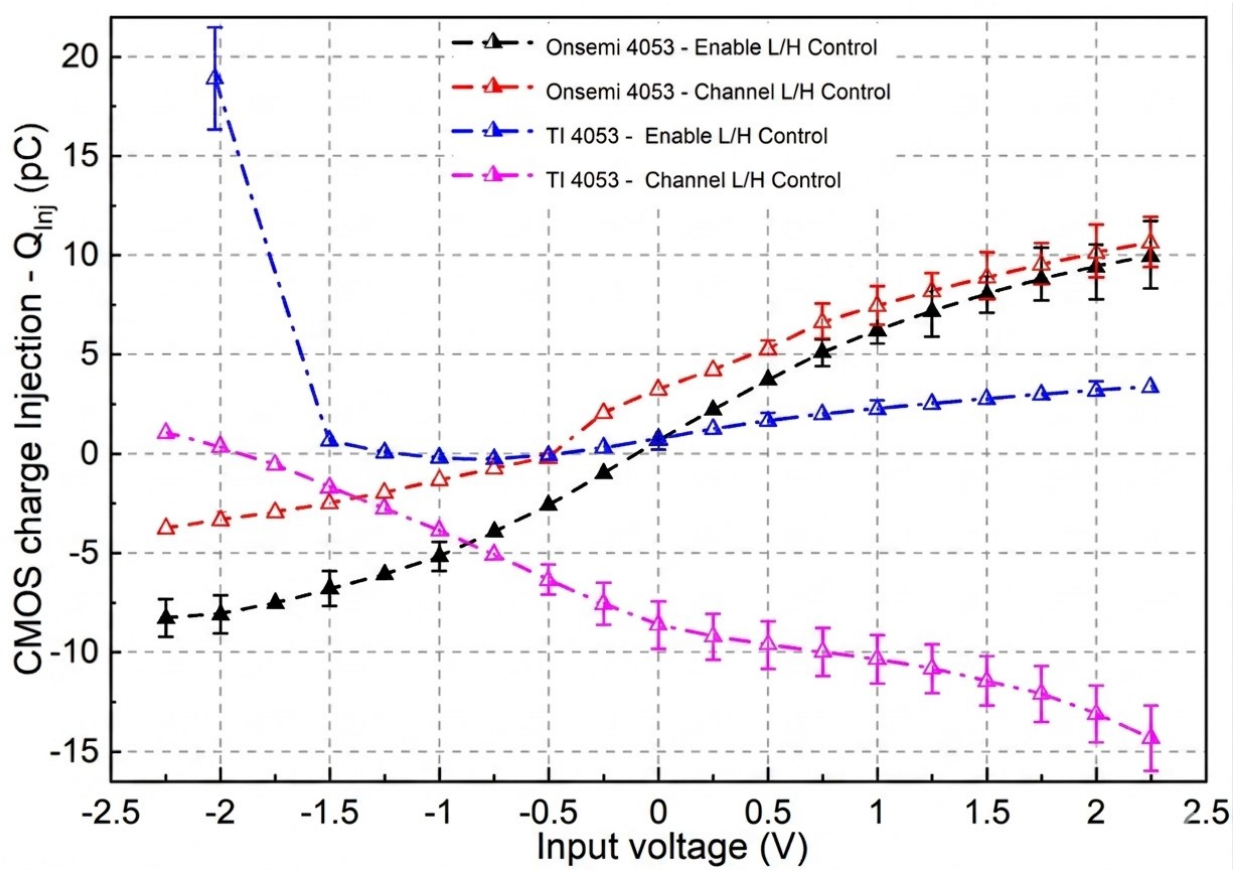
$u(Q_{inj}) <\approx 0.25$ pC

Q_{inj} of commercial CMOS switches (2)

Texas Instruments 4053 and Onsemi 4053:

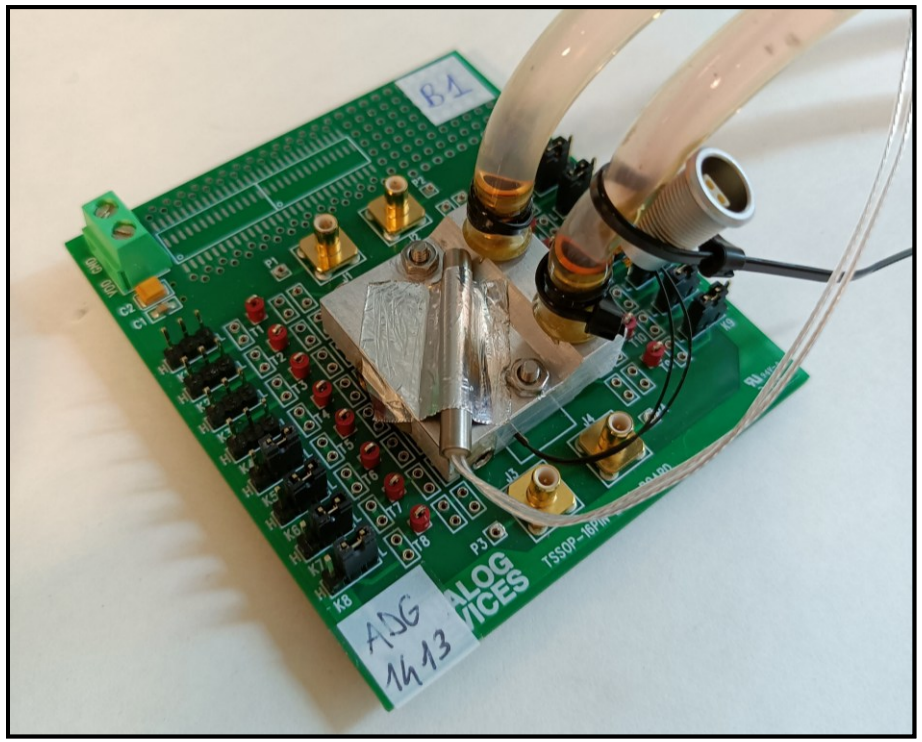
- 3 x **SPDT** switches per IC
- ± 3 V dual supply
- V_{in} limited below 3 V
- Two modes: Channel select / ENABLE

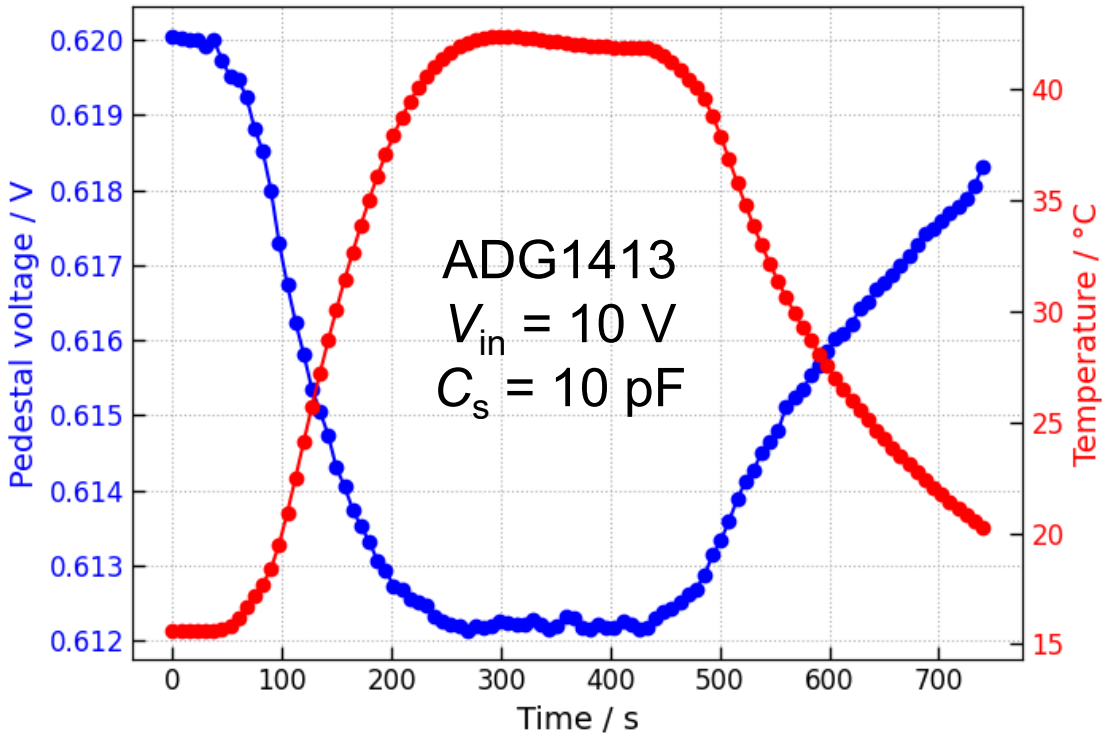




Switch temperature influence (1)

- Study Q_{inj} dependence on temperature T ~ 15°C - 40°C
- Purposely-designed T-controlled heatsink onto the IC, thermoelectric Liquid Chiller and PT100





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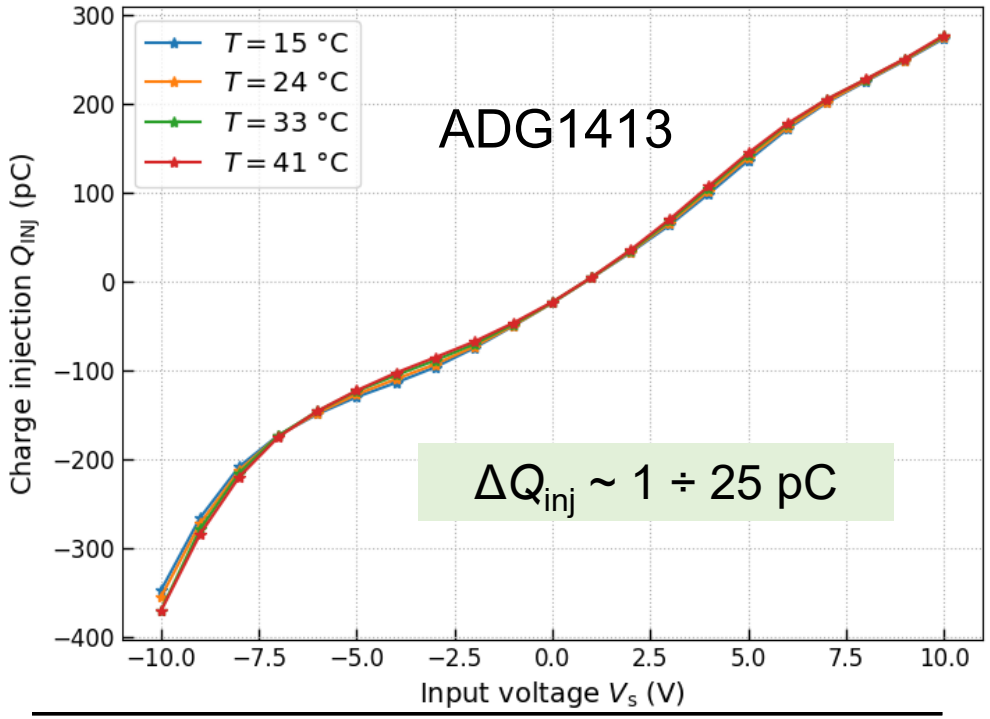

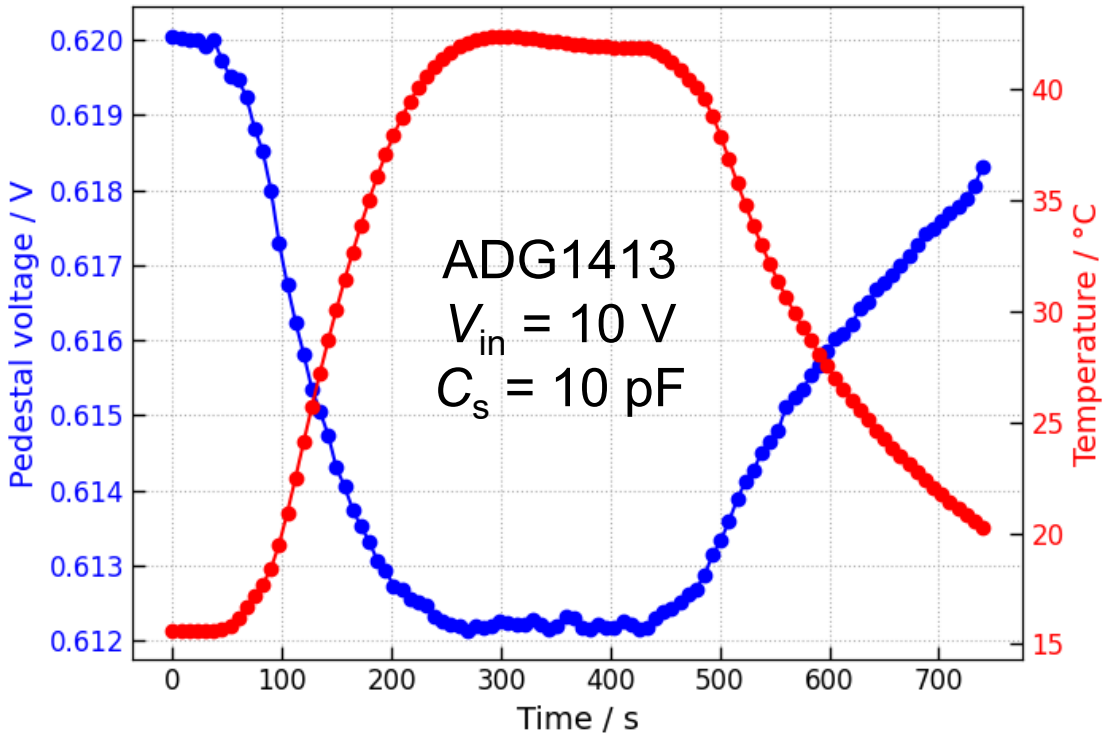

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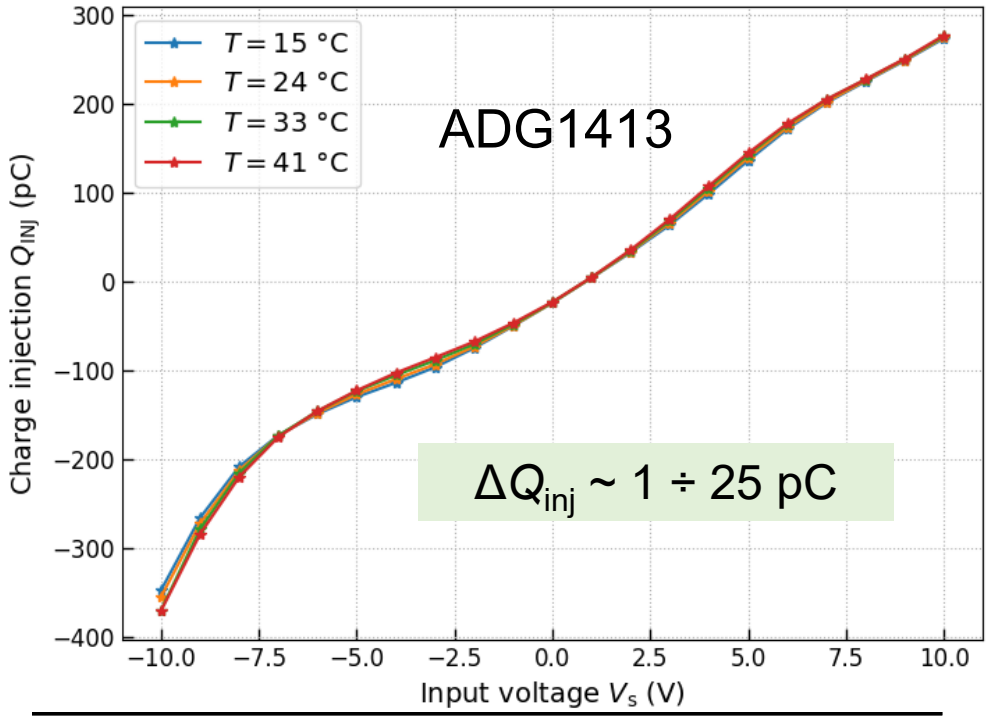
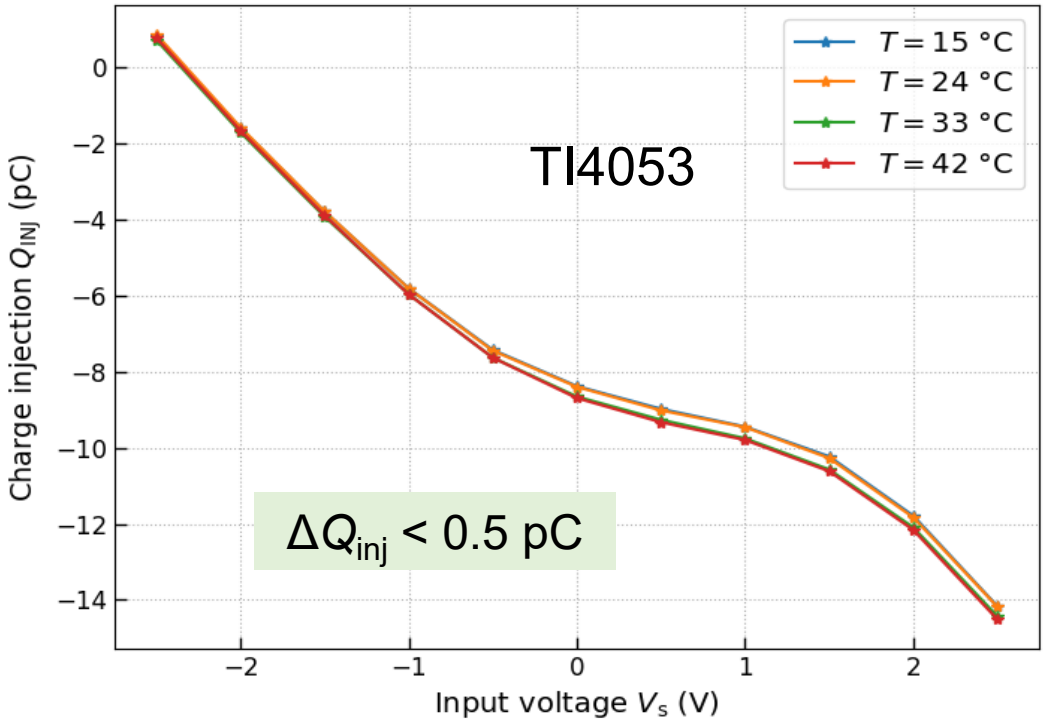
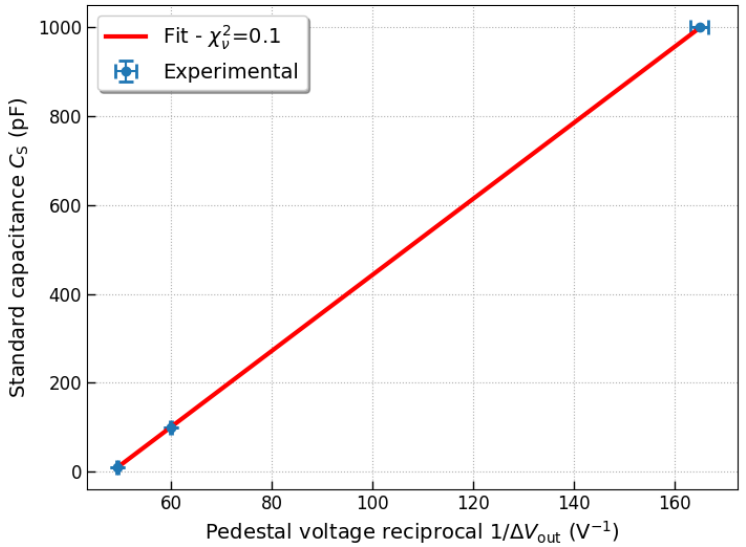




Q_{inj} uncertainty budget (1)

Mathematical model → $C_s = Q_{Inj} \cdot (\Delta V_{out})^{-1} - C_P \rightarrow y = a\,x + b$



Three (1/ ΔV_{out} , C_s) pairs

ΔV_{out} (=1/x) uncertainty sources:

- ❑ Repeatability (Type A)
- ❑ Digitizer gain and non-linearity
- ❑ Digitizer resolution (≈40 µV)
- ❑ Capacitor discharge

C_S (=y) uncertainty sources:

- ❑ Calibration
- ❑ Temperature dependence
- ❑ Time drift
- ❑ AC-DC difference

Q_{Inj} uncertainty by propagating the input uncertainties through the ODR algorithm

→ finally scaled by sqrt(χ^2) to take the goodness of the linear model into account

Q_{inj} uncertainty budget (2)

Uncertainty source $u(x_i)$	$u_i(Q_{Inj})/Q_{Inj}$ (%) $1\,pC \lesssim Q_{Inj} < 30\,pC$	$u_i(Q_{Inj})/Q_{Inj}$ (%) $30\,pC \lesssim Q_{Inj} < 350\,pC$
C_S : Standard capacitance		
Calibration @ 1 kHz (Type B)	0.011 – 0.001	0.002 – 0.002
Temperature effect (Type B)	0.011 – 0.001	0.002 – 0.002
Time drift (Type B)	0.009 – 0.004	0.004 – 0.004
AC-DC relative difference (Type B)	0.013 – 0.009	0.011 – 0.011
ΔV : Pedestal voltage measurement		
Repeatability @ 1 s (Type A)	1.583 – 0.329	0.091 – 0.011
Digitizer gain (Type B)	0.002 – 0.001	0.001 – 0.001
Digitizer non-linearity (Type B)	10.95 – 1.187	0.313 – 0.030
Digitizer resolution (16 bit) (Type B)	3.709 – 0.398	0.112 – 0.011
Capacitor discharge time (τ) (Type B)	0.215 – 0.230	0.130 – 0.088
Combined standard uncertainty		
$u(Q_{Inj})$	11.67 – 1.315	0.368 – 0.095
Goodness of statistical fit		
χ^2_ν	0.342 – 0.008	2.084 – 1319
Scaled combined standard uncertainty		
$u_s(Q_{Inj})/Q_{Inj} = \sqrt{\chi^2_\nu} \cdot u(Q_{Inj})/Q_{Inj}$	6.820 – 0.118	0.532 – 3.446

Two Q_{Inj} ranges

Negligible

Mostly dominates

Incomplete model for high Q_{inj}

Open-Access paper on IEEE TIM

https://ieeexplore.ieee.org/abstract/document/11270954

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Metrological Assessment and Simulation of Charge Injection Phenomena in CMOS Electronic Switches

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For further info contact the authors →

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