22RPT02 EPM True8DIGIT

Welcome to

Towards a true 8-digit digitiser

NEWSLETTER issue 4 (May 2026)

web version

Bottom-up development and research underpinning the design of a digitiser with state-of-the-art performance.

Introduction

Welcome to the fourth and final True8DIGIT project newsletter. Here you can read about some notable outcomes of the project. Each work package has produced results of interest:

- An efficient method to supress the harmonics of DAC-based sinewave sources, rendering them suitable for testing ADCs. Additionally, an efficient method to supress the harmonics of ADC channel based on a clean programmable ultra-pure sine wave source.
- An alternative approach to characterising ADCs using a multi-tone signal.
- A method to measure the distortion of resistors and capacitors at the 170 dB level.
- A power supply with continuous output, low noise and high isolation.
- An ultra-low jitter timing platform to provide trigger and synchronisation signal.

Fuller accounts of these and other project outcomes may be accessed on the project's website where you will find detailed reports and a full list of related publications.

Project Workshop

A project workshop with more than 40 participants (in-person and on-line) was hosted by the Instituto Português da Qualidade (IPQ) on 15 May 2026.

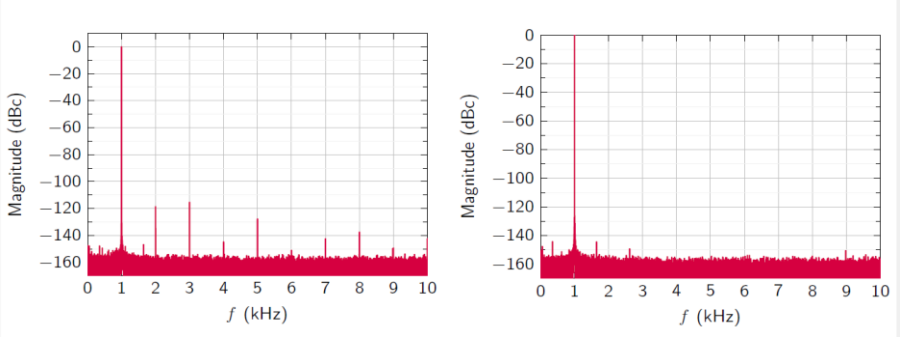
Time	Title	Presenter
10:00 hrs	The True8DIGIT project – objectives, work programme and outputs	Oliver Power, NSAI
10:20 hrs	Precision ADCs – current state-of-the art	Nikolai Beev, CERN and STU
10:40 hrs	A bridge for measuring distortion of components at the 170 dB level	Rado Lapuh, Left Right s.p.
11:20 hrs	Coffee Break	
11:40 hrs	Characterisation of components for use in precision integrating ADCs	Vitor Cabral, IPQ
12:00 hrs	Measurement of charge injection of electronic Switches	Paolo Durandetto, INRIM
12:20 hrs	Design, fabrication and testing of an ultra-clean power supply with continuous output	Jan Kucera, CMI
12:40 hrs	Lunch	
13:30 hrs	Ultra-low jitter timing platform for high-precision composite ADCs	Ricardo Iuzzulino, INTI
13:40	Ultra-low distortion sinewaves for ADC testing	Rado Lapuh, Left Right s.p.
14:00	Recent improvements in multi-tone testing of ADCs	R. A Belcher, Signal Conversion Ltd.
14:20	Discussion Forum	
15:00	Close of Workshop	

Presentations including some practical demonstrations of the main project outcomes were made. Copies of the presentations are available on the project's web page.

Some Project Outcomes

Ultra Low Distortion Sine Waves from Digital to Analog Converters[1]

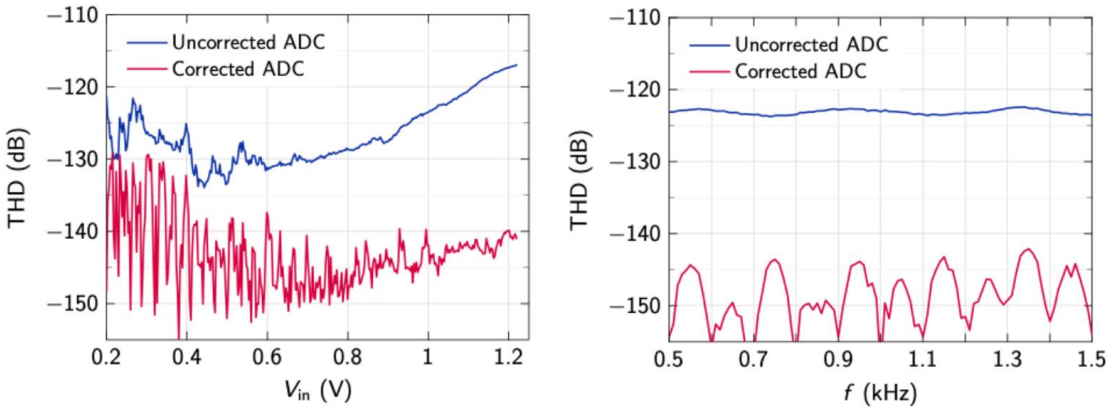
There is a growing need for spectrally pure sinewaves both in metrology and for testing Analog to Digital Converters (ADC) with resolution in excess of 20 bit. Analog generators have traditionally dominated the lowest distortion end, but an increasing number of applications demand the ability to synchronize the signal generator to the digitizer used in the measurement. Digital generators for the audio frequency range have also been developed with harmonics at or below −140 dBc but are only available as part of a complex system designed for testing integrated circuits. To achieve harmonic suppression beyond the native linearity of a typical DAC-based generator, a closed-loop digital pre-distortion routine has been implemented using a custom Python-based automation framework.



Spectra showing harmonic content of DAC source before and after harmonic suppression

Ultra Low distortion Sine Wave Sampling with Analog to Digital Converters[2]

Building on our work in ultra low distortion digital sinewave generation, we are also developing techniques for ultra low distortion sinewave sampling using high-resolution Analog-to-Digital Converters (ADCs). While modern ADCs provide excellent nominal linearity and dynamic range, achieving reliable harmonic measurements below −140 dBc remains challenging due to residual distortion originating from the sampling front-end, clocking system, reference circuitry, and signal processing chain. Traditional approaches rely heavily on carefully optimized analog hardware, but increasing demands for traceable and repeatable measurements require advanced digital correction and synchronization techniques. To extend the achievable spectral purity beyond the intrinsic limitations of the acquisition system, a closed-loop calibration and digital compensation framework has been developed using a custom Python-based automation environment, enabling ultra low distortion sinewave sampling and characterization in the audio frequency range.



An ultra clean DC power supply for precision digitisers[3]

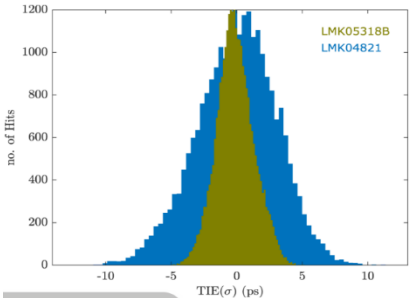
A continuous isolated power supply unit has been designed, and its first demonstrator was developed. The design is based on automated switching of battery cell banks, ensuring continuous operation of the output power rails, providing voltages from ±5 V up to ±18 V. A dedicated system of switching relays was designed to ensure low leakage between banks in both charging and loading mode. The picture shows the testing of the power supply's stability, temperature sensitivity and load regulation.

Characterisation of key components for integrating ADCs[4,5]

In order to properly model the performance of an integrating ADCs the parameters of its key components (resistors, capacitors and switches) need to be known with high accuracy. Sound metrological testing procedures were developed to characterise the components for temperature and humidity sensitivity of the highest quality resistors and capacitors, dielectric absorption of capacitors and charge injection for electronic switches.

Ultra-Low Jitter Timing Platform for High-Precision ADC Architectures[6]

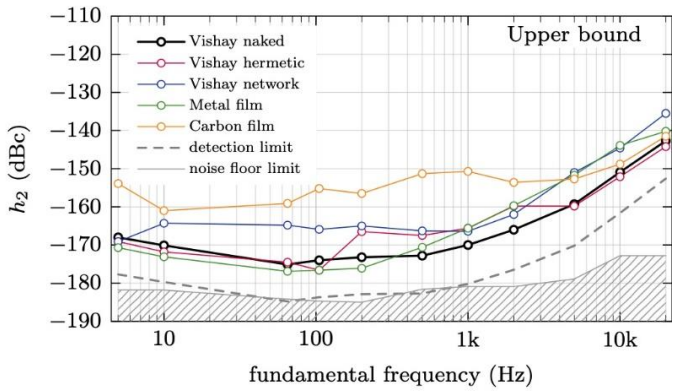
Clock jitter affects ADC performance directly by degrading the total signal-to-noise ratio. A novel ultra-low jitter timing platform for high-resolution and precision composite ADC architectures with galvanically isolated external reference clock and internal clocks and trigger outputs. The platform allows the synchronization of different kind of ADCs (SAR, IADC and Σ-Δ ADC) to run in parallel or interleaving mode in order to increase the effective vertical resolution of the composite architecture and to improve the signal-to-noise ratio.



The figure shows the measured jitter level which is at the picosecond level.

Characterisation of Resistor and Capacitor Non-linearity below 160 dB level[7]

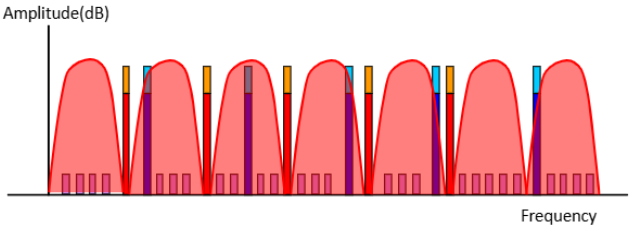
The accurate measurement of the non-linearity of resistors and capacitors is crucial for designing high-precision analogue circuits and instrumentation systems. A modified Wheatstone bridge topology designed to simplify the balancing and improve harmonic sensitivity and measurement accuracy was developed.



The technique offers a robust, sensitive, and simplified method for quantifying the component's non-linearity down to −170 dBc with a single grounded source and no special guarding techniques. A full uncertainty analysis of the results was performed.

Improved multi-tone testing method for ADCs[8]

Multi-tone testing of ADCs offers several advantages over single tone tests and offer a better representation of ADC's response to "real world" waveforms and signals.



Moving beyond standard testing, our research successfully addressed and resolved critical aliasing problems inherent to multi-tone methods. It demonstrated how a standard 14 bit arbitrary waveform generators can be used to test a 24 bit 2 MHz ADC and associated composite operational amplifier. For further details see the presentation on this topic given at the project's final workshop (available on the project website).

Dissemination

(1) *Ultra Low Distortion Sine Waves from Digital to Analog Converters,* Luis Palafox, Rado Lapuh, accepted for presentation at CPEM 2026, Sep 2026, Madrid

(2) *Ultra Low Distortion Sine Wave Sampling*, Rado Lapuh, Luis Palafox, accepted for presentation at CPEM 2026, Sep 2026, Madrid

(3) *Development of Silent, Galvanically Isolated Power Supply for Precision Metrology Applications,* Jan Kucera et al., accepted for presentation at CPEM 2026, Sep 2026, Madrid

(4) *Characterization of Passive Components for Use in a Precision Integrating Analogue-To-Digital Converter,* V. Cabral et al. IMEKO TC4 Workshop at a Special Session at XVI Semetro, 1-4 December 2025, Maceió - Alagoas, Brazil

(5) *Metrological Assessment and Simulation of Charge Injection Phenomena in CMOS Electronic Switches*, B. Trinchera, P. Durandetto and R. Iuzzolino, IEEE Trans Instrum Meas, vol. 74, pp. 1-11, 2025, Art no. 1508811, doi: 10.1109/TIM.2025.3637972.

(6) *Ultra-Low Jitter Timing Platform for High-Precision ADC Architectures,* Ricardo Iuzzolino et al., accepted for presentation at CPEM 2026, Sep 2026, Madrid

(7) *A Modified Wheatstone Bridge for High-Precision Characterisation of Resistor Nonlinearity*, Vojtech Janásek et al., submitted to IEEE Trans. Instrum. Meas.

(8) *Measuring Wideband Nonlinearity of Analog to Digital Converters*, R. A. Belcher and L. Palafox, 2024 IEEE International Instrumentation and Measurement Technology Conference (I2MTC), Glasgow, United Kingdom, 2024, pp. 1-6, doi: 10.1109/I2MTC60896.2024.10560654.

Technical Deliverables

(also available from the website)

Report identifying novel metrology grade ADC architectures for the DC to 100 kHz frequency band, 22RPT02-True8DIGIT-Deliverable D1, Jan 2026.

Report on metrological methods for characterisation of resistors, capacitor and electronic switches for use in ADCs, 22RPT02-True8DIGIT-Deliverable D3, Nov 2024.

Report on the assessment of at least 2 designs for novel amplifiers (composite operational amplifiers (COPAs)), 22RPT02-True8DIGIT-Deliverable D4, Jan 2026.

Report on the development of an ultra-quiet and stable low noise power supply, 22RPT02-True8DIGIT-Deliverable D5, May 2026.

Timing and Synchronization Platform suitable for use in precision digitizers, 22RPT02-True8DIGIT-Deliverable D6, Jul 2025.

Representation on Standards Committees

The key standard relating to this research is IEC 60748-4-3. This I2MTC 2024 paper cited above[7] was submitted though IEEE standards committee TC10. The relevant IEC committee is SC47A. IEC standards committees already have members who are also IEEE members so our work may lead to update to IEC 60748-4-3 though collaboration with IEEE TC10 members and members of IMEKO TC4.

True8DIGIT Contacts

A more detailed overview of the project and a list of **Contacts Persons** can be found at the **project's website.**

If you're interested in this work or would consider contributing to any follow-on research, please contact the True8DIGIT science leader **Rado Lapuh**

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