22RPT02 EPM True8DIGIT

Welcome to

Towards a true 8-digit digitiser

NEWSLETTER issue 2 (Jan 2025)

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Bottom-up development and research underpinning the design of a digitiser featuring state-of-the-art performance.

Introduction

Welcome to the second newsletter for the True8DIGIT project. Research towards the development of a digitiser with performance beyond the state-of-the-art was planned as a two-step approach. The role of the True8DIGIT project is to prepare the groundwork for a follow-on project in which a working digitiser will be developed. Results and developments in the True8DIGIT project have been encouraging and a proposal for a follow-on project is under preparation for the 2025 Integrated European Metrology call of the European Partnership for Metrology. This newsletter highlights some of the more important results and developments achieved in the True8DIGIT project so far.

Project status

The project has reached its mid-term and is generally progressing on schedule. All expected deliverables have been submitted and accepted.

Tests identified and performed on ADCs, a sinewave source developed with further testing planned; models for the IADC have been developed, and barriers to improving IADC and SAR ADC performance have been explored. The COPA design is complete and key measurements on capacitor dielectric absorption, resistance array sensitivity to temperature and humidity, distortion analysis, electronic switch characterization, leakage current and noise levels of a DC/DC converter have been completed; two demonstrator clocks are underway, showing good jitter performance.

There is a proposal for a follow-on project, and a special session on digitisers will be held at the forthcoming IMEKO TC4 conference.

Project meetings

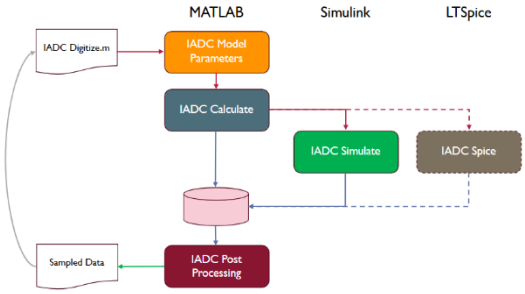
In addition to meetings between partners to discuss the development and progress of work against each work package, a hybrid mid-term meeting involving the consortium and hosted by SIQ, Ljubljana, Slovenia, was organized.

M18 Meeting
2-3 Dec 2024

- To review the work done so far
- To find workarounds for obstacles
- To plan the next stages
- To outline proposal for follow-on project
- To provide input for mid-term report

Recent developments

Comprehensive MATLAB model for studying IADC performance

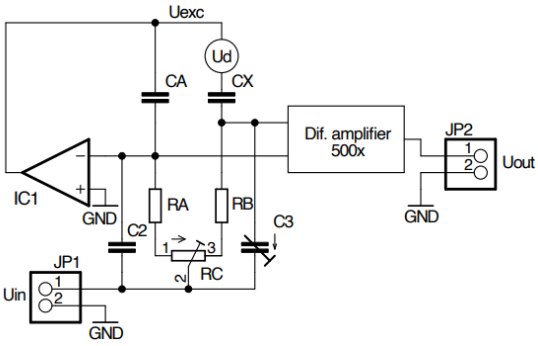


For the development of an advanced ADC design—offering beyond state-of-the-art performance and enabling a framework for a digitizer digital twin—comprehensive models and simulations are being utilized to identify key components that limit current IADC design performance. These insights help propose workarounds that can ease critical component requirements.
The implemented model, developed primarily in MATLAB with optional integration of SIMULINK and LTSpice, demonstrates a highly adaptable and comprehensive approach, making it well-suited for future design iterations.

Multi-tone method to measure broadband performance of ADCs

A new multi-tone method for measuring the wideband non-linearity of ADCs has been developed and tested. This approach, which uses two multi-frequency signals to reveal intermodulation products, offers a key advantage: it is not limited by the non-linearity of the signal generator used to produce the test signal.
The method was presented at the IEEE I2MTC 2024 conference and has been published in a peer-reviewed journal. Additionally, the IEEE TC10 standardization committee has expressed interest in its potential applications.
To validate the method, the distortion of 24-bit **Σ-Δ** ADCs within the Audio Precision APx555 Audio Analyzer was measured using both this technique and an ultra-pure sinewave source. The results demonstrated strong agreement, confirming the method's effectiveness.

Novel bridge to measure component distortions with unprecedented sensitivity



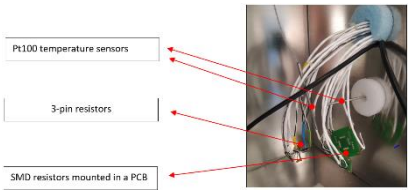
A bridge method for measuring the distortion of resistors and capacitors has been developed, featuring a key innovation: feedback OP-AMP significantly relaxes the signal generator requirements, while on board differential amplifier relaxes detector requirements and simplifies bridge operation.

This method has demonstrated the ability to measure the non-linearity of capacitors and resistors with a 2nd and 3rd harmonic distortion sensitivity below -170 dBc in frequency range between 5 Hz and 20 kHz.

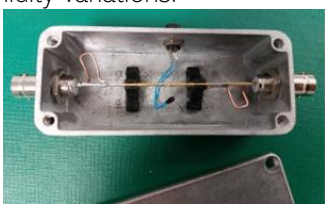
The method was presented at CPEM 2024, and a publication detailing its findings is currently in preparation.

Measurement of temperature and humidity sensitivity of components

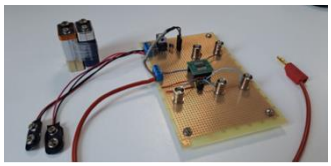
The characterization of linear components (resistors and capacitors) and electronic switches in the front-end circuitry is crucial for selecting high-quality elements essential to the overall performance of the integrator and digitizer front-end. To ensure optimal performance, these components will be analysed for non-linear behaviour, allowing for the selection of the most suitable options. Metrological methods for the measurement of the temperature and humidity coefficients and dielectric absorption of capacitors have been established and validated.



Measurements in high-precision resistance arrays revealed that resistance ratio temperature coefficients were below 0.1 ppm/K, with even lower sensitivity to humidity variations.



Capacitors dependence variations in temperature coefficients of approximately 13 ppm/°C were observed across different manufacturers. Measurements repeated for a sample of capacitors drawn from two different batches showed a spread of ±0.2 ppm/°C. Sensitivity to humidity showed a clear nonlinear dependence, where the sensitivity to humidity changes increases with the humidity level.



Electronic switches were characterised for their input and output capacitance, delay, rise-time and charge injection.

Improved designs for composite operational amplifiers

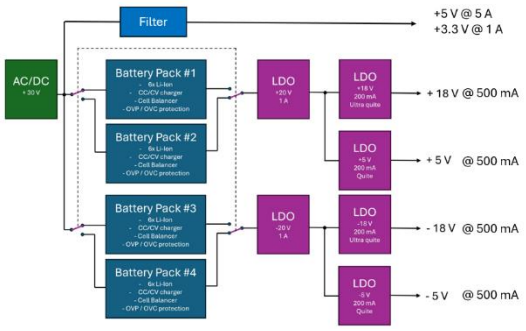
Two composite operational amplifier (COPA) designs have been developed for the input stage and integrator of an integrating ADC. Simulations were conducted to evaluate frequency response, DC output voltage swing, step response, noise, and the impact of component tolerances.

A prototype evaluation board for the input stage COPA was fabricated and extensively tested. Measurements of gain, total harmonic distortion, current and voltage noise, input impedance, and transition times indicated that most parameters met expectations. Based on the findings, improvements have been proposed, and a second iteration of the COPA will be fabricated and tested.

Design plans for ultra-quiet and low noise power supply

The voltage and power levels required for the ADCs and timing platform under development have been defined. Key performance parameters—stability, low intrinsic noise, and high isolation—have been identified as critical, with the goal of surpassing state-of-the-art performance in these areas.

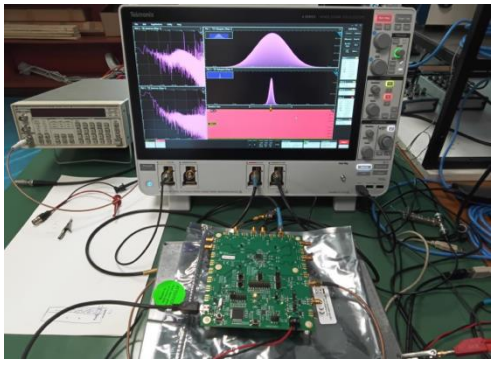
Development of the architecture concept for the power supply



Three potential architectures for an ultra-quiet, low-noise power supply were evaluated, with a battery-operated design featuring automatic switchover selected as the preferred solution for continuous operation. The necessary functional blocks and electronic components have been identified, their availability confirmed, and the optimal power and communication interfaces chosen.

Low jitter timing signals for ADCs

An analysis of novel ADC designs was conducted to identify timing limitations — such as clock, trigger, and synchronization — that impact ADC accuracy.



To characterize the timing and synchronization platform, a method was developed to measure the time jitter of the output signals from both clock demonstrators. The FPGA-based clock exhibited a measured jitter of 16 ps, while the network synchronizer-based clock achieved an even lower jitter of 1.2 ps. Both clocks successfully meet the target jitter requirement of less than 50 ps.

Divulgation

Towards a true 8-digit digitiser – EU Project overview and progress, High Performance Digitizer and DC Metrology, Feb 2024

Measuring Wideband Nonlinearity in Analog to Digital Converters, Allan Belcher and Luis Palafox, paper accepted for publication at IEEE - I2MTC May, 20-23, 2024 Glasgow.

Quadrature Bridge for Non-linearity measurement, Vojtech Janásek, Nikolai Beev, Bočtjan Voljc, Rado Lapuh, CPEM 2024, Jul 2024, Denver, Colorado

Digital Multimeters Sampling Performance Comparison, Rado Lapuh, Jan Kučera, Jakub Kováč, Bostjan Voljč, CPEM 2024, Jul 2024, Denver, Colorado

Is a digitizer with sub-ppm accuracy feasible? Rado Lapuh, Bjørnar Karlsen, Jan Kučera, Bruno Trinchera, Allan Belcher, NCSLI 2024 Workshop & Symposium, Jul 2024, Denver, Colorado

Progress Report on 22RPT02 True8DIGIT project and prospects for a follow-on project, EURAMET TC-EM 2024, Oct 2024

Representation on Standards Committees Divulgation

Following the presentation of the multi-tone method to measure broadband performance of ADCs at the IEEE I2MTC 2024, the IEEE TC10 standardization committee has expressed interest in its potential applications.

True8DIGIT Contacts

A more detailed overview of the project and a list of Contacts Persons can be found at the project's website.

If you're interested in becoming a stakeholder and directly benefiting from the project outputs or if you'd like to learn more about the work carried out in each WP, feel free to reach out to **the project coordinator or any WP leader**

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