Welcome to

Towards a true 8-digit digitiser

22RPT02 EPM True8DIGIT

NEWSLETTER issue 1 (Mar 2024)

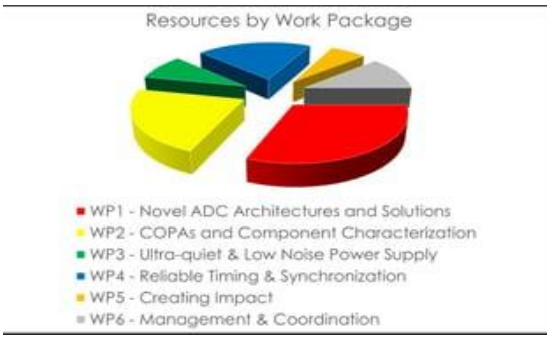
Bottom-up development and research underpinning the design of a digitiser featuring state-of-the-art performance.

Project overview

This project addresses the development of a digitiser based on state-of-the-art analogue-to-digital converters (ADCs), operating from direct current (DC) to 100 kHz, meeting the demands for linearity, noise, and overall accuracy of high-level measurement applications that cannot be met using currently available digitisers. In this project research on the key techniques and technologies needed to underpin a follow-up full-scale project will be performed.

An important aim is to provide research capacity building opportunities for developing NMIs/DIs on the design and characterisation of electronic measuring devices needed for a wide variety of interdisciplinary metrological challenges such as state-of-the-art DC measurements and advanced digital sampling techniques.

Distribution of Resources by Work Package



Work Programme

The research is divided into four technical work packages. The first deals with the design and modelling of novel analogue-to-digital converters (ADCs) The goal is to model an improved integrating ADC and an ADC which employs several successive approximation register (SAR) ADCs operating in parallel. The second work package deals with the design of improved composite operational amplifiers for use in the input stage or the digitiser and in the integrator of the IADC. Methods for the characterisation of linear components will also be addressed in this work package. In the third work package the ultra-clean, low noise power supply needed for a precision digitiser is addressed. The fourth work package aims to provide a precision timing platform for the digitiser which will minimize timing errors.

Project meetings

In addition to regular informal meetings between partners to discuss the development and progress of work relating to each work package, two formal meetings have already been held involving the consortium:

Kick-off Meeting
13-14 Jun 2023
The group had the opportunity to meet face-to-face on the occasion of kick-off meeting at the NSAI-NML facility in Dublin.

M09 Meeting
29 Feb 2024

- To review progress to date
- To provide input for M09 progress report
- To identify roadblocks or risks
- To plan for the following 9 months

Consortium

Industrial end users and stakeholders will directly benefit from the project outputs, such as advanced instrumentation with interference-free power supplies, cost effective selection of passive components for sensor/transducers and instrumentation, as well as precision isolated timing solutions for synchronised measurement systems.

The project will provide key techniques and develop technologies to improve available state-of-the-art digitiser performance.

See here the full composition of the consortium...

15 Partners | 3 Collaborators | 11 Stakeholders

Let us know if you're interested in becoming a stakeholder and directly benefit from the project outputs
Contact the project coordinator or any WP leader

Highlights so far

Although the project has only been in operation for 9 months, significant progress has been made in some areas:

- An improved bridge-based method to measure the non-linearity of passive components with a sensitivity of -160 dB. A paper has been submitted to CPEM 2024.
- A new method to measure dynamic nonlinearity below 22 effective number of bits using a multi-tone test signal. This will be presented at the I2MTC (Glasgow, 20-23 May 2024)
- Novel designs for composite operational amplifiers that could provide a path to improved performance of an integrator once fully implemented.

Representation on Standards Committees

The project is expected to generate results that will be valuable to standardisation work within IEC and IEEE. It is estimated that project members will maintain liaisons with the following committees:

- IEEE Std. 1241, TC10
- IEC 60748-4-3, TC47 SC47A
- IEC TC85 WG22

Recent developments

Work package 1
Novel Architectures and Solutions for the ADCs

Simulations of the parallel operation of the AD4630 SAR ADC have been carried out and a prototype with 4 ADCs in parallel is presently under construction. Theoretical improvements were predicted to be later compared with measurements.

Work package 2
Novel Composite Operational Amplifiers and Key Component Characterisation

Two COPA designs have been prepared and the evaluation boards are under construction. Some simulations have been carried out. The characterisation methods of the COPAs have been established.
The characterisation methods for measurement of the temperature coefficient, dielectric constant and distortion of capacitors have been established and tested. A novel bridge-based method for measuring the distortion of capacitors and resistors with a sensitivity of –160 dB has been developed by a collaborator. A paper describing the work has been submitted to CPEM 2024.

Work package 3
Ultra-Quiet and Low Noise Power Supply

The task of specifying the output levels and specifications of the power supply has proved challenging due to the on-going development of the circuits that the power supply must drive. Nevertheless, preliminary specification has been prepared. Three architectures have been examined, one using a battery switching method, the other two based on DC-DC converters. The use of super capacitors rather than conventional batteries is being investigated.

Work package 4
Reliable Timing and Synchronisation Methods for Novel ADC Architectures

The timing platform is intended to supply timing signals for the novel ADC architectures under development in WP1. Timing limitations (clock, trigger, synchronisation) that affect ADC performance have been identified, Three possible timing solutions have been proposed and one has been chosen for development A block diagram has been prepared, the necessary hardware acquired, and the timing platform is under construction.

Do you want to know more about the work carried out in each WP?
Address your question to the correspondent WP coordinator

Recent publications

Measuring Wideband Nonlinearity in Analog to Digital Converters, Allan Belcher and Luis Palafox, paper accepted for publication at IEEE - I2MTC May, 20-23, 2024 Glasgow.

True8DIGIT Contacts

A more detailed overview of the project and a list of Contacts Persons can be found at the project's website.

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