



Progress Report

22RPT02 – True8DIGIT Towards a true 8-digit digitiser

Robert Walsh (NSAI) 05 Jun 2025







Outline

Introduction to True8DIGIT project

Activity Overview

Some results to date







A two-step approach

Step 1 (Preparatory Research)

EPM Research Potential Project (22RPT02)

True8DIGIT "Towards a true 8 digit digitizer" Jun 2023- Jun 2026

Step 2 (Implementation)

EPM Follow-on Project

Next-generation digitiser for scientific and technological frontiers

IEM Call 2025



Industry Call 2026





Comparison of ADC performance

METROLOGY

PARTNERSHIP

EURAMET





Graphic Courtesy of Nikolai Beev (CERN)





An improved integrator for the IADC

- 3458A Integrator analysed
- New improved integrator design proposed
- Modelling predicts improved performance (against Keysight 3458A integrator)
- New integrator built and under test
- Selection of switches with low charge injection is vital







Simulation of Parallel ADC Operation

Parallel ADC operation simulated



Measurements are underway









Bridge for non-linearity/distortion measurement of components down to -170 dBc







Temperature & Resistance Sensitivities of Resistor Arrays

 \Box 10 k Ω /10k Ω Foil Resistor Arrays

□ Plastic packaging & hermetically sealed

Relative TempCos: -0.05 to +0.14 K⁻¹

Slight humidity effect for plastic packages













Measurement of the dielectric absorption of capacitors







Recovery voltage for 470pF ceramic CG0 Capacitors 5 samples from two different manufacturers



Component Nr.	R _i (ΤΩ)	C _i (pF)
1	82.5	1.780
2	255.0	2.410
3	25.6	1.620
4	18.1	0.571
5	16.1	0.031







Traceable Measurement of Charge Injection in CMOS Switches





- □ Measurement Resolution $\approx 1 \text{ pC}$
- □ Type A Std. Uncertainty: 10 70 fC
- □ Temperature Dependence: 3%-6% (15 40°C)





A comprehensive IADC model simulator

- capacitor voltage dependence and dielectric absorption
- resistor voltage dependence and self heating
- switch charge injection and time jitter
- COPA imperfections
- and more









Proposed Timing Platform







10 MHz and 100 MHz Synchronization Signals

Galvanically Isolated

Ultra-low jitter (< 5 ps)

Traceable measurement of jitter, delay and stability



Ultra-low Noise Power Supply



Switched battery based



DC-DC converter based

Very high mains isolation Isolation > 20 GΩ, < 12 pF AC CMI < 5 nA









Dynamic measurement of ADC non-linearity

Sine sources with ultra-low THD are used to test and characterise digitiser non-linearity

Multi-tone testing successfully performed on Audio Precision APx555 (24 bit DAC)



See Belcher R.A. et al. 12MTC 2024 Conference Proceedings



Conclusion



With our current research we are exploring possible areas of improvement, underpinning a successor project to design and test a real digitizer with sub-ppm performance.



Collaborators: Janascard, Metron Design, Jaromir Sukuba

- Stakeholders and collaborators are welcome to join the current project
- We plan to submit a proposal for a follow-on project for IND 2026 Call





Questions?

Contacts:

Oliver Power <u>oliver.power@nsai.ie</u> (Project co-ordinator)

Rado Lapuh <a>rado.Lapuh@gmail.com (Science leader)

Project website

https://true8digit.eu/

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