22RPT02 True8DIGIT

Deliverable D6:

Report on the development of a precision (< 50 ps jitter) timing solution for the ADC architectures with a galvanically isolated external trigger, lock-in and internal clock frequency output. This includes the development of the metrological tools to evaluate its performance and a comprehensive report on the jitter and synchronisation performance achieved.

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1. Summary

The present document deals with the development and investigation of key components identified for the setting up of a precision, galvanically isolated trigger and lock-in clock synchronization timing solution for digitizers architectures developed within the project such as those based on Integrating ADCs (IADC), Successive Approximation Register ADCs(SAR) and Sigma-Delta ADCs (Σ–Δ). These digitizers are intended to have state-of-the-art capabilities in their class in the frequency range from DC to 100 kHz.

The content of the report is as follows:

In chapter 2, the general concept of a galvanically isolated, unified clock synchronization and triggering system suitable to host several digitizer architectures is presented. The proposed timing platform encompasses additional features which enable the characterization of digitizers with parallel ADC structure and identification of the digitizer transfer function by using ultra-pure sine wave excitation at different frequencies. A demonstrator timing platform, designed and set up within the project, using commercial components and evaluation boards with lock-in capability to an external reference signal and suitable for delivering multiple clock signals is described. Furthermore, a set of galvanically isolated solutions has been identified and tested using the demonstrator clock hardware, verifying that the overall jitter noise remains far below the project target of less than 50 ps.

Chapter 3 focuses on methods for traceable time delay measurement techniques needed to characterise time delay and stability of the demonstrator clock hardware developed within the project and between galvanically isolated systems.

In chapter 4, a method for a traceable time jitter measurement needed to characterise time jitter below 50 ps for non-isolated and isolated clock/trigger signals on the demonstrator clock hardware is presented.

In chapter 5, a method for traceable measurements of clock stability is presented.

Finaly, chapter 6 reports on the measurement results of clock stability, time delays and time jitter on the demonstrator clock hardware set up within the project.

2. Development and architecture concept for ADC timing solution

2.1. Introduction

The identification, design, and development of a galvanically isolated, unified clock synchronization and triggering system for digitizer architectures based on IADC, SAR, and Σ-Δ ADCs - with time jitter performance below 50 ps, pose significant challenges, especially as these ADC architectures aim to overcome the limitations of current state-of-the-art digitizers. Accurate and stable digital clock and trigger signals are essential to operate the ADCs under optimal conditions. As the digitizer's bandwidth increases and its vertical resolution approaches higher bit depths, ultra-precise clock and trigger alignment, along with extremely low intrinsic noise, become critical to maintain the expected performance.

2.2. Unified timing solution for ADCs architectures

Available high-precision digitizer solutions explored within the project, could implement different routes for synchronisation their internal clock to external time events, depending on the internal architecture, as follows:

i) Integration ADC converters (I-ADC), e.g. DMM 3458A (HP/Keysight), through suitable programming, use *Trig In* and *Trig Out* signals to provide synchronization to external time events.

ii) Delta-sigma ADC converters (Σ-Δ), e.g. NI-PXIe 5922, uses *Clock In* and *Trig In* input signals to provide full synchronization to external time reference signals.

iii) Successive-approximation converters (SAR ADC), e.g. AD4630/AD4030, use an external clock for their self-synchronization accompanied with trigger stimuli.

The developed timing platform should cater for the operation of a digitizer with a parallel ADC structure and provide the necessary timing signals for the testing of ADCs using ultra-pure sinewave excitation. The concept shall therefore provide for both:

a) four trigger channels (for AD4030-24 SAR ADCs), which can trigger simultaneously or in series in a continuous circling manner (1-2-3-4-1-2-3-4- …). External synchronisation with 10 MHz or 100 MHz clock shall be provided and 10 MHz and 100 MHz clock output as well. Sampling times shall span from (say) 10 ms to 500 ns (200 ns for circling option), with a usable setting resolution (3458A has a 100 ns resolution, but this is not mandatory).

b) one trigger channel shall be provided (for various digitiser platforms) with sampling times from 10 ms to 500 ns, with setting resolution at the 100 ns level. Clock output for 10 MHz and 100 MHz shall be provided for pure sinewave source synchronisation.

As these triggers are originating from within the clock circuit, they can be treated as INTERNAL triggers. We shall also provide the means for EXTERNAL triggers, but this can be dealt with in a later stage.

Further, identification of clock, trigger and synchronisation limitations that affect the digitiser’s metrological performance such as noise and time delay (phase) shall be deduced with mathematical relationships where available.

2.3. Clock synchronization and triggering concept for novel ADC architectures

A general concept to ensure suitable clock and trigger signals for ADC architecture converters is reported in Figure 2-1. It has been designed taking into account the relation of this activity with the activities in the other parts of the project.

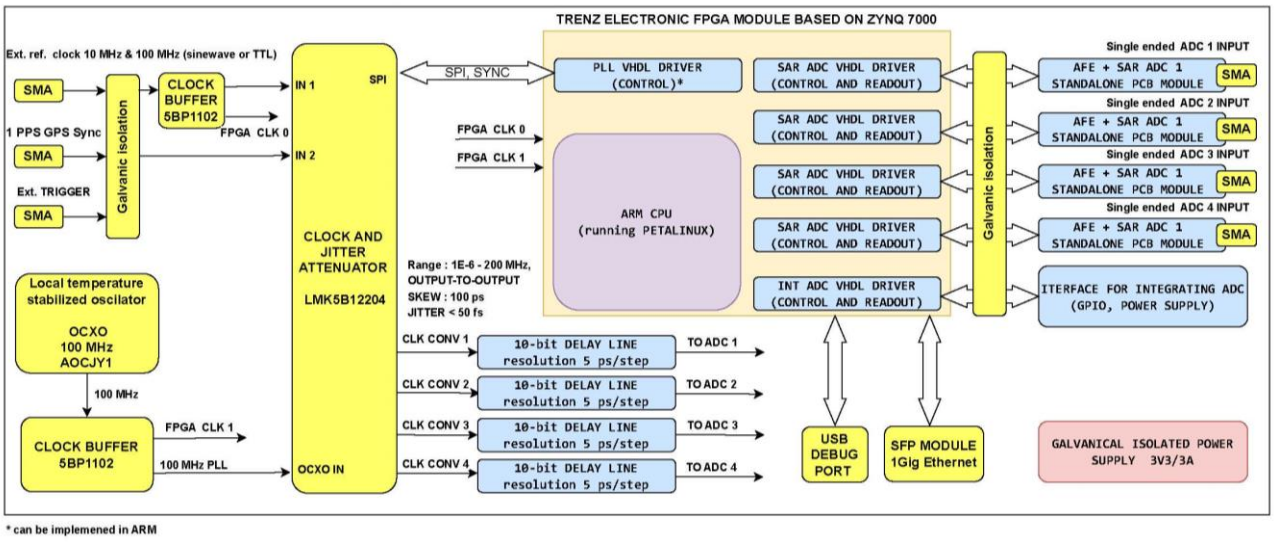

Figure 2-1. General concept of the unified timing platform for the next generation of ADC architectures.

The timing platform can be configured to be frequency locked to an external signal from 10 MHz to 100 MHz coming from atomic clocks or other synchronization platforms available in a laboratory.

Additional external trigger signals might be necessary if the platform is used to drive parallel ADC architectures.

Additional clock and trigger external signals are required for testing of the ADC architectures using ultra-pure signal sources or multi-tone signals. In this case the timing platform will be able to deliver the necessary timing signals to synchronize the external signal sources to the ADC platforms under test.

2.4. Block diagram for clock synchronization and triggering - Practical implementation

Starting from the availability of commercial off-the-shelf electronic components and/or boards/equipment, three possible solutions for practical implementation of the concept were identified. The proposed set-ups are described in sections 2.4.1, 2.4.2 and 2.4.3 below.

Each solution presents different manufacturing costs and construction complexity to fulfil the project objectives in terms of flexibility and programmability to be readily adapted to simple and complex ADC architectures and jitter performance.

2.4.1. Triggering and synchronization solutions using fractional DPLL

In this concept two banks of Digital Phase Locked Loops (DPLL), are used. The idea is to use one bank to deliver clock signals to ADC boards and a second bank to deliver trigger signals, Figure 2-2. Both DPLL banks are running synchronously with a reference external clock (optically isolated). To program and control the

DPLL a FPGA or microcontroller (µC) can be used as a control unit, which can be connected to a PC for setting.

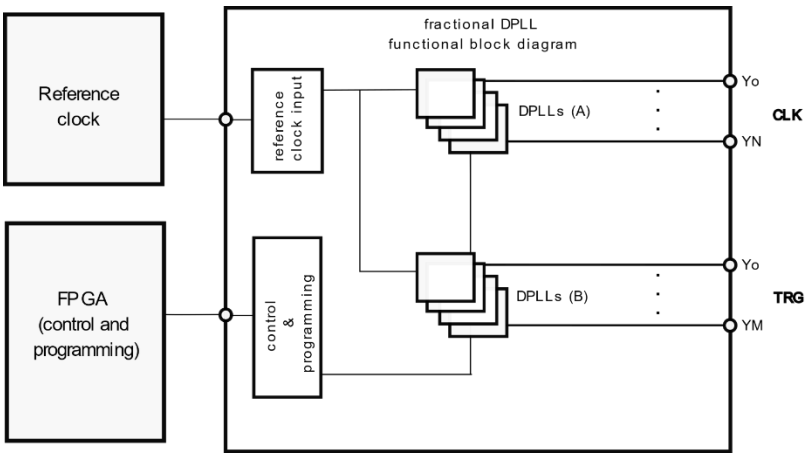

Figure 2-2. Basic solution using two banks of DPLLs, bank A for clock and bank B for trigger.

A second possibility is to use a DPLL bank to provide clocks signals, Figure 2-3. The triggers are from the FPGA, which is controlling and programming the DPLL to the desired clock frequency.

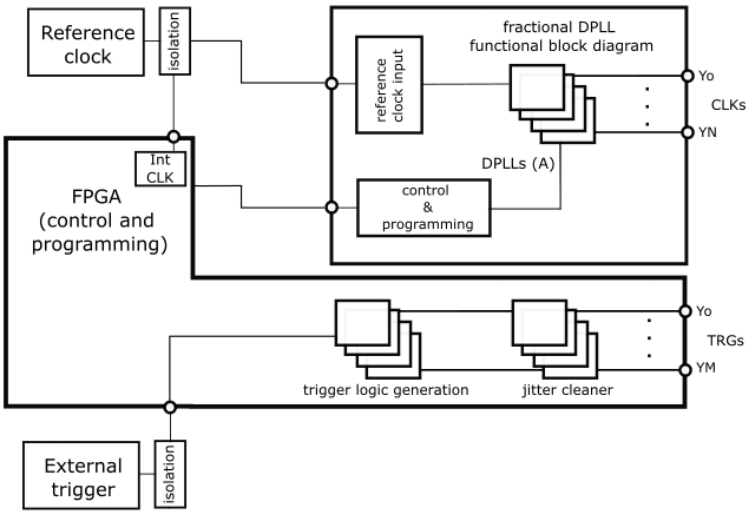

Figure 2-3. DPLL bank for clock and FPGA for trigger.

The most suitable concept might be that proposed in Figure 2-4, which differs mainly from the previous one in that it considers also the control and readout signals needed to get a continuous data stream from the ADC architecture. For this implementation a set of suitable drivers must be developed for handling a single SAR ADC or for multiple SAR ADCs used in the ADC parallel architecture.

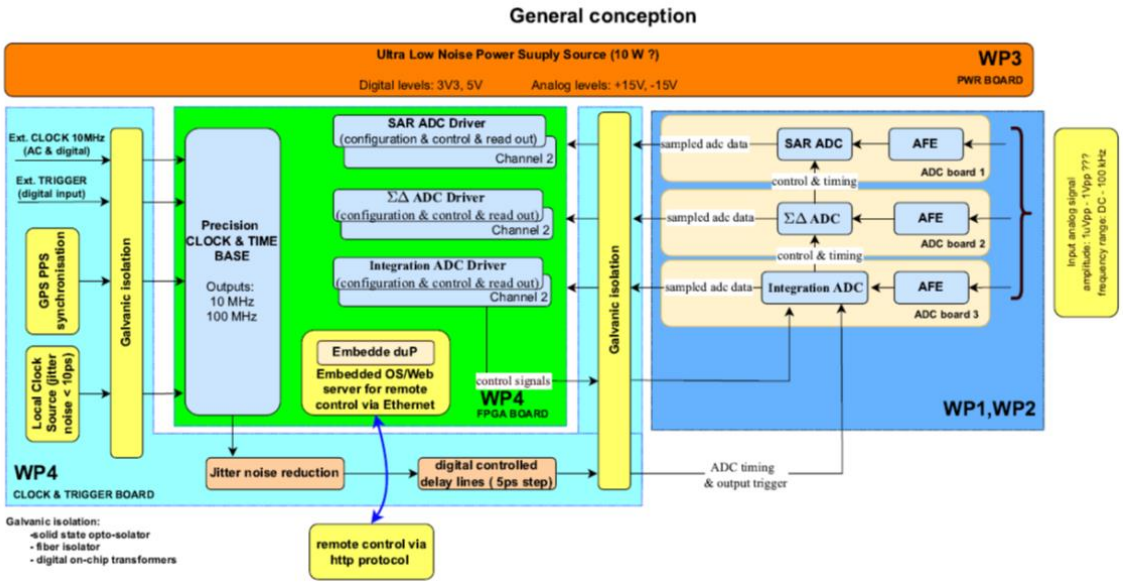

Figure 2-4. General concept with ADC timing (clock and trigger) and readout signals.

2.4.2. Time solutions based on FPGA with dedicated IP timing core

The second concept provides the ADC triggering and synchronization signals using an FPGA. The development and performance testing of the method was carried out at the Laboratory of Measurement and Signal Processing of the University of UniSannio.

Figure 2-5 shows a photograph of the implemented pulse generator board using a Xilinx KC705 FPGA evaluation board.

In particular, the reference signal (10 MHz) is connected to an input clock channel of the FPGA board and the pulse signal is generated by FPGA on an output GPIO channel of the board. By using the PLL module of the FPGA, the pulse signal is synchronized with the reference provided by a signal generator. The user can set the pulse period, pulse duration and the position of pulse along the sine wave period by sending commands via USB to the FPGA.

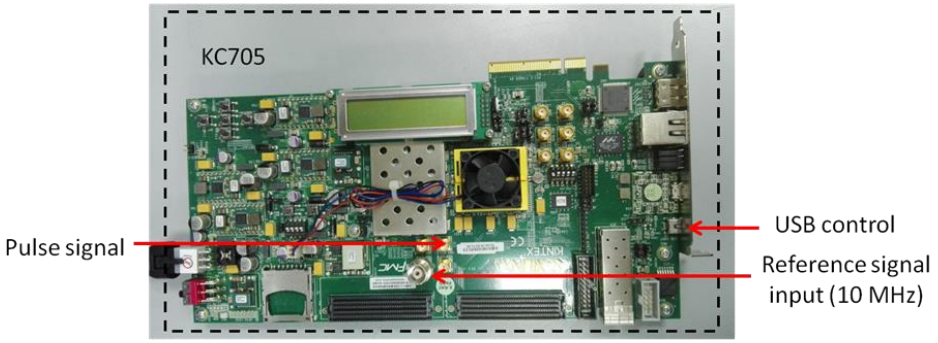

Figure 2-5. Pulse generator circuit implementation using the KC705 FPGA board.

The general architecture of the implemented pulse generator is reported in Figure 2-6. It is composed by the following logic blocks:

i) microprocessor, which configures the peripheral modules and receives the commands via USB;

ii) UART block, which enables the communication between the PC and the microprocessor via USB;

iii) pulse shaping logic, which provides the pulse signal according to a clock signal received by the clock management block;

iv) clock management sub-system, which provides a clock signal with selectable frequency synchronized with the reference clock signal (10 MHz).

The user can manage the pulse shaping logic by selecting the pulse train period and the pulse delay. The pulse duration can be selected by changing the frequency of the Clk signal. The clock management block consists of a PLL that provides a clock signal (Clk) synchronized with the signal provided by the sine wave generator under test (Ref clock – 10 MHz). The frequency value of the Clk signal can be chosen by the user (max. 640 MHz). The pulse duration is equal to the period of the Clk signal (min. 1.56 ns).

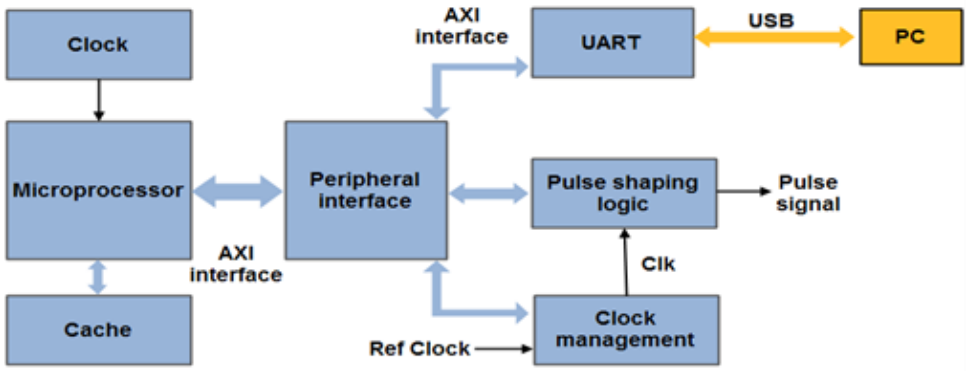

Figure 2-6. Architectural overview of the proposed pulse generator sub-system.

The architecture of the pulse shaping logic block is reported in Figure 2-7. The idea underlying this architecture is to provide a pulse, which corresponds to a changing of a state level of a port for a time defined by the Clk period, driven by a digital counter.

A 32-bit digital counter increases the value of the counting value register when a positive edge of the Clk signal occurs. The counting value is cleared when it reaches the final value imposed by the user. In this way, it is possible to change the period of the pulse signal. By using the 32-bit not XOR and the 32-bit AND, the counting value is continuously compared with a counting threshold value selected by the user. When the counting and the counting threshold values are equal, the pulse signal is generated.

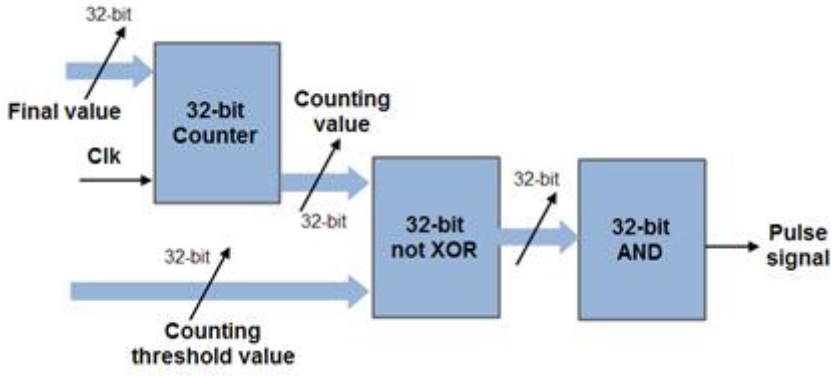

Figure 2-7. Architectural overview of the pulse shaping logic block.

In Figure 2-8, the generated pulse signal is depicted. It is possible to change the pulse signal characteristics according to the Clk period, the counting threshold value, and the final value. The period of the CLk signal defines the pulse duration, the counting threshold value imposes the instant position of the pulse along the pulse period with a time resolution equals to the pulse duration, and the final value defines the period of the pulse signal.

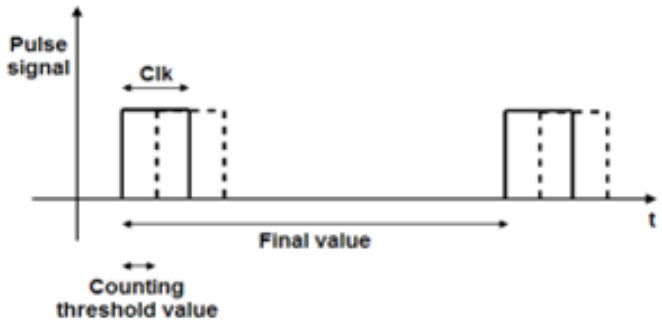

Figure 2-8. Pulse signal settings

2.4.3. Commercial-off-the-shell (COTS) for ADC time solutions

The third and last concept useful for ADC triggering and synchronisation uses commercial-off-the-shell (COTS) equipment.

There are various technological solutions on the market capable of implementing the concept. With COTS it is possible to realize a timing platform based on the modular concept, which can provide ADC synchronization and triggering using a common time-based synchronisation with 10 MHz reference signal from atomic clock, GPS, IEEE 1588, IRIG-B or PPS.

Typical jitter noise of the generated signals is about 60 ps, and an ad-hoc software development is required. Further COTS are required, such AWG generators or pulse generators, which meet the requirements of the project because they offer multiple programmable signals having jitter below the picosecond level and time delay between the signals in the picosecond range. A limitation in their use is the development of a full platform containing the necessary driver for data ADC handling. There is also the matter of their cost, which makes these solutions useful in the testing phase but impractical to be integrated into a standalone structure.

2.5. Identification of key components and evaluation boards

Identification of components and suitable evaluation boards for the fast prototyping of timing and synchronization of mixed analog/digital devices is a key challenge for the success of the project and achieving its goals.

Figure 2-9 shows a photo of the FPGA board identified during the project which is composed of essentially two parts:

i) FPGA module TE0715-04/05-21C33, based on SoC module with AMD ZYNQ™ 7012S-1C having 1 GByte DDRL3L memory;

ii) Carrier board TE0706.

Figure 2-9. Low-cost FPGA board for building the clock demonstrator.

The FPGA identified board can provide a powerful platform for demonstrating the concept of the timing platform for generating multiple clock signals in the range 10 MHz up to 100 MHz.

Figure 2-10 shows the entire board and its possibility to be expanded using the multiple connectors available on the board.

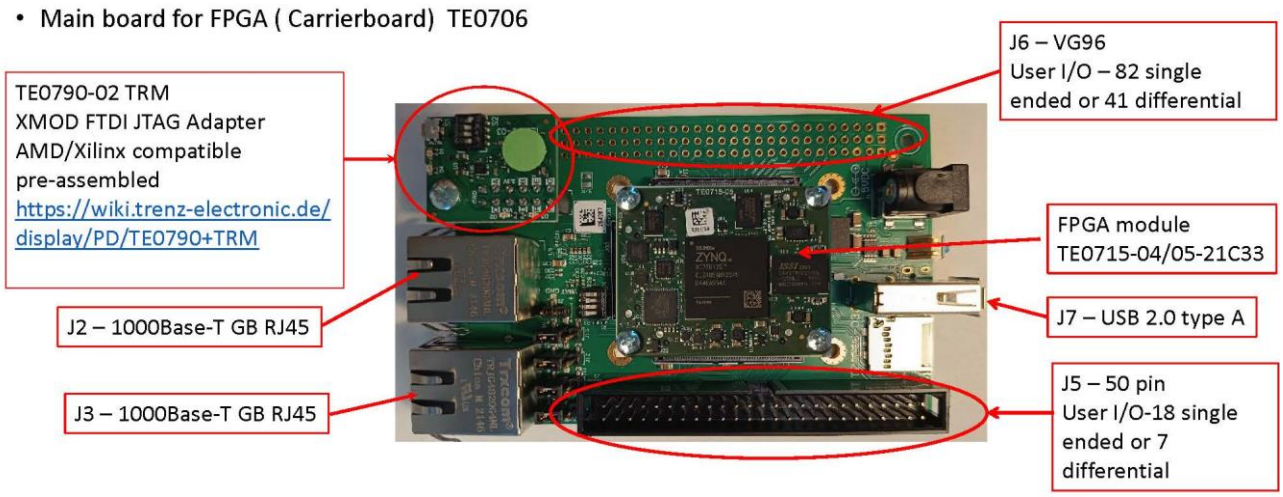

Figure 2-10. Assembled FPGA and carrier board as a single unit.

The carrier board provides two expansion connectors J5 and J6, through proper programming it is possible to deliver clock reference signals and useful signals for ADC driving.

The clock demonstrator has been designed to use the J5 connector to deliver several clock signals. A simple plug-in module has been developed for the characterization and distribution of the clock signals for other platforms, as shown in Figure 2-11.

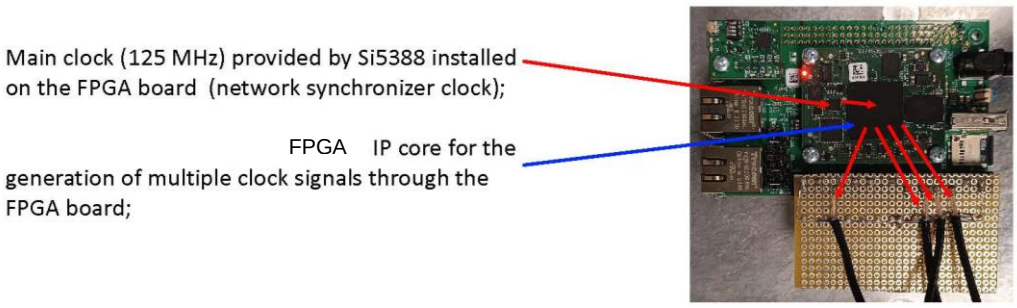

Figure 2-11. Plug-in module with coaxial cables for distribution of clock signals.

The demonstration clock platform uses the Si5388A device, which is a network synchronization clock with more than one clock. One of its clocks was programmed to deliver a primary clock of about 125 MHz and then it was distributed into the FPGA device.

A simple firmware was developed, which synthesises an additional clock inside the FPGA. In particular, the developed firmware allows for up to four clocks to be synthesized simultaneously each with a different frequency.

Figure 2-12 shows the schematic of the demonstrator clock developed for the FPGA using Vivado environment.

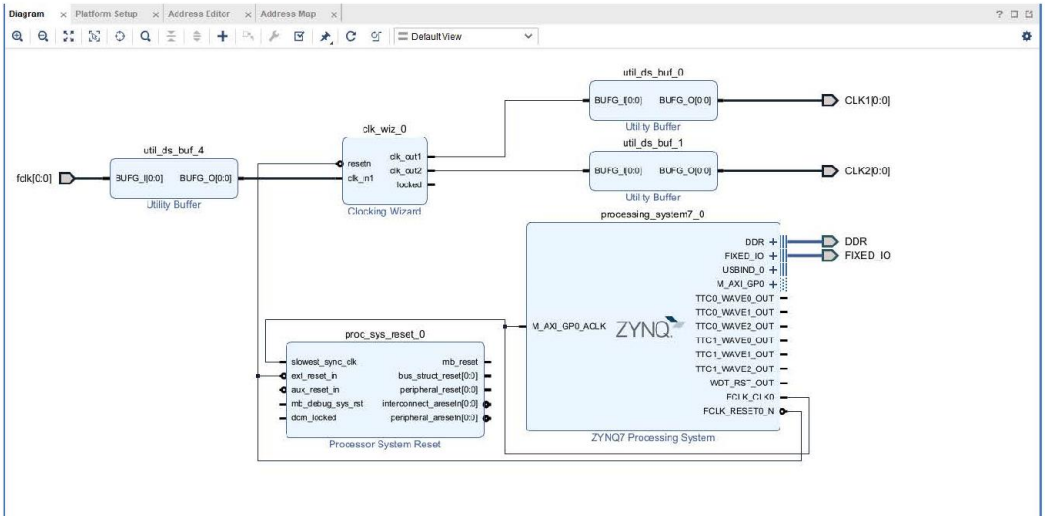

Figure 2-12. Schematic of the Vivado project for the clock demonstrator platform developed for FPGA chips.

Fully synchronized platform for clock demonstrator

One of the limitations with the FPGA platform concerns its synchronization using external clocks. In principle the platform can perform this task, but hardware modification is required.

An alternative way is to consider the use of additional devices which have the possibility to be synchronized to external clocks as reported in the section 2.4.1. For this purpose, and as specified in the general concept of the timing platform in Figure. 2.1, the evaluation board based on the LMK05318B, which is high-performance network synchronizer clock device that provide jitter cleaning, clock generation and advanced clock monitoring was chosen as a prototype for the setting up of the demonstrator clock.

Figure 2-13, shows the EVM-LMK05318B used for the setting up of the demonstrator timing platform required by the project.

The board provides up to eight clock inputs with frequencies which can be programmed from 1 Hz (1 PPS) up to 800 MHz. It provides the necessary circuitry to achieve jitter in the sub-picosecond range which meet the project requirements.

To achieve such a performance, i.e., 50 fs jitter declared by the manufacture, the device uses a proprietary Bulk Acoustic Wav (BAW) VCO technology, independent of the jitter and frequency of the XO and reference inputs. In particular, the ultra-low jitter and high power supply noise rejection (PSNR) of the device can reduce bit error rates (BER) when used in high-speed serial links or as clock source for ADCs.

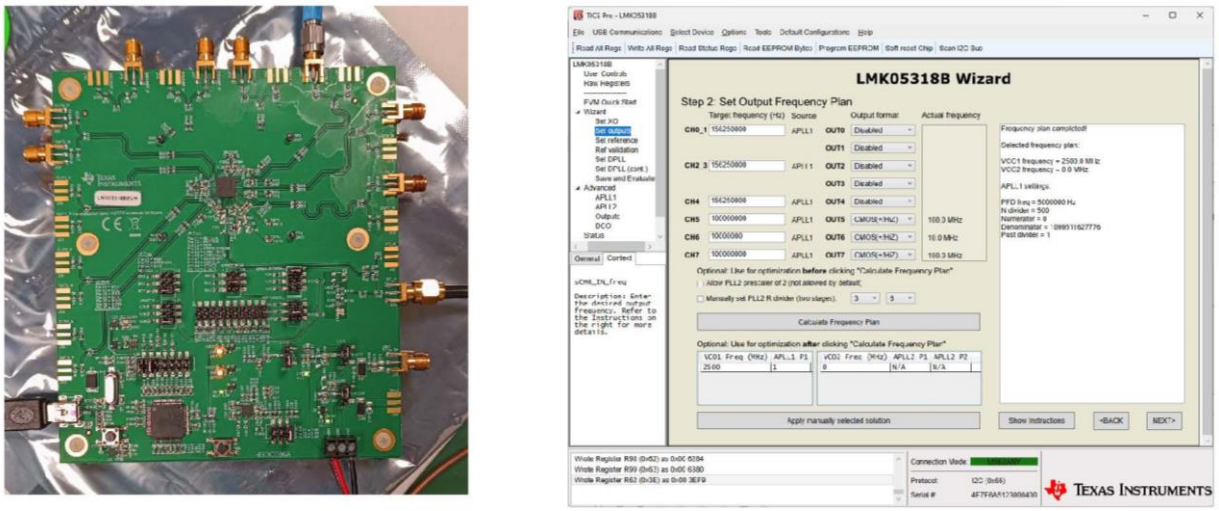

Figure 2-13. EVM-LMK05318B on the left and control software on the right provided by TI.

2.6. Setting up the clock demonstration platform

The clock demonstration platform was set up at INRiM to demonstrate the possibility of:

i) generating multiple clock signals covering the whole frequency spectrum that are needed to ensure stable operation of novel ADCs structures proposed within the project;

ii) synchronization of external equipment such as commercial pure sine-wave source for single tone or multi-tone test signals on the novel ADC architectures.

Figure 2-14 reports a simplified schematic of the clock demonstrator platform. The main components and instruments are:

- DDS Clk. Source, is a single channel reference clock source with ultra-low jitter which can be phase locked to an external reference clock;
- FPGA Clk. source, is a multi-channel clock source developed withing the project (firmware provide by INTI);
- EVM-LMK0531B, is a network clock generator and synchronizer composed as follow:
  - DPLL with programmable loop bandwidth for input jitter and wander attenuation;
  - Two Analog PLLs (APLLs) for flexible low-jitter clock generation;
  - Two clock inputs supporting hitless switching and holdover;
  - Eight differential clock outputs, or combination of differential and up to eight LVCMOS clocks;
  - On-chip EEPROM for custom start-up clocks
- HS-WB Oscilloscope (Tek. MSO64B), is a high sampling rate (50 GSa/s) wideband oscilloscope (6 GHz) with large memory and advanced jitter analysis option installed to perform several jitter and other time parameters measurements.

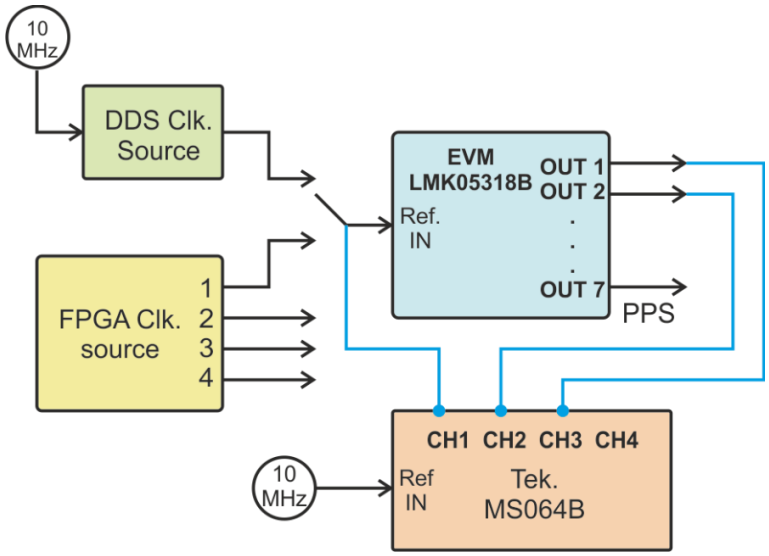

Figure 2-14. Schematic of the clock demonstrator platform.

The top-level internal block diagram of the LMK05318B device is reported in Figure 2-15.

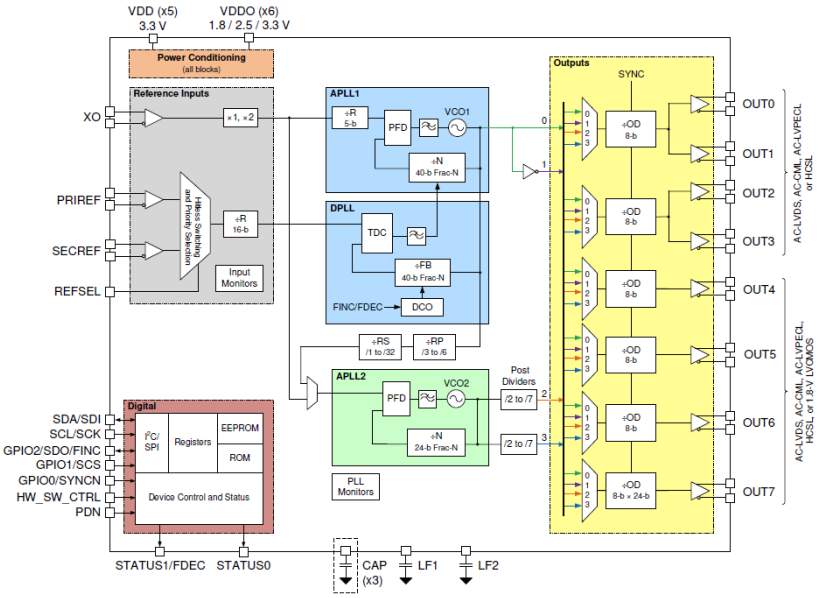

Figure 2-15. Top-level device internal block diagram of LMK05318B device.

Figure 2-16 shows the test bench of the clock demonstrator. The reference clock for EVM-LMK05318B was provided by two separate clock sources: i) a commercial DDS clock source, and ii) the FPGA multiple clock source. Both sources offer clock signals in the range from 10 MHz up to 100 MHz, with different jitter noise but both below the 50 ps target.

All the generated clock signals by the EVM-LMK05318B have jitter in the range below 10 ps, demonstrating that the jitter cleaner circuitry inside this device works well even in presence of reference input clock signals with different jitter noise levels.

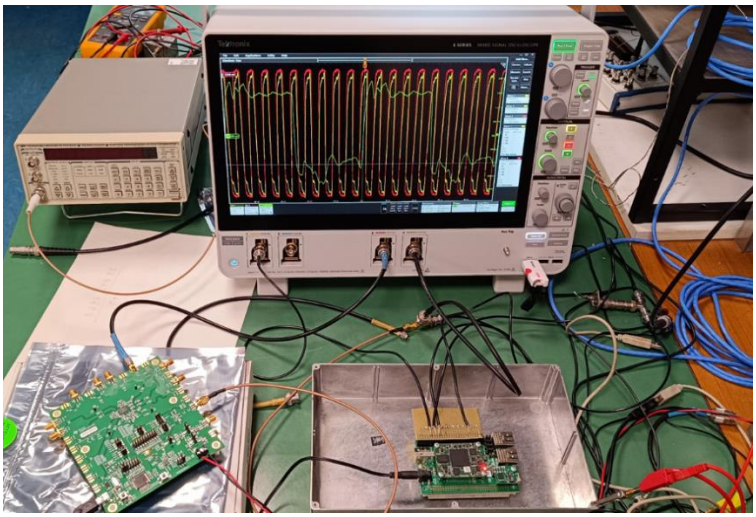

Figure 2-16. Test bench of clock demonstration platform. On the left the EVM-LMK05318B and on the right the FPGA multi-clock output board.

2.7. Galvanically isolated components and characterization

Two solutions have been proposed to provide galvanic isolation for the clock demonstration platform.

The first one is based on a true wideband optical link with bandwidth from 1 Hz up to 100 MHz, and the second uses a DC–block having bandwidth from 100 kHz up to few GHz. The aim was to introduce galvanic isolation between the system components with different bandwidths without degrading the original jitter performances.

Figure 2-17 gives a general overview of the bock diagram demonstrator clock with both input and output ports of the EVM-LMK05318B galvanically isolated.

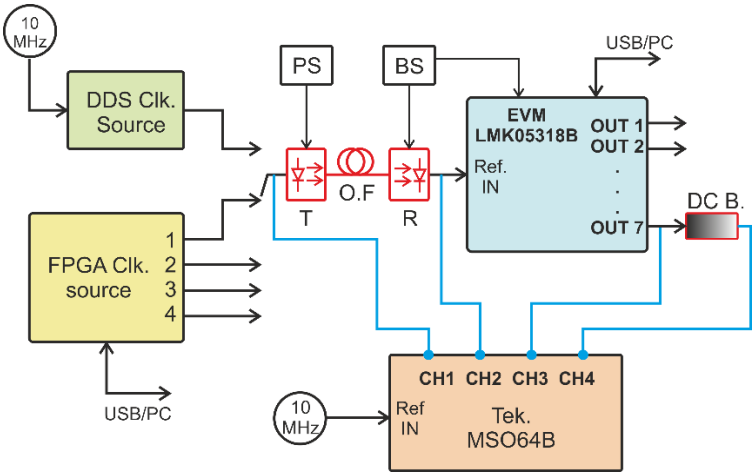

Figure 2-17. Block diagram of the test bench employed to test the galvanic isolation between the modules.

As can be shown In Figure 2-18, for the transmitter, T, the optical based galvanic isolator is connected to the output connector of the reference clock and it is supplied with a conventional bipolar DC power source, PS. The receiver, R, is connected to the input reference connector of the EVM-LMK05318B and it is supplied by a battery source, BS.

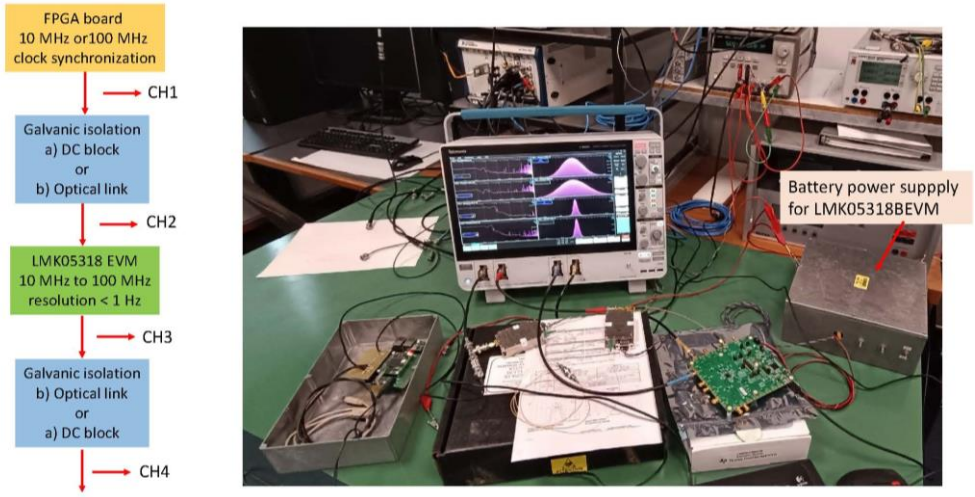

Figure 2-18. Photo of the entire clock demonstrator setup with input and output isolated galvanically.

Figure 2-19 gives further experimental details related of the insertion of galvanically isolated solutions within the demonstrator clock platform.

The two proposed solutions are reversible, and we tested that the overall jitter noise at the output of the EVM-LMK05318B board remains unchanged within the targets of the project.

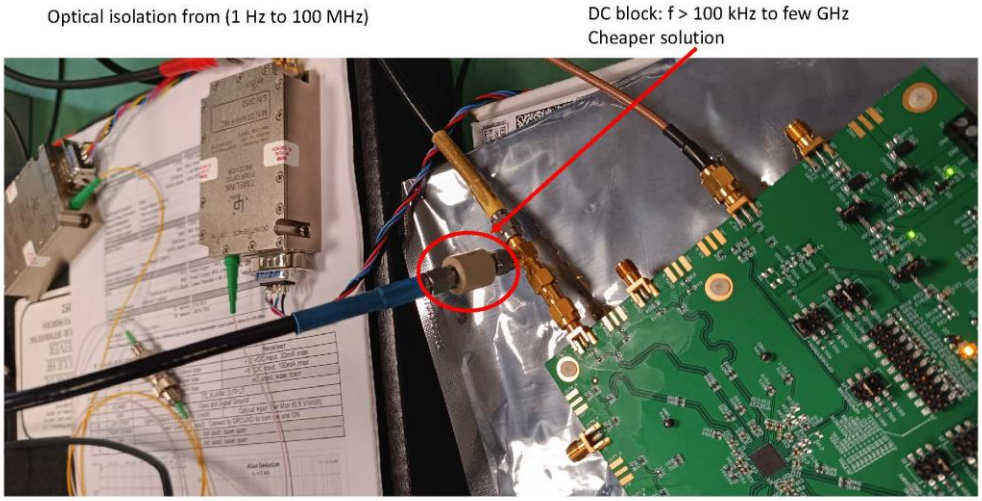

Figure 2-19. Experimental details about the insertion of the galvanically isolated solutions into the demonstrator clock platform

2.8. Identification of clock, trigger and synchronisation limitations that affect the digitiser's metrological performance such as noise and time delay (phase)

Time base errors

Time signals will define the instants at which the signal is sampled by an ADC. Therefore, drift and jitter errors in the timing signals will affect the input signal amplitude measurement made by the ADC.

The drift of a time signal is the result of the oscillator ("clock" or "time base") frequency error, and the jitter is the consequence of the oscillator frequency noise.

Time signal drift will produce a cumulative error in the sampling instant along the consecutive samples.

"Timing jitter" or "Aperture uncertainty" (other synonyms used are: "aperture jitter"; "timing phase noise") is defined in [1] as "The standard deviation of the apparent sampling time" and assumes a random nature. It will introduce an amplitude noise in the sampled signal that is proportional to the slew rate of the signal. For a sine wave signal the amplitude noise is maximum at crossing zero and is minimum at the peak amplitude of the signal [2].

The amplitude noise of a sine wave signal due to the jitter could be expressed in terms of SNR (signal to noise ratio) by the following expression [1], [2]:

$$\mathrm{SNR_j} = -20\log_{10}(2\pi f t_\mathrm{j})$$

where f is the signal frequency in Hz and t_j is the time jitter value in seconds.

From the expression above, the $\mathrm{SNR_j}$ depends on the frequency of the sampled signal. For a fixed value of t_j, the $\mathrm{SNR_j}$ value will decrease with the increase of the signal frequency. For higher frequencies the jitter becomes more critical as a source of noise error in the ADC measurements and dominates the quantization noise due to the ADC finite resolution whose SNR is given by the expression:

$$\mathrm{SNR_{bits}}=6.02\mathrm{N}+1.76$$

where N is the ADC number of bits.

The time jitter value for a particular frequency can be estimated by:

$$t_j = \frac{10^{-SNR_j/20}}{2\pi f}$$

The maximum noise, expressed as a standard deviation, to be added to a sine wave signal, measured by the ADC is given by the following expression [1], [2]:

$$\sigma_j = 2\pi A_{rms} f t_j$$

Where A_{rms} is the rms signal amplitude. The amplitude noise is considered normally distributed although this is not completely correct due to its dependence on the slew rate of the signal as referred above.

Tigger and synchronization errors

The use of trigger signals could also be used to start each sampling and to synchronize two or more ADCs.

The jitter of these trigger signals will also affect the sampled values of the measured signal. Furthermore, in applications where two or more ADCs are required to simultaneously sample different waveforms, e.g. in power, power quality and impedance measurements, the jitter of these trigger signals will also affect the phase difference measurements.

Depending on the time circuit of the ADC, these trigger signals could work together with the clock signal of the ADC (10 MHz in the case of the Keysight 3458A Digitizer [3]).

Keysight 3458A Digitizer could use an external tigger signal to trigger the sampling instant, but the effective sampling instant only occur when the next clock pulse arrives following the trigger signal. For a clock signal of 10 MHz (with a resolution of 100 ns), this delay in between the external trigger and the clock pulse could vary from 0 to 100 ns.

This justifies a maximum jitter limit of 50 ps assumed as specification (DCV mode) for the trigger signal which is significantly higher than the specification for the jitter of the clock signal with a maximum value of 100 ps [4]. Use of higher frequency clock signals will increase the time resolution and decrease this jitter error related to trigger signals.

2.9. References

[1] IEEE Std 1241-2010 IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters

[2] R. Lapuh, Sampling with 3458A

[3] Keysight 3458A Multimeter - User's Guide, Edition 9, June 2021

[4] Keysight 3458A Multimeter - Data Sheet, July 31, 2014

3. Method for traceable time delay measurements

3.1. Introduction

For a traceable time delay measurements, an experiment based on three White Rabbit LEM modules (WR) and two PLL boards was set up. One of the WR boards was configured as the Master clock and the other two as Slave A and Slave B units. All three WR modules were connected by optical fibre links. Two PLL boards were used to generate the 100 MHz clock signal from the 10 MHz output of the WR modules

3.2. Measurement Setup

Figure 3-1 shows the block diagram of the measurement setup.

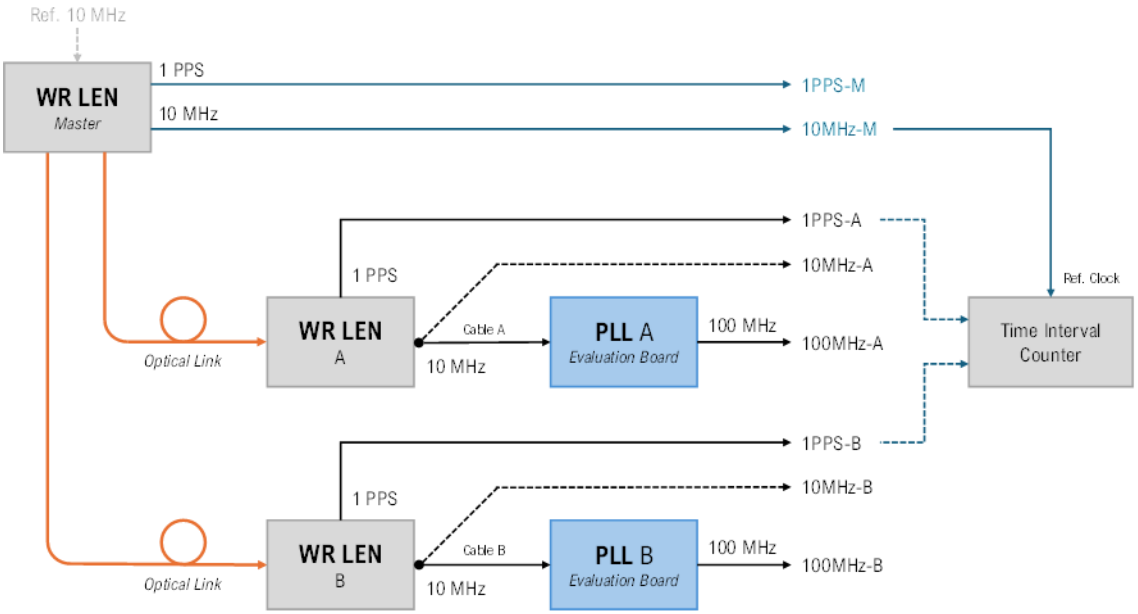

Figure 3-1. Time delay measurement setup.

In this setup three White Rabbit LEN modules were used. One is configured as master (WR-M) and two as slave WR modules (WR-A and WR-B) which were locked and calibrated to the WR-M module. Two AD9615-4 PLL boards were used to generate a 100 MHz signal from the 10 MHz output of the WR-A and WR-B modules. A SR620 Frequency/Time-Interval Counter from Stanford Research Systems was used to measure and then log the results into a PC.

Figure 3-16 at the end of this chapter shows the image of the measurement setup. In these experiments the 10 MHz clock from the Master White Rabbit Unit (WR-M) was used as the reference of the time interval counter, but the WR-M could be easily locked to a precise 10 MHz source to have a traceable 10 MHz reference.

3.3. White Rabbit Clock Synchronization

White Rabbit is a collaborative R&D project involving CERN, GSI Helmholtz Centre for Heavy Ion Research, and various academic and industrial partners. It focuses on developing a deterministic Ethernet-based network

architecture that integrates IEEE 1588 Precision Time Protocol (PTP) with Synchronous Ethernet (SyncE) to achieve sub-nanosecond time synchronization and reliable data transfer. The system is designed for applications requiring high-precision timing and deterministic communication, such as in particle accelerators, power systems, and telecommunications. White Rabbit offers extremely precise time synchronization—accurate to less than a nanosecond—using Ethernet networks instead of complex, dedicated timing systems. It can be used just to keep devices in sync, or to handle both timing and real-time data communication at the same time [1, 2]. Figures 3-2 and 3-3 show the White Rabbit LEN [3] module and its block diagram, respectively.

Figure 3-2. WR LEN module manufactured by Safran.

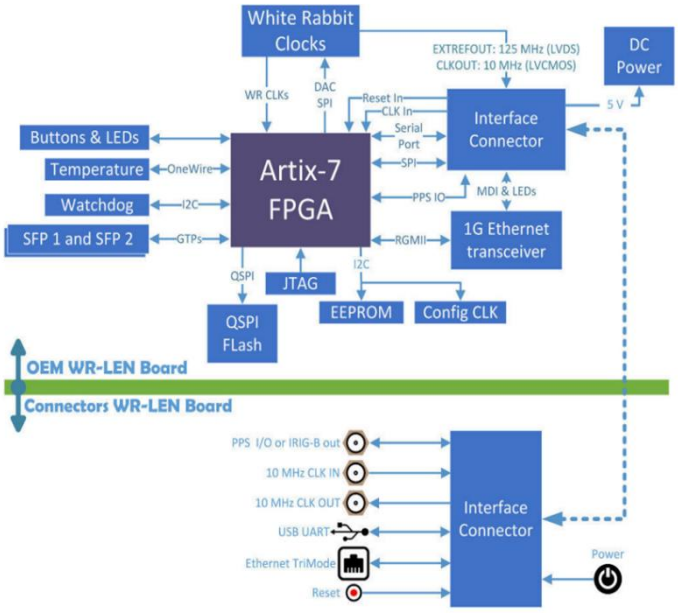

Figure 3-3. White Rabbit LEN block diagram.

Figures 3-4, 3-5 and 3-6 show the user interface (GUI) of the master unit (WR-M) and slave units (WR-A and WR-B), respectively. The master node is free running and used as the reference clock for all measurements, but it could be locked directly to any precise 10 MHz reference clock.

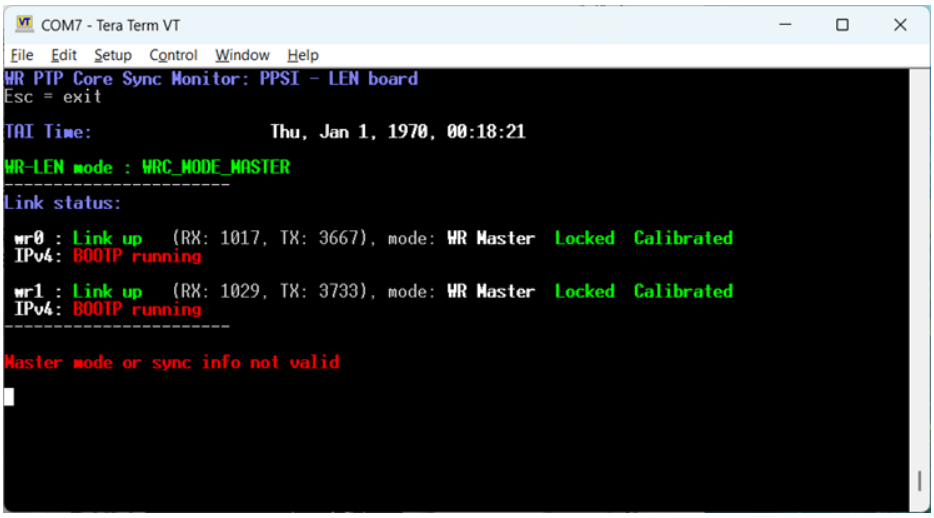

Figure 3-4 GUI of the Master White Rabbit (WR-M).

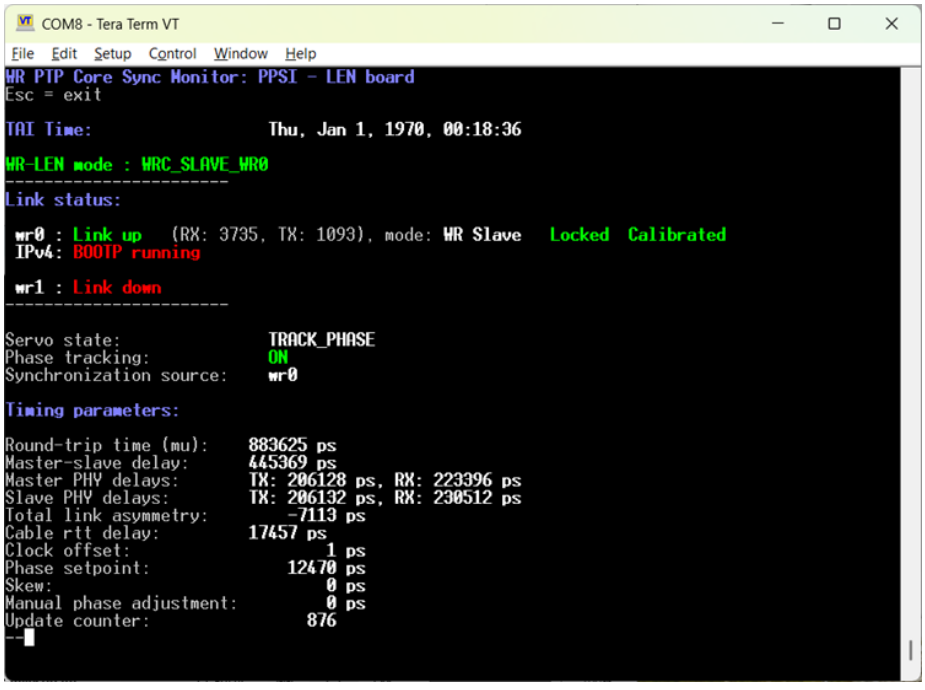

Figure 3-5. GUI of the Slave White Rabbit A.

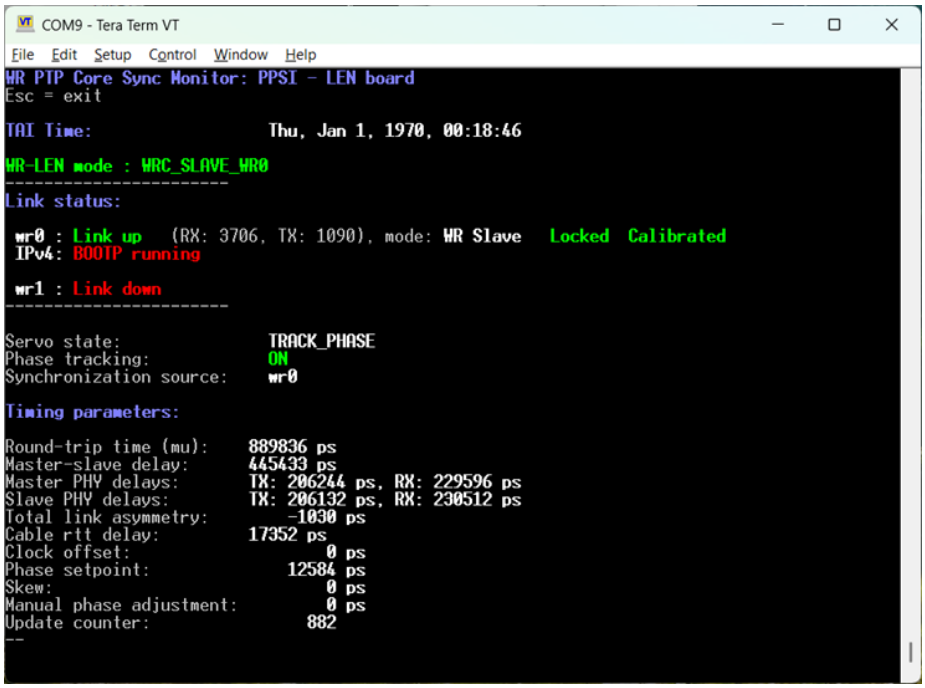

Figure 3-6. GUI of the Slave White Rabbit B.

3.4. PLL Board

In this setup a AD9516-4 PLL evaluation board [4 - 6] was used to generate the 100 MHz clock from the 10 MHz output of the WR-A and WR-B modules. Figures 3-7 and 3-8 show the PLL board and the PLL's simplified block diagram.

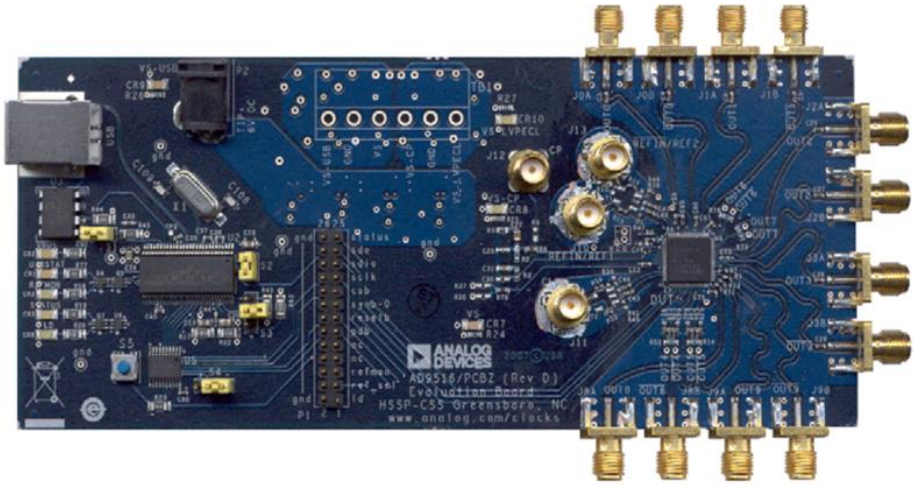

Figure 3-7. AD9516-4 PLL evaluation board.

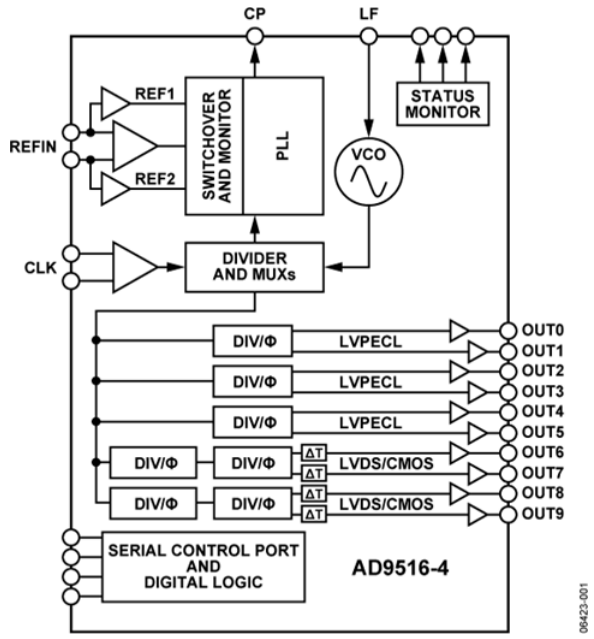

Figure 3-8. Simplified block diagram of the AD9615-4 PLL.

Figure 3-9 shows the PLL configuration that used for both PLL boards. To generate 100 MHz, the VCO is locked to the input reference of 10 MHz on its REF1 input and using N = 160 the VCO locks at 1.6 GHz. The VCO's output is divided by 2 and later by 8 (by divider 0) to have 100 MHz at the OUT0 output. Both PLL boards were set to exactly the same settings to measure the differences. The PLL settings on the GUI of the evaluation board's software is also showed.

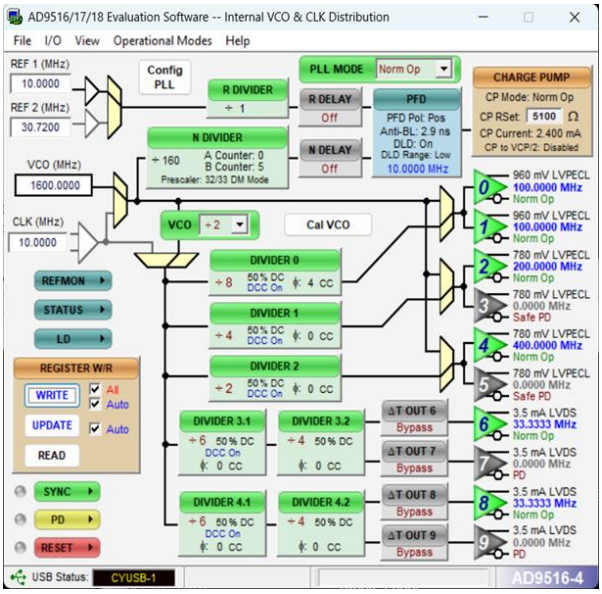

Figure 3-9. PLL settings as shown in the evaluation software.

3.5. Measurement Results

3.5.1. Timing Accuracy of the 1 PPS Signals

Figure 3-10 shows the histogram and the Gaussian distribution fit functions of the time interval measurements of the 1 PPS signals. All the measurements were logged for a minimum of 300 seconds to have sufficient data for statistical analysis. The accuracy of these 1 PPS signals could be considered as the main criteria for timing accuracy of two remote systems. WR LEN supports programmed trigger outputs which could be used as the ADC start conversion trigger signal.

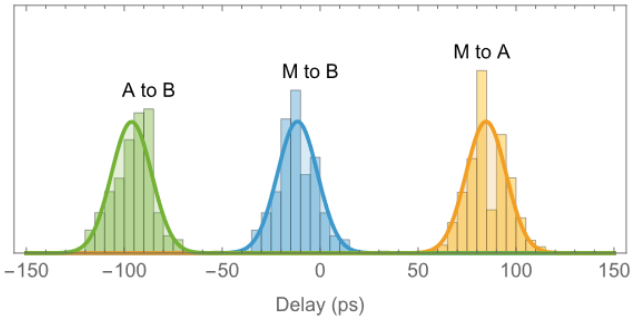

Figure 3-10. Time interval measurement results between 1 PPS signal.

The results are in a good agreement with White Rabbit specification of maximum 300 ps (peak-to-peak) accuracy of 1 PPS signals. Mean time delay between slave (A and B) to the master (M) module are 84.7 ps and -11.6 ps, respectively, and -96.3 ps in between A and B modules. Standard deviation of the measured values for all the values is 10.2 ps which confirms the White Rabbit specification of maximum of 60 ps peak-to-peak jitter for the 1 PPS signals. Figure 3-11 shows the oscilloscope screen shot of the 1 PPS signals.

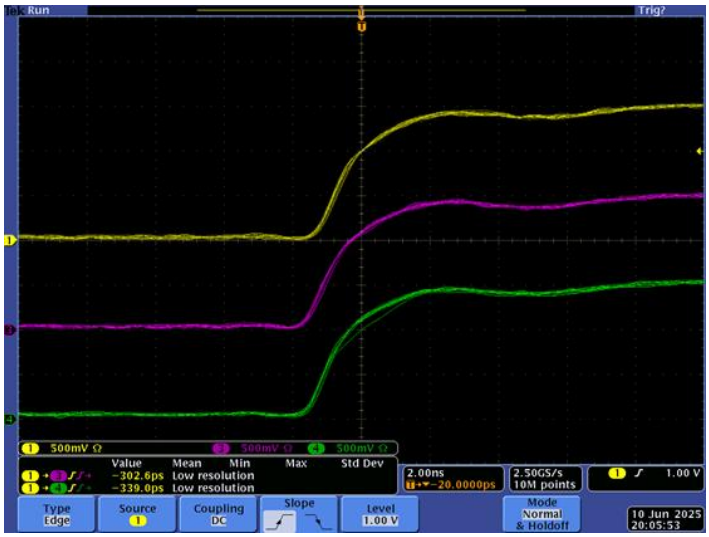

Figure 3-11. Oscilloscope screenshot of 1 PPS signals (Yellow: WR-M, Green: WR-A, and Magenta: WR-B).

3.5.2. Timing Accuracy of 10 MHz Clocks

To characterize the timing accuracy on the output of the White Rabbit modules, we measured the time delay in between the 10 MHz output signal and the 1 PPS output on each of the slave White Rabbit modules. Figure 3-12 shows the results of this measurement.

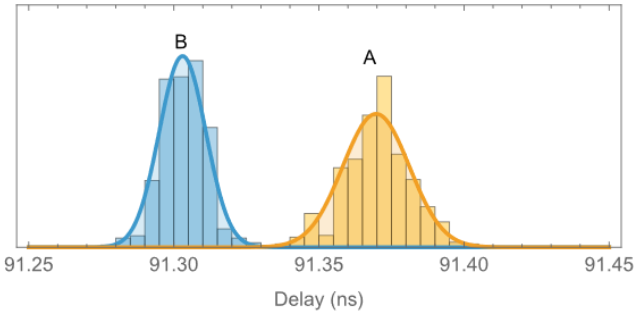

Figure 3-12. Delay between 1 PPS and the 10 MHz signals on the slave White Rabbit modules

The delays measured as 91.4 ns and 91.3 ns, with standard deviations of 11.5 ps and 8.0 ps, for WR-A and WR-B modules, respectively.

Figure 3-13 shows all 10 MHz clocks from WR boards (M, A, and B). Based on the oscilloscope waveform, a slight difference in the rise time of two slave modules is observable which could lead to errors in the edge detection of signals.

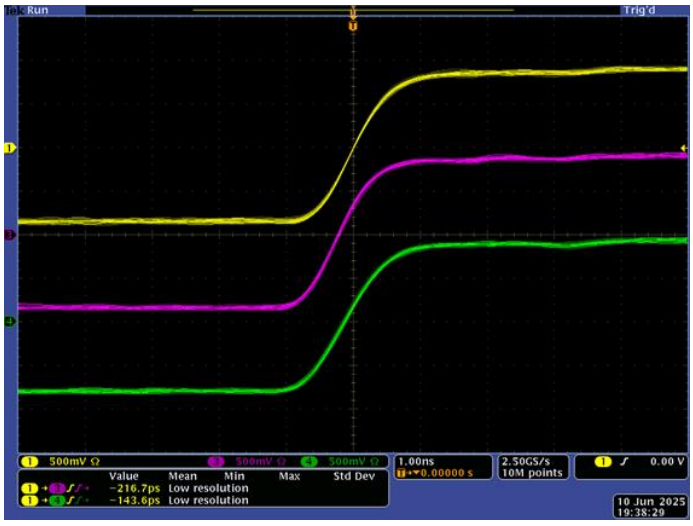

Figure 3-13. Oscilloscope screenshot of 10 MHz signals (Yellow: WR-M, Green: WR-A, and Magenta: WR-B).

3.5.3. Timing Accuracy of 100 MHz Clocks

To measure the total timing accuracy between the two slave channels A and B, we measured the time delay between the 100 MHz of one channel to the 1 PPS of the opposite channel. Figure 3-14 shows the results of this measurement.

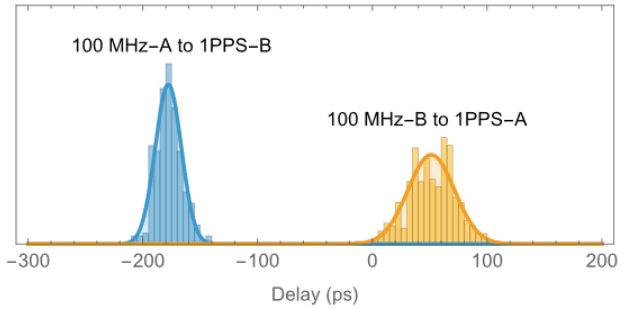

Figure 3-14. Time delay of 100 MHz to the 1 PPS of the opposite channel.

Both PLLs have exactly the same settings but we observed slightly different delays. The PLL boards have two programmable phase delay counters to fine-tune the delays up to 1.08 ns which could be used for calibration and edge alignment, but here we set all the delays to zero.

3.5.4. Longterm stability of 100 MHz Clocks

For long term timing stability, we logged the time delay between 100 MHz-A to 1 PPS-B for over 3 days. Figure 3-15 shows the long-term measurement (red graph is the moving average of 300 seconds length). Logged data shows a +50.3 ps jump in the last day which might be due to relocking of the PLL or an auto calibration event of the PLL when the VCO voltage reaches to its limits. The mean and standard deviation of the delay before the jump is -193.2 ps and 11.59 ps (calculated on the first 500 seconds of data) and after the jump is -142.9 ps and 12.37 ps (on the last 500 seconds of data), respectively.

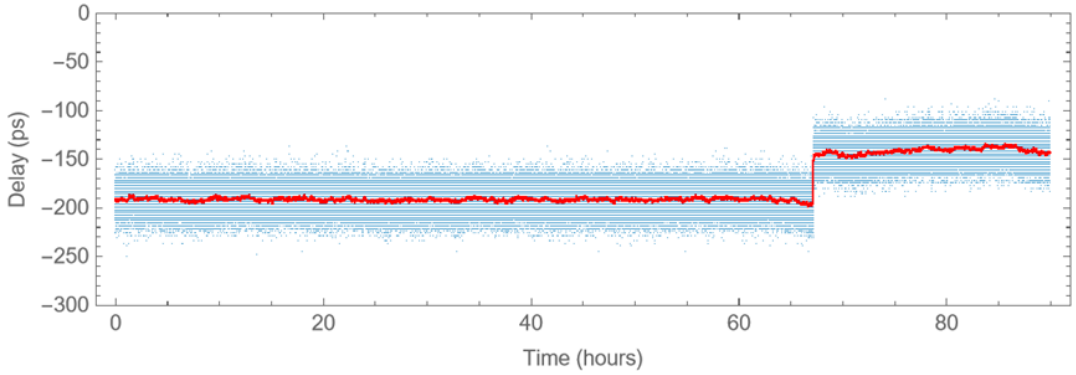

Figure 3-15. Longterm measurement of the time delay between 100 MHz of PLL-A to the 1 PPS-B.

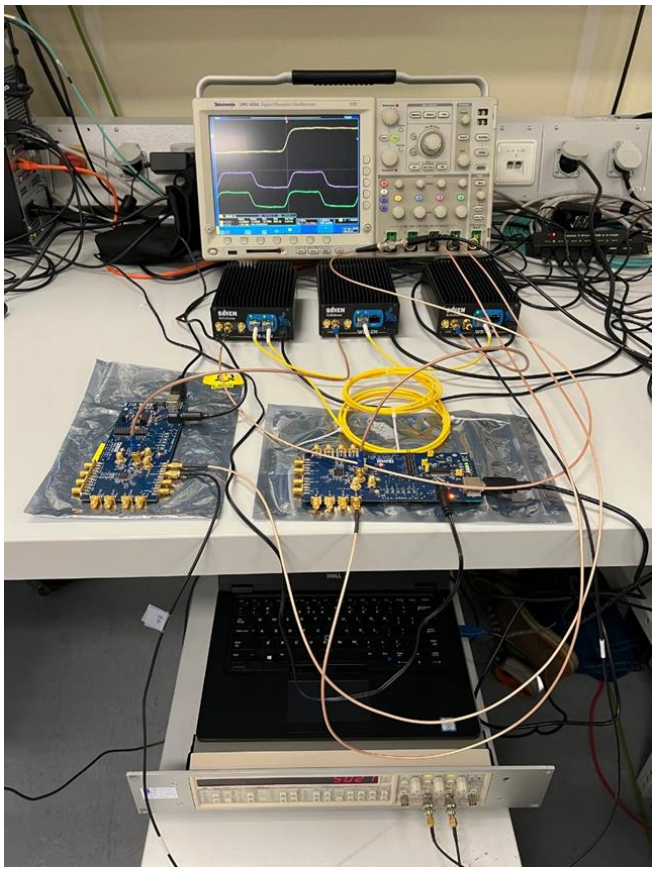

Figure 3-16. Measurement setup at VSL.

3.6. References

[1] https://en.wikipedia.org/wiki/White_Rabbit_Project

[2] https://ohwr.org/projects/white-rabbit/

[3] https://safran-navigation-timing.com/product/white-rabbit-len/

[4] https://www.analog.com/media/en/technical-documentation/data-sheets/AD9516-4.pdf

[5] https://www.analog.com/en/resources/evaluation-hardware-and-software/evaluation-boards-kits/eval-ad9516-4.html

[6] https://www.analog.com/media/en/technical-documentation/user-guides/UG-075.pdf

4. Method for traceable time jitter measurements

An important objective of the project was to develop at least one method for a traceable time jitter measurement technique needed to characterise time jitter below 50 ps for non-isolated and isolated trigger signals on the demonstrator clock hardware which has been developed.

4.1. Introduction

Time Jitter or jitter can be defined as the variation in time of a signal edge from its ideal time position. In other words, jitter is a measure of how early or late a signal event can differ from its ideal time. Existing different jitter definitions as [1-2]:

a) Cycle-to-Cycle Jitter. The time differences between successive periods of a signal. Cycle to cycle (C2C) jitter is defined in JEDEC Standard 65B as the variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs.

b) Period Jitter. An RMS calculation of the difference of each period from a waveform average. Period jitter is the deviation in cycle time of a clock signal with respect to the ideal period over a number of randomly selected cycles.

c) Long Term Jitter. Long-term jitter measures the change in a clock's output from the ideal position, over several consecutive cycles.

d) Phase Jitter. Phase noise is usually described as either a set of noise values at different frequency offsets, or as a continuous noise plot over a range of frequencies. Phase jitter is the integration of phase noises over a certain spectrum and expressed in seconds.

Time Interval Error (TIE). The difference in time between the actual threshold crossing and the expected transition point (or derived clock edge).

4.2. Jitter measurement using a fast oscilloscope

One method of characterizing the jitter level is to use a histogram of Time Interval Errors (TIE). The TIE is the time difference between the real clock signal edge to an ideal clock edge signal. First, Time Interval is defined as in the reference [2]:

$$TE(t) = T(t) - T_{ref}(t) \tag{4.2.1}$$

The difference in time between the current clock period to the reference clock period over N-period as depicted in Figure 4-1, is expressed as,

$$TIE(t,\tau) = \big(T(t+\tau) - T(t)\big) - \big(T_{ref}(t+\tau) - T_{ref}(t)\big) \tag{4.2.2}$$

$$TIE(t,\tau) = TE(t+\tau) - TE(t) \tag{4.2.3}$$

where τ, is the time interval which encompass N-periods to measure time error, TE.

As jitter can be considered as a random process, it is useful the compute or represent it by statistical tools, of which a histogram is the more popular and widespread. Therefore, in this method the histogram is computed and from it the TIE's standard deviation, coverage intervals, RMS value and peak-to-peak value can be computed and reported.

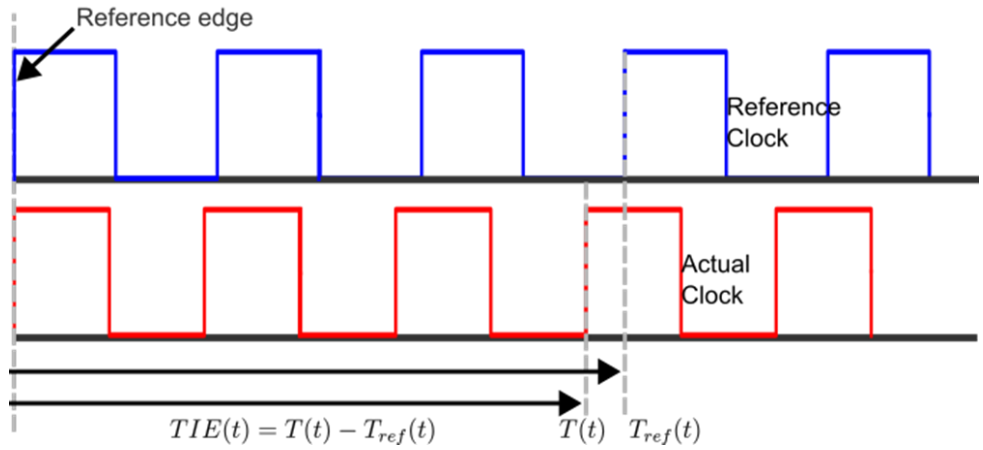

Figure 4-1. Time Interval Error. Blue signal is the reference clock; red signal represents the clock under test.

To measure jitter TIE it is necessary to use a real-time fast oscilloscope, with a large amount of internal memory. Since the TIE is the time difference (see eq. (4.2.2)) an external clock reference of 10 MHz from an atomic clock is needed in order to guarantee traceability.

The scope has to be configured for a large observation time, in order to capture a large number of periods from the reference edge, which is commonly the trigger point.

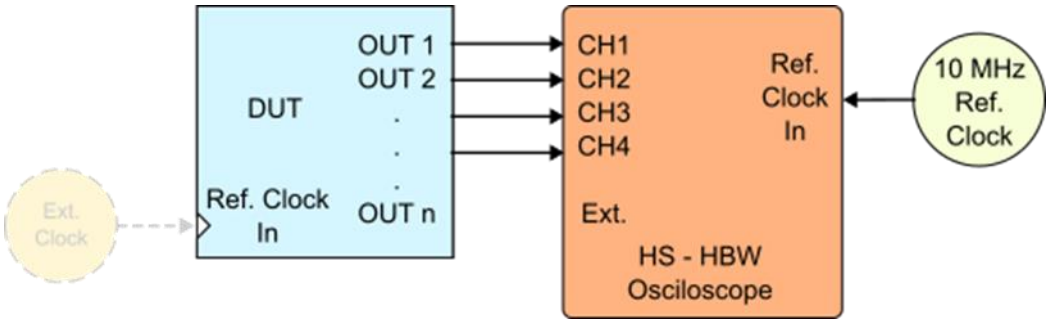

Figure 4-2. Time Interval Error measurement setup. An external clock frequency of 10 MHz is plug to the high speed oscilloscope. The DUT can be any device to characterize Jitter. (optional) An external clock reference could be connected to the DUT

4.3. Clock platforms for Jitter measurement and characterization

Using the platform described in sections 2.5 to 2.7 several jitter tests were carried out. Different clock frequencies were synthesized by the FPGA core and with the Digital PLL.

a) Clock signals generated by the FPGA. The selected FPGA for this project has the capability to generate up to 4 clock signals., It can be configured and setup using the Xilinx Clock Wizard application [5] allowing it to generate two primitives, a mixed-mode clock manager (MMCM) and/or phase-locked loop (PLL).

The clock output can be set up to frequencies of 664 MHz for this specific device. In Table 1 a list of possibles frequencies for this project are depicted. Figure 4-3 shows the block diagram of the FPGA clock core and Figure 4-4 reports the core clock IP configuration diagram.

Table 1. Clock generation frequency specification.

	Conf. #1	**Conf. #2**	**Conf. #3**	**Conf. #4**
CLK_1	10 MHz	50 MHz	25 MHz	10 MHz
CLK_2	100 MHz	100 MHz	50 MHz	100 MHz
CLK_3	100 MHz		100 MHz	50 MHz
CLK_4	50 MHz			

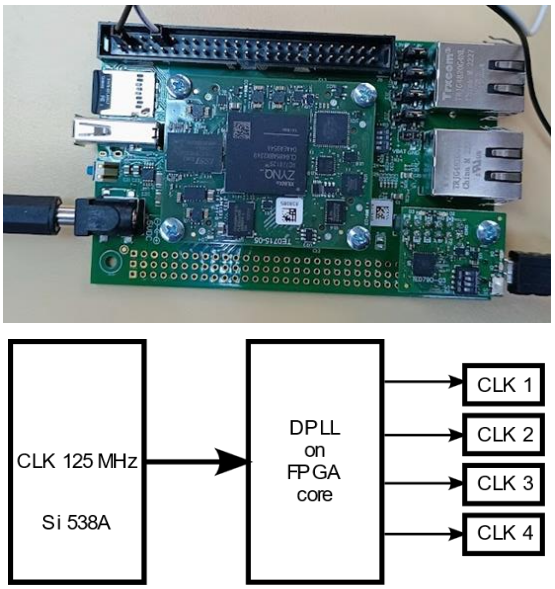

Figure 4-3. FPGA core clock signals frequencies.

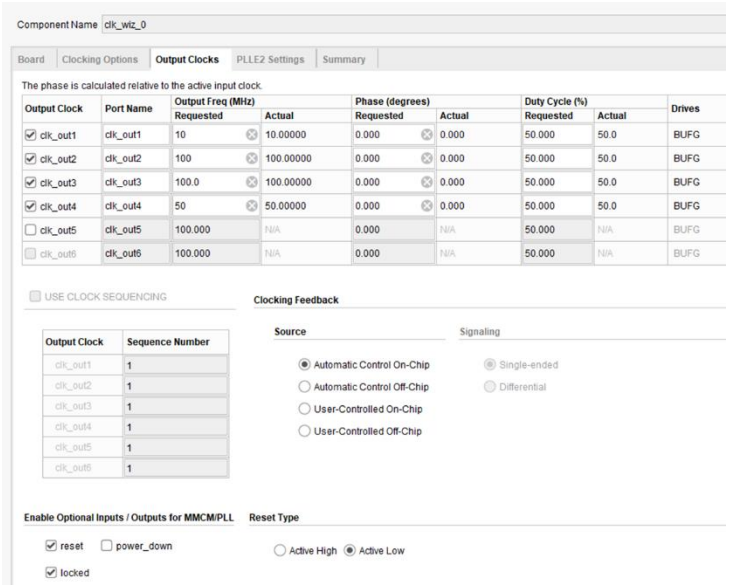

Figure 4-4. FPGA core clock configuration diagram.

Figure 4-5 shows the clock wizard used for setting the signal frequencies and the output paths using Vivado development environment.

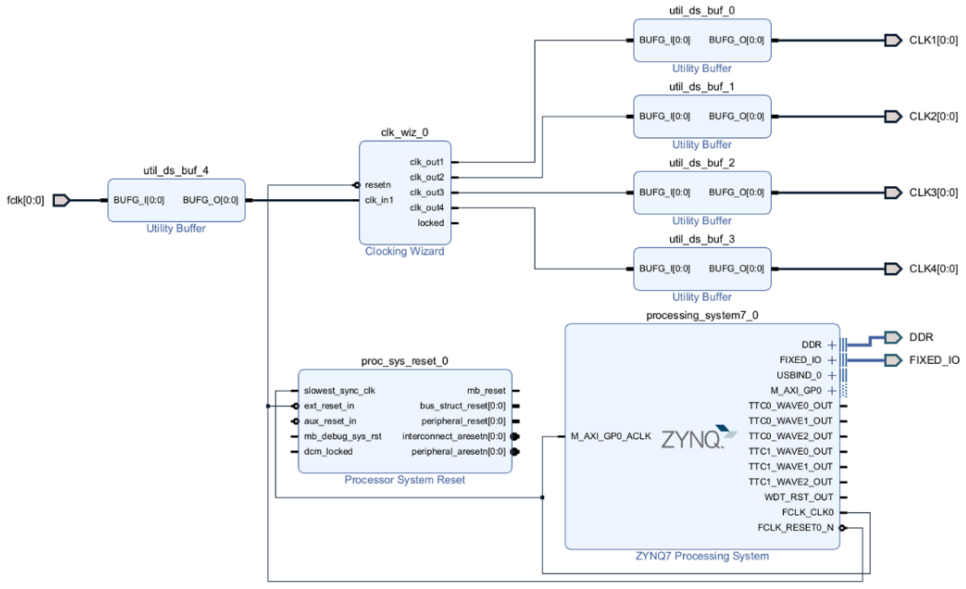

Figure 4-5. FPGA core clock wizard to setup signals frequencies and output paths

b) Clock signals generated by the EVM-LMK05318B evaluation board.

The second board is a network synchronizer clock evaluation module. The evaluation board was already described in section 2.5 and 2.6. It was used to synthesize four clock output frequencies as shown in Figure 4-6, at 100 MHz.

An external stable clock signal was plug into the external clock reference input in order to provide a clean frequency reference.

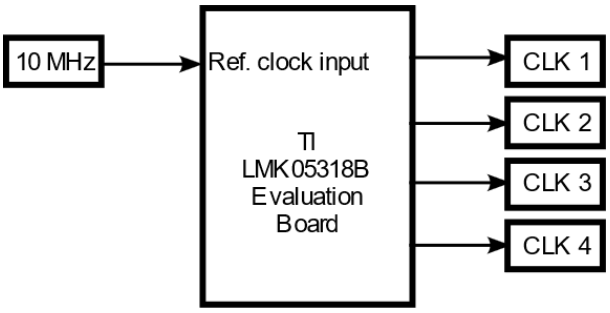

Figure 4-6. EVAL-LMK05318B clock configuration.

4.4. Sources of Jitter

There are several sources of jitter, [4], which are reported below:

1) Systems and circuits: jitter arises from, for example, crosstalk between components, interaction between circuits , or impedance mismatch.
2) Data jitter is caused by errors in data transmission such as. symbol interference, duty-cycle errors, bit-sequence periodicity.
3) Random noise. Jitter is related to noise in the system: thermal noise, shot noise, 1/f noise.

The first two sources of jitter reaches its maximum and minimum values between a deterministic period of time, so it is also called as deterministic jitter. Instead, the third source jitter reaches its minimum and maximum at any time interval, thus it is referenced as random jitter.

4.5. Jitter effect on ADC performance

Clock jitter affects ADC performance directly. To calculate the jitter noise power we can use the following [6]:

$$SNR_{jitter}(dBFS) = -20\log(2\pi f_{in} t_{jRMS}) \quad (4.5.1)$$

where f_{in} is the input signal frequency to be sampled and t_{jRMS} is the RMS jitter. In order to obtain the SNR degradation due to jitter, this results should be subtracted from the ADC SNR specification:

$$SNR_d(dBFS) = 10\log\left(10^{\frac{-SNR_{ADC}}{10}} + 10^{\frac{-SNR_{jitter}}{10}}\right) \quad (4.5.2)$$

And therefore, the effective number of bits (ENOB) it is also degraded.

4.6. Jitter measurement accuracy and uncertainty budget

The jitter measurement depends on the signal characteristics to be measured, and the instrumentation involved. Therefore, apart from the instrument's accuracy, the signal quality plays an important role. Some instrument factors which have to be taken into account are [7-8]:

- instrument timing stability;
- sampling noise;
- amplitude instrument noise floor;
- signal interpolation error and amplitude noise.

When using a high speed real-time oscilloscope all these factors are specified, according to a manufacturer, as *Delta-Time accuracy* (DTA) [8] or *Jitter Measurement Floor* (JMF) [7].

DTA usually can be estimated from the following relationship [8]:

$$DTA_{RMS} = \sqrt{2 \cdot \left(\left(\frac{N}{A} \cdot t_{rm}\right)^2 + t_j\right)} + TBA \cdot t_p \tag{4.6.1}$$

where N is the input referred noise (V_{RMS}), A is the input signal amplitude (V), t_{rm} is the measured risetime, t_j is the aperture uncertainty, TBA is the base time accuracy and t_p is the measurement duration. Typical DTA values are listed in the oscilloscope specification.

JMF is the lowest jitter value when measure a reference signal with zero jitter, then this value is subtracted from the measured jitter, J_m, to obtain the real jitter, J_r, using the following equation [7]:

$$J_r = \sqrt{J_m^2 - JMF^2} \tag{4.6.2}$$

4.7. References

[1] ITU-T Recommendation G.810: Definitions and Terminology for Synchronization Networks," International Telecommunication Union (ITU), 1996.

[2] Da Dalt N, Sheikholeslami A. "Understanding Jitter and Phase Noise: A Circuits and Systems Perspective". Cambridge University Press; 2018.

[3] SiT-AN10007 Rev 1.21, "Clock Jitter Definitions and Measurement Methods".

[4] Johnnie Hancock , "Jitter—Understanding it, Measuring It, Eliminating It Part 1: Jitter Fundamentals", High Frequency electronics, 2004.

[5] https://docs.amd.com/r/en-US/pg065-clk-wiz/Clocking-Wizard-v6.0-LogiCORE-IP-Product-Guide.

[6] Derek Redmayne, Eric Trelewiczand Alison Smith (High Speed ADC Product Marketing Engineer) DN1013 - Understanding the Effect of Clock Jitter on High Speed ADCs, Analog Devices.

[7] Johnnie Hancock and Steve Draving, "Jitter—Understanding it, Measuring It, Eliminating It Part 2: Jitter Measurements ", High Frequency electronics, 2004.

[8] Tektronix application note 61W_18786_2.

[9] Tektronic 6 Series MSO Specifications and Performance Verification.

5. Method for traceable measurements of clock stability

5.1. Introduction

Accurate and reliable evaluation of clock stability is essential for high-precision analog-to-digital converter (ADC) architectures and systems that require a stable timekeeping reference. To ensure that such measurements are traceable - i.e., directly linked to the International System of Units (SI) - the stability of a device under test (DUT) must be compared to a reference clock whose performance is well-characterized and traceable to a national or international time standard.

This section discusses the principle and method employed to achieve traceable measurements of clock stability of the demonstrator timing platform. The typical approach assumes that both the DUT and the reference clock are located within the same facility or laboratory. The reference may be a local realization of a national time scale or a high-performance commercial device that is periodically calibrated and synchronized to a national metrology institute. Crucially, the reference clock must exhibit superior frequency stability to ensure that observed variations can be confidently attributed to the DUT.

Two key parameters define the performance of any frequency reference: accuracy, which describes how closely the clock's output aligns with the SI-defined second, and stability, which describes the consistency of that output over time. While stability is a prerequisite for accuracy, it is not sufficient on its own; many oscillators are stable over short timescales yet deviate significantly from the true second over longer durations.

To evaluate these characteristics, this section introduces the conceptual framework for frequency stability comparison and describes how frequency differences between the DUT and reference are monitored and processed to estimate the relative fractional frequency devastations.

5.2. Method using digital time counter

The method proposed for practical estimation and characterization the frequency stability of the clock signals generated with the demonstrator timing platform is based on the use of a digital counter which is a well-defined universal tool used for a wide range of applications, spanning from telecommunications to fundamental research [1-7].

Figure 5-1, shows the general schematic of the proposed method. The prerequisite of the method is that the clocks must be well synchronized. The synchronization signal is derived starting from the reference clock, i.e. 10 MHz signal distributed coming from the atomic clock.

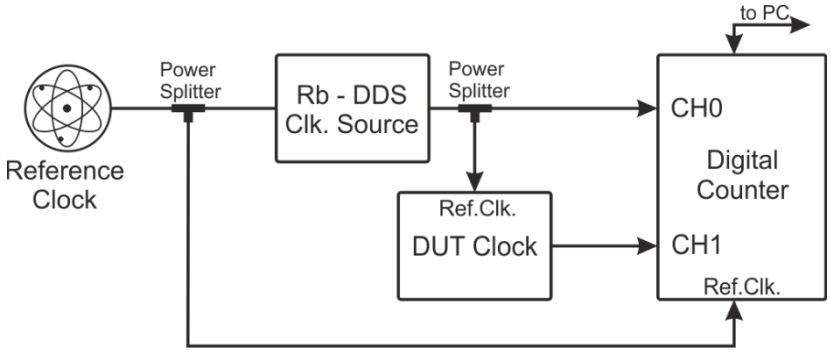

Figure 5-1. Generalized measurement setup for clock stability characterization of a DUT device based on the use of digital counter

5.3. Clock stability setup for FPGA demonstration board

For the measurement of the clock stability using the FPGA platform a modified measurement setup has been used. Since in the present development of the FPGA platform it cannot be frequency locked to the external source the proposed setup results simplified, and is modified as follow:

- The two-channel counter is frequency locked to the 10 MHz laboratory reference signal.
- The two outputs of the FPGA timing platform are directly connected to the digital counter inputs.

All the measurements have been performed by setting the gate time of the counter to approximately 1 s. The stability of the clock delivered by the FPGA platform has been measured before and after the galvanic optical fibre isolator.

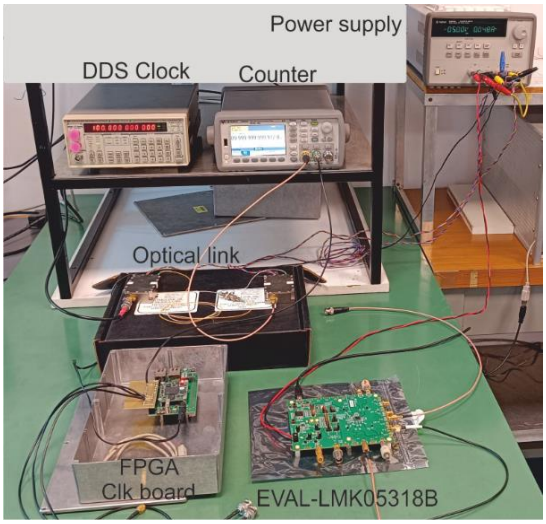

Figure 5-2. Photo of the experimental setup employed for clock stability measurements on the FPGA npt PLL platform (left side) and on the PLL EVM LMK05318B (right side).

5.4. Setup for frequency stability measurements on the PLL EVM board.

To perform the clock stability measurements on the PLL EVM-LMK05318B platform the following changes on the experimental setup were made:

- The EVAL-LMK05318B was externally synchronized to a reference signal derived by the 10 MHz signal using a DDS clock generator, as shown in Figure 2.
- The reference clock of the counter is connected to the 10 MHz through a power splitter.
- The counter measured the 10 MHz reference signal and the synchronism signal generated by the DDS clock generator and the signal generated by the EVM-LMK05318B

The present measurement campaign aims to emphasize the quality of the clock signals generated by the EVM-LMK05318B platform in terms of accuracy and stability compared to with the reference 10 MHz clock.

Measurement results are reported in the next section.

The frequency stability measurements on the white Rabbit platform for the 1 PPS, 10 MHz and 100 MHz signals are reported in the section 3.5.

5.5. References

[1] P. Kartaschoff, “Synchronization in digital communications networks,” *Proc. IEEE*, vol. 79, pp. 1019–1028, July 1991.

[2] J. C. Bellamy, “Digital network synchronization,” *IEEE Commun. Mag.*, vol. 33, pp. 70–83, Apr. 1995.

[3] S. Bregni, “Clock Stability Characterization and Measurement in Telecommunications” *IEEE Trans. Instrum. Meas.*, vol. 46, no. 6, Dec. 1997.

[4] F. L. Walls and D. W. Allan, “Measurement of frequency stability,” *Proc. IEEE*, vol. 74, Jan. 1986.

[5] D. W. Allan, “Time and frequency metrology: Current status and future considerations,” in *Proc. 5th Eur. Frequency Time Forum*, 1991.

[6] C. A. Greenhall, “A method for using a time interval counter to measure frequency stability,” in *Proc. 41st Annu. Frequency Control Symp.*, 1987.

[7] J. A. Barnes, A. R. Chi, L. S. Cutler, D. J. Healey, D. B. Leeson, T. E. McGunigal, J. A. Mullen, Jr., W. L. Smith, R. L. Sydnor, R. F. C. Vessot, and G. M. R. Winkler, “Characterization of frequency stability,” *IEEE Trans. Instrum. Meas.*, vol. IM-20, May 1971.

6. Experimental results

6.1. Introduction

In this section there are reported the measurements of time delays, jitter and clock stability of the hardware platform tested during the project. Here we briefly summarize the importance of such of measurements on the ADC performances.

Time delay measurements are of particular importance for ADCs with a composite architecture based on parallel structures. In such a case, the non-deterministic nature of the clock alignment causes additional distortion of the final waveform. When multiple sub-ADCs operate in parallel - such as in time-interleaved architectures - any mismatch in clock phase or sampling instant between channels introduces timing skew, resulting in amplitude-dependent errors and interleaving artifacts. These timing mismatches are particularly critical when high resolution and accuracy are required, as even sub-picosecond variations can propagate into significant spurious components in the frequency domain.

Moreover, in metrological applications where measurement traceability and uncertainty budgets are tightly controlled, such time delay inconsistencies challenge the reliability of the output data. The composite signal reconstruction relies heavily on accurate timing alignment; therefore, the lack of determinism in sampling instants leads to degraded Signal-to-Noise and Distortion Ratio (SINAD) and reduced Effective Number of Bits (ENOB). This degradation is often indistinguishable from real signal features, complicating post-processing and calibration routines. Compensating for time delay effects often requires intricate calibration procedures or sophisticated digital correction algorithms, but these too have limitations in terms of stability over temperature, aging, and dynamic input conditions. As such, ensuring deterministic and stable timing across all channels is not just a design preference but a performance-enabling requirement for high-precision ADC systems in metrological contexts.

Clock stability is crucial in all the ADCs, as even minor timing deviations can introduce measurement errors that compromise accuracy and traceability. In precision measurements, clock jitter affects the sampling instant, leading to errors in the digitized signal that can corrupt low-level or slowly varying input voltages. In particular, for high-resolution ADCs used in metrology, unstable clock signals can degrade the Effective Number of Bits (ENOB), resulting in reduced dynamic range and increased uncertainty. Furthermore, the stability of the ADC's sampling clock directly impacts the linearity and repeatability of measurements, which are critical for calibration and standards compliance. To ensure accurate and consistent results in metrological systems, the ADC clock must exhibit low jitter and long-term frequency stability.

Phase noise and jitter noise are two related quantities associated with a noisy oscillator. Phase noise is a frequency-domain view of the noise spectrum around the oscillator signal, while jitter is a time domain measure of the timing accuracy of the oscillator period. Clock Jitter in ADC is probably the most obscure specification in data converters. It basically describes the timing errors in the sampling operation due to clock disturbances. This error cannot be corrected later in the ADC because it is already attached into the sampling sequence being processed for digitization and will impact the overall performance of the ADC. Therefore, clock jitter is critical to the performance of an ADC and must be specified appropriately.

6.2. Time delay measurement results

An evaluable method and measurement results for traceable time delay measurements using the experimental setup based on three White Rabbit LEM modules (WR) and two PLL boards is described in the chapter 3.

Here we report the measurement results obtained with the EVM-LMK05318B board.

Figure 6-1 reports the test bench set up for time delay measurements and frequency stability. Time delay measurements are performed with a high sampling rate oscilloscope; frequency stability measurements are performed with a high precision frequency counter.

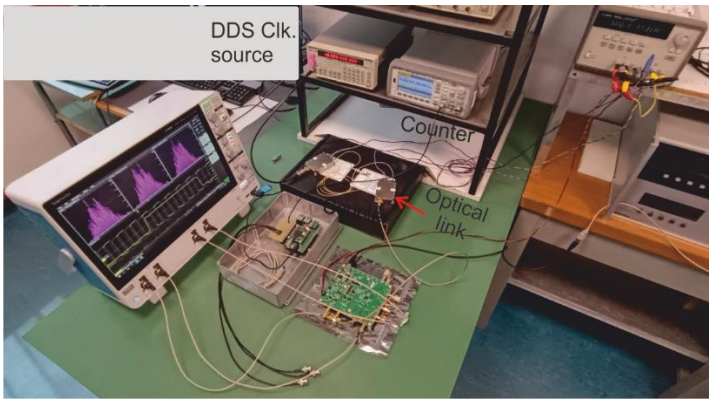

Figure 6-1 Test bench for time delay measurements and frequency stability.

The test bench with the EVM-LMK05318B was configured as follows:

- Clock in reference linked to the 10 MHz clock provided by the DDS clock source linked to the 10 MHz national reference signal.
- Optical link inserted between the output of the DDS clock source and the clock in reference port of the EVM-LMK05318B;
- CH1 of the MSO oscilloscope connected to the receiver output of the optical link.
- Three outputs of the EVM-LMK05318B programmed for generation of isofrequential clocks 10 MHz and 100 MHz.

The high speed oscilloscope measures the four signals and calculates the time-delays of the three clocks with respect the to 10 MHz input signals.

Figure 6-2 reports the time delay measurements of the three 10 MHz clock signals generated with the EVM-LMK05318B computed with respect the 10 MHz reference clock signal. As can be shown the relative differences are within 30 ns without soft rest chip.

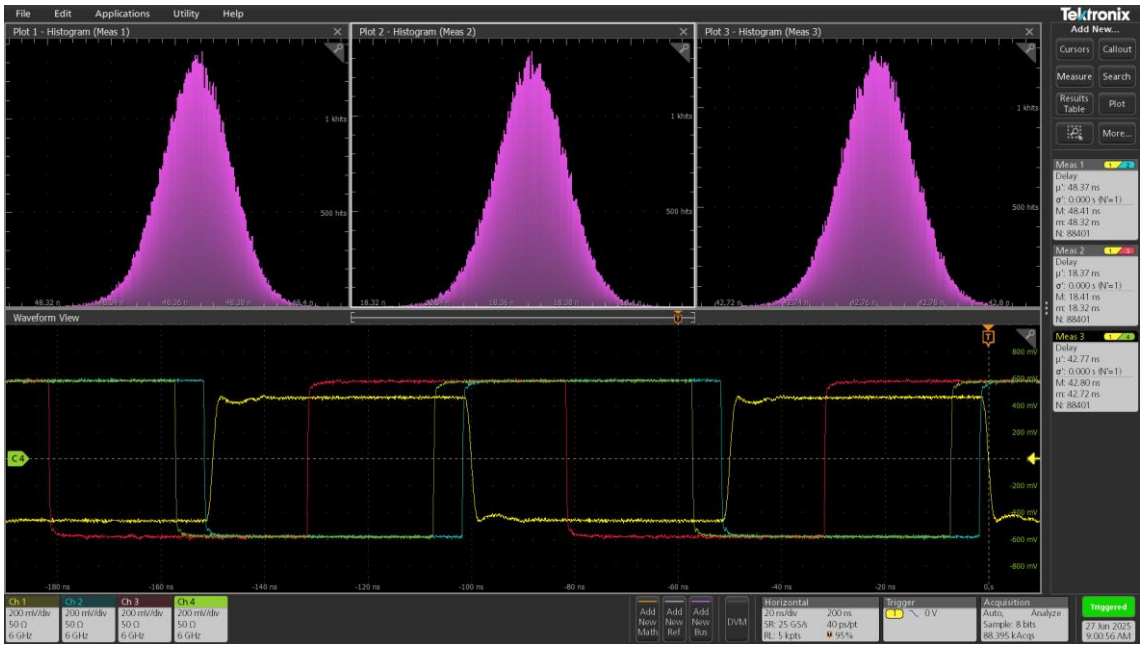

Figure 6-2. Time delay of three 10 MHz clocks measured with respect the 10 MHz reference clock signal. Yellow waveform is the 10 MHz reference clock signal.

Figure 6-3 reports the time delay measurements of the three 100 MHz clock signals generated with the EVM-LMK05318B computed with respect the 10 MHz reference clock signal. In this case the relative differences are within 1 ns without soft reset chip.

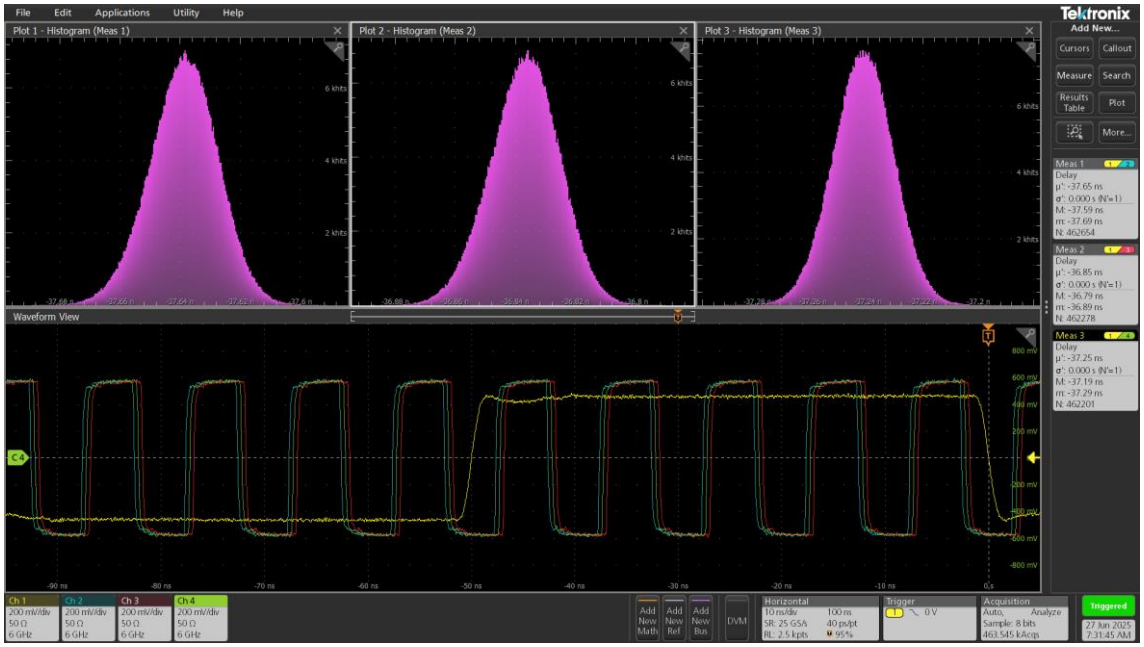

Figure 6-3. Time delay of three 100 MHz clocks measured with respect the 10 MHz reference clock signal. Yellow waveform is the 10 MHz reference clock signal.

The EVM LMK05318B provides a self-synchronization mechanism suitable to align the phase of the clock signals with picosecond resolution by using a reset mechanism. The GUI enables this reset mechanism by pushing the *soft rest chip* button.

Figure reports the measurement results in terms of relative time delay after the synchronization on the EVM LMK05318B. For this test the outputs 4, 5 and 6 have been set to deliver clock signals having the same frequency 10 MHz and 100 MHz or different frequencies, e.g. the OUT 4 and 5 set to 10 MHz and OUT 6 set to 100 MHz.

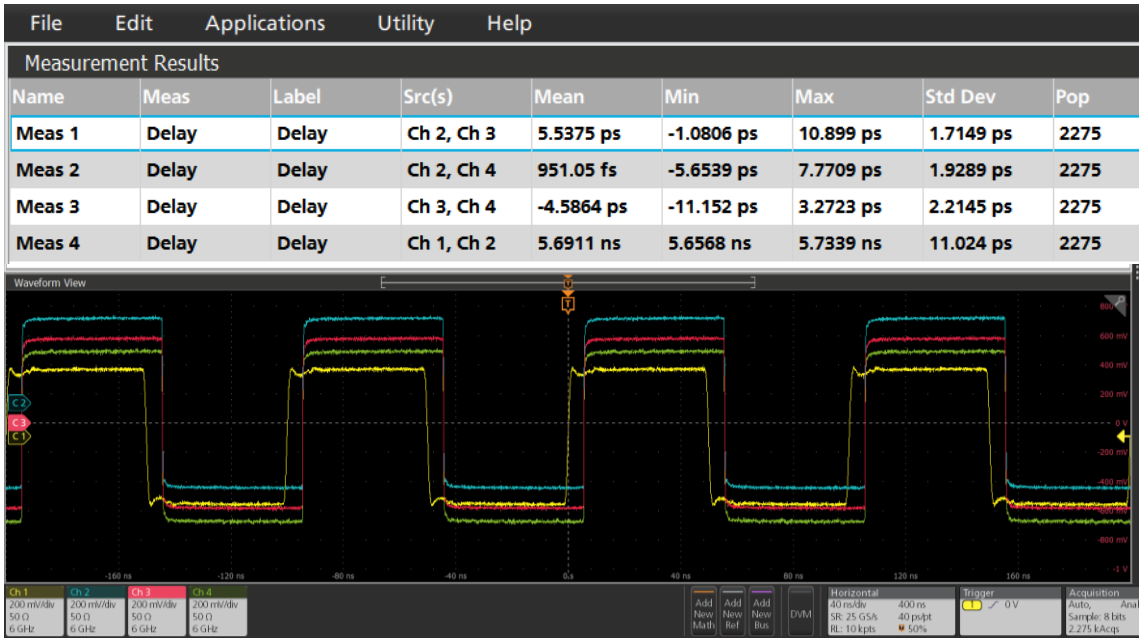

Figure 6-4. Relative time delays measurements on three outputs set to 10 MHz (blue, red and green traces). Yellow trace the 10 MHz reference clock provided by the optical link.

File Edit Applications Utility Help

Measurement Results

Name	Meas	Label	Src(s)	Mean	Min	Max	Std Dev	Pop
Meas 1	Delay	Delay	Ch 2, Ch 3	5.0860 ps	-1.1466 ps	11.858 ps	1.7327 ps	2233
Meas 2	Delay	Delay	Ch 2, Ch 4	312.96 fs	-5.7328 ps	6.4404 ps	1.9274 ps	2233
Meas 3	Delay	Delay	Ch 3, Ch 4	-4.7731 ps	-12.147 ps	1.9552 ps	2.1486 ps	2233
Meas 4	Delay	Delay	Ch 1, Ch 2	-44.514 ns	-44.549 ns	-44.479 ns	11.177 ps	2233

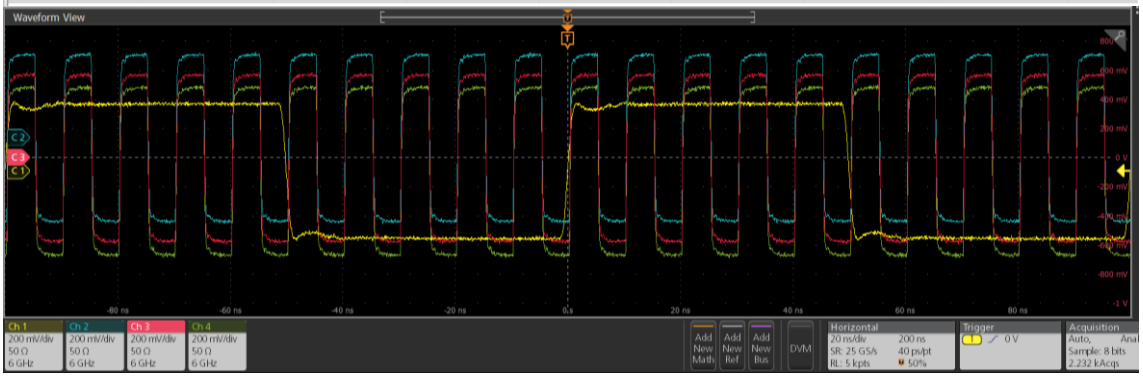

Figure 6-5. Relative time delays measurements on three outputs set to 100 MHz (blue, red and green traces). Yellow trace the 10 MHz reference clock provided by the optical link.

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Measurement Results

Name	Meas	Label	Src(s)	Mean	Min	Max	Std Dev	Pop
Meas 1	Delay	Delay	Ch 2, Ch 3	5.5984 ps	-204.66 fs	10.368 ps	1.7001 ps	1917
Meas 2	Delay	Delay	Ch 2, Ch 4	-4.6655 ps	-11.117 ps	1.7513 ps	1.9262 ps	1917
Meas 3	Delay	Delay	Ch 3, Ch 4	-10.264 ps	-16.748 ps	-2.0535 ps	2.1512 ps	1917
Meas 4	Delay	Delay	Ch 1, Ch 2	7.2924 ns	7.2535 ns	7.3300 ns	10.988 ps	1917

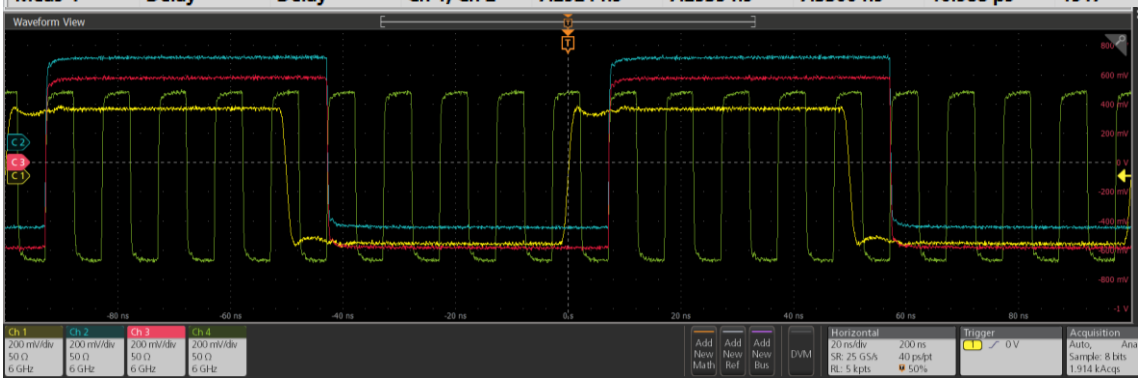

Figure 6-6. Relative time delays measurements of three outputs set to 10 MHz (blue and red traces) and 100 MHz green trace. Yellow trace the 10 MHz reference clock provided by the optical link.

Using a second EVM-LMK05318B board (at IPQ), the time delay between output signals of 10 MHz and 100 MHz was measured using an Oscilloscope Tektronix MSO64B (1 GHz, 50 GS/s) referenced to a 10 MHz signal from a caesium atomic clock of the Lab. The same 10 MHz signal was used as the external reference of the EVM-LMK05318B board and connected to the input of the Oscilloscope.

The cables connecting the Board clock signal outputs to the Oscilloscope were the same length to ensure an identical delay was introduced by the cables.

The outputs of the Evaluation Board were synchronized through the control software of the Board before the measurements, running the command “soft reset”. Figure 6-4 shows the 100 MHz signals before and after synchronization.

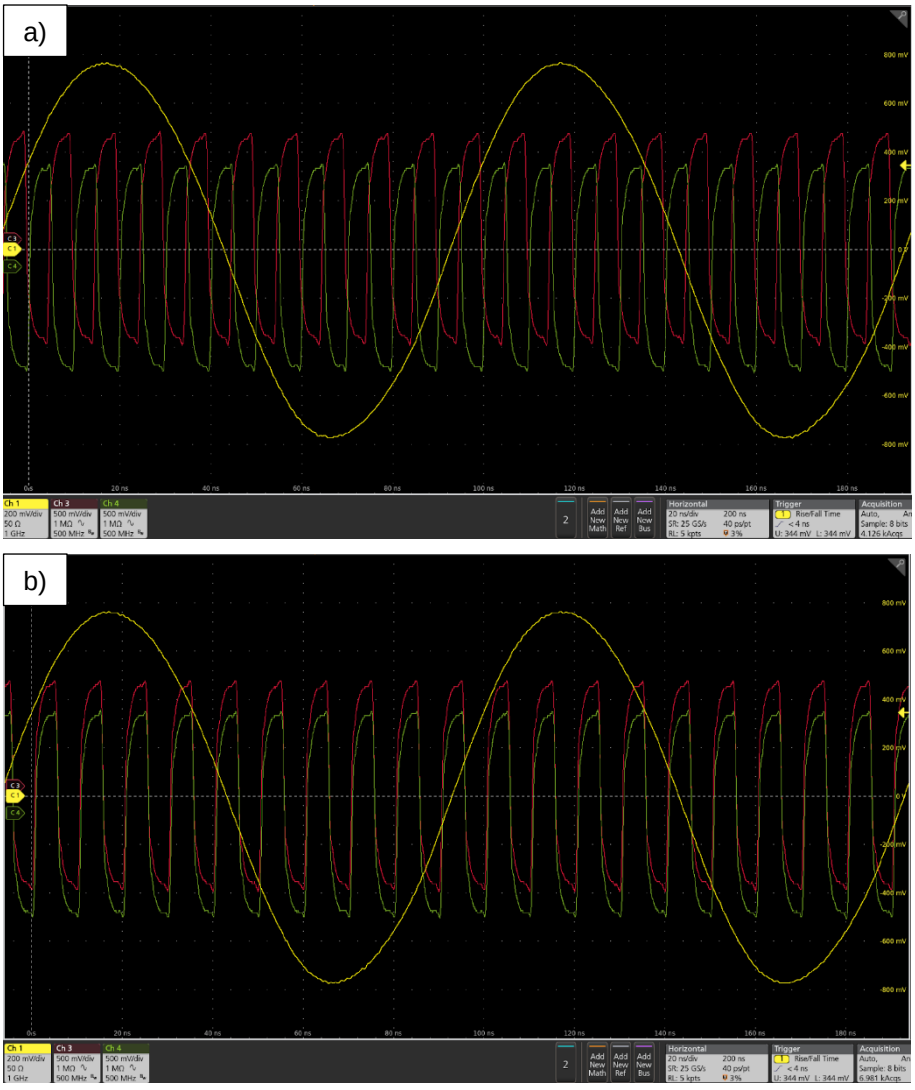

Figure 6-7. 10 MHz reference signal (yellow curve), 100 MHz clock output (channel 3, red curve) and 100 MHz clock output (channel 4, green curve), a) before being synchronized; b) after being synchronized.

The time delays between signals shown in Figures 6-8 to 6-10, were measured after synchronization.

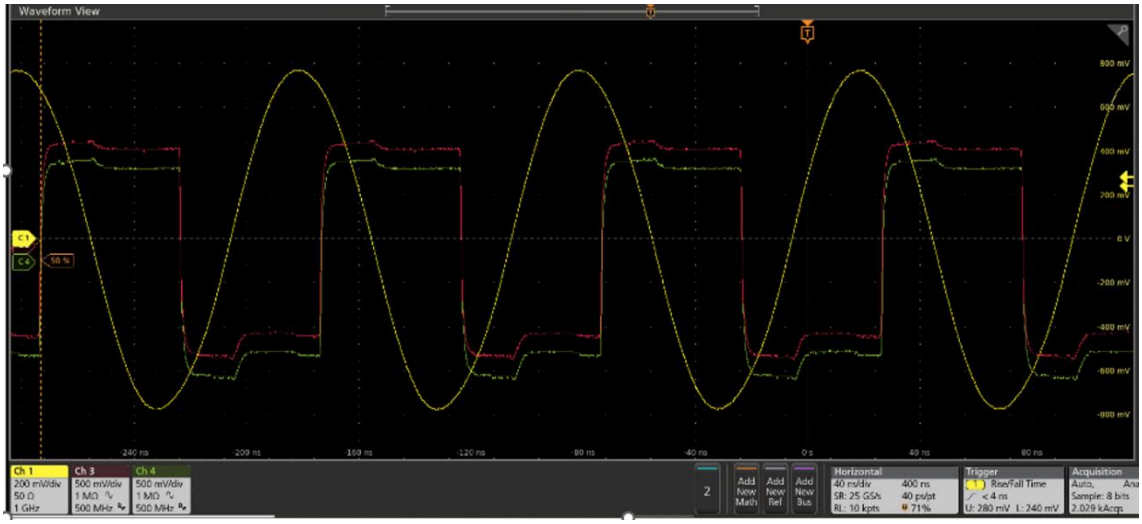

Figure 6-8. Time delay measured between the 10 MHz clocks outputs (red curve and green curve); 10 MHz reference clock signal (yellow waveform).

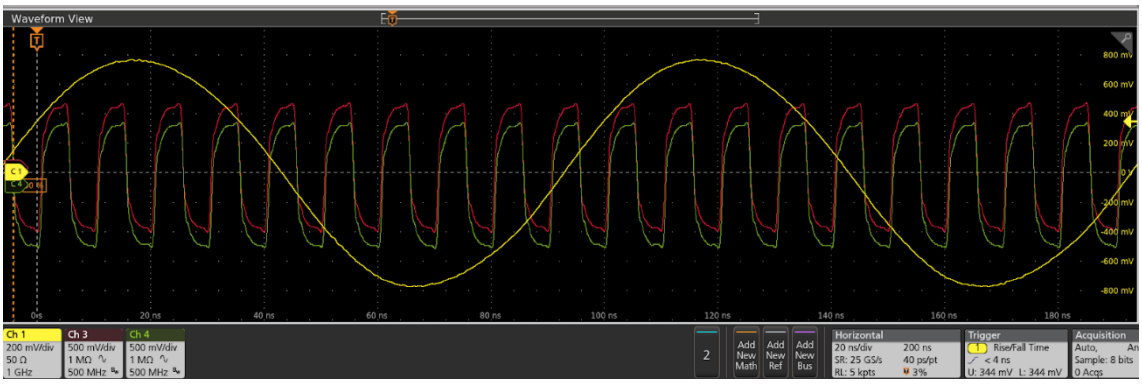

Figure 6-9. Time delay measured between the 100 MHz clocks outputs (red curve and green curve); 10 MHz reference clock signal (yellow waveform).

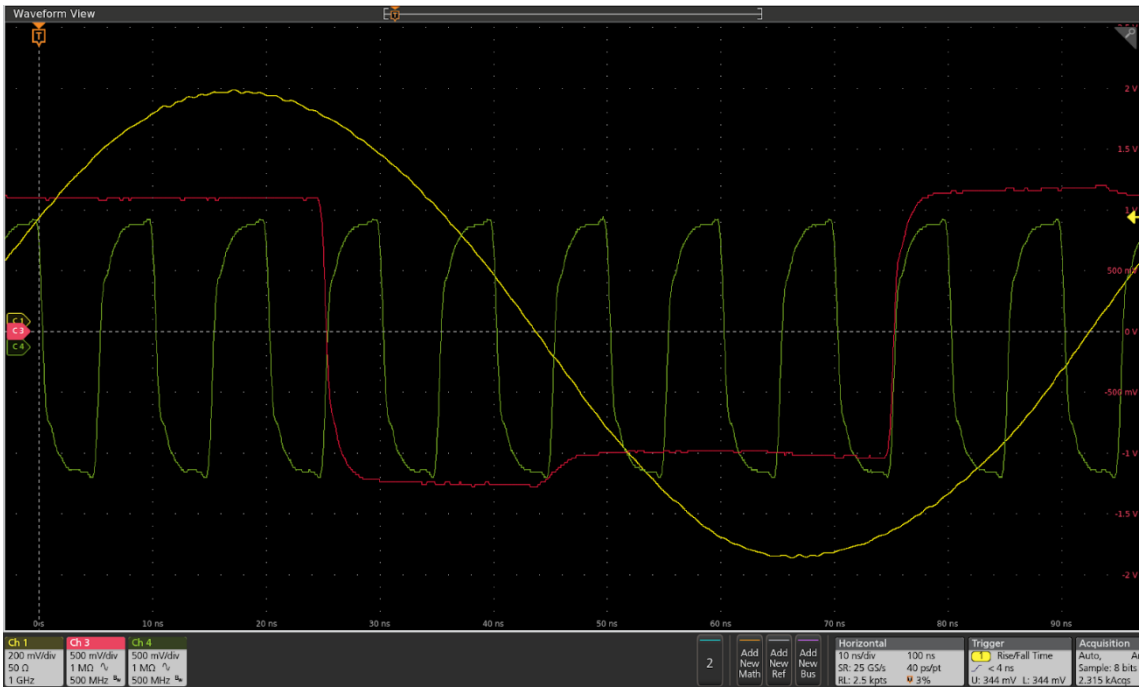

Figure 6-10. Time delay measured between the 10 MHz clocks outputs (red curve) and the 100 MHz (green curve); 10 MHz reference clock signal (yellow waveform).

The characterization of the two EVM LMK05318B boards at INRIM and IPQ in terms of time delay shows and excellent agreement, and the measurement results can be summarized as follows:

- The relative time delay between the outputs for both 10 MHz and 100 MHz signals are within a few picoseconds, and the standard deviation is below 2 ps.
- The relative difference between outputs programmed to generate 10 MHz and 100 MHz clock signals is within 10 ps, and the standard deviation below 2 ps.
- The relative time delay differences between the outputs and the refence clock in input are not deterministic and are subject to variation from a few nanoseconds to tens of nanoseconds.

6.3. Time jitter measurement results

Several tests on the platforms described in section 4.3 were performed. The jitter was characterized and measured in terms of the Time Interval Error TIE and phase noise.

6.3.1. Jitter measurement on FPGA

Figure 6-11 shows the test bench for jitter measurements on the FPGA platform. The outputs of the FPGA platform are connected to the inputs of the fast oscilloscope as follows:

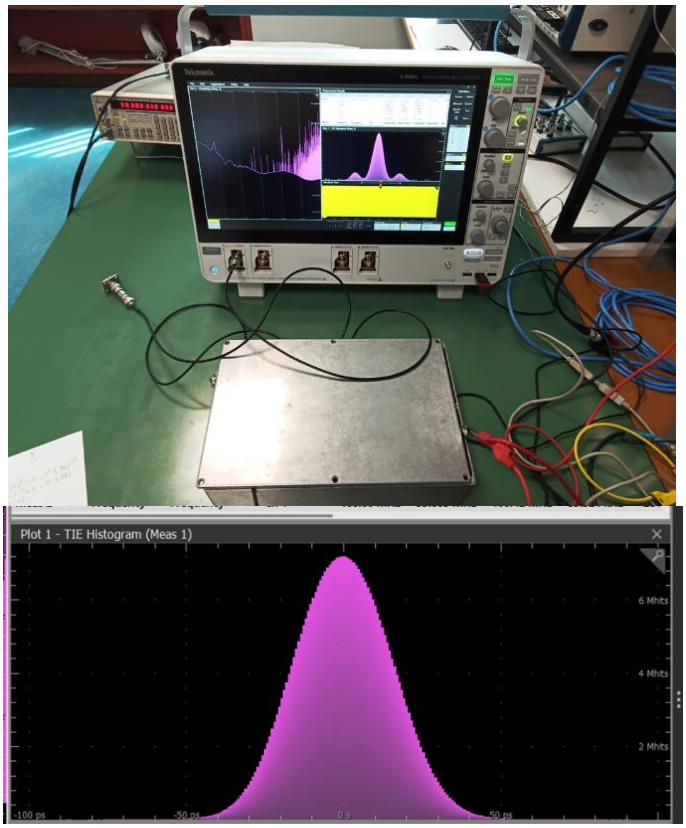

Figure 6-11. Trest bench photo and TIE histogram on FPGA jitter measurements.

A) One signal of 100 MHz connected at CH-1.

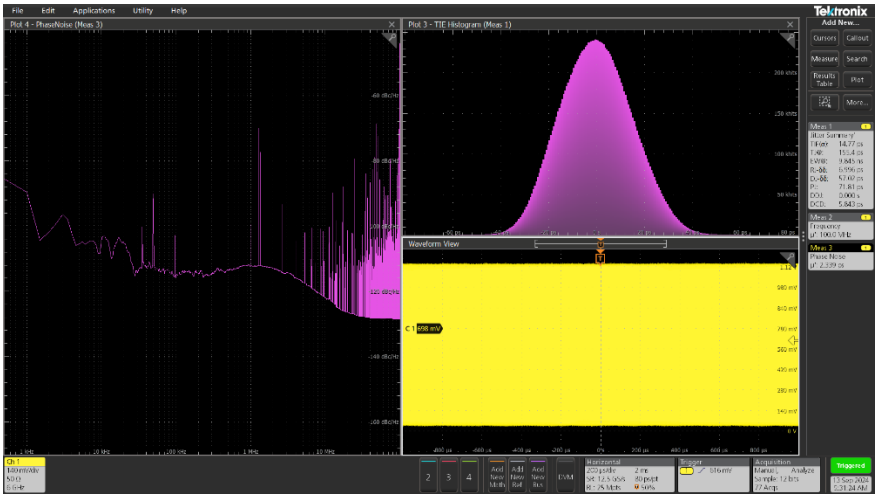

Figure 6-12. Oscilloscope screenshot of TIE spectrum and histogram of the clock signal. In yellow time domain 100 MHz signal is shown.

TIE(σ) = 14.77 ps

Clock frequency = 100 MHz

Sample Rate = 12.5 Gs/s

Record Length = 25 Mpts

B) Two outputs on the FPGA 100 MHz connected at CH-1 and 10 MHz connected at CH-3.

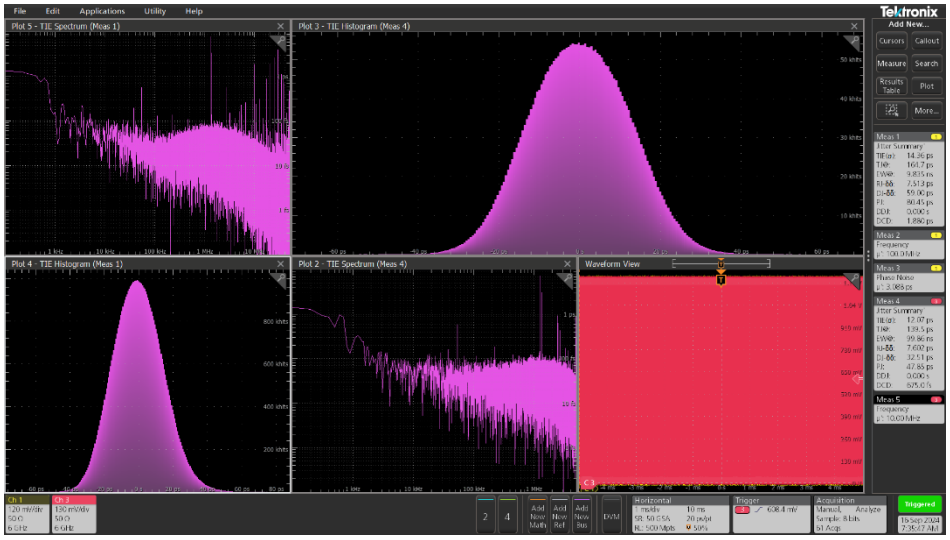

Figure 6-13. Oscilloscope screenshot of the CH1 and CH3 showing the TIE histogram, TIE spectrum and time domain signals.

TIE(σ) = 14.39 ps @ 100 MHz

TIE(σ) = 11.89 ps @ 10 MHz

Sample Rate = 50 Gs/s

Record Length = 500 Mpts

6.3.2. Jitter measurement on EVM-LMK05318B

Two outputs on the evaluation board 100 MHz connected at CH-1 and 100 MHz connected at CH-3.

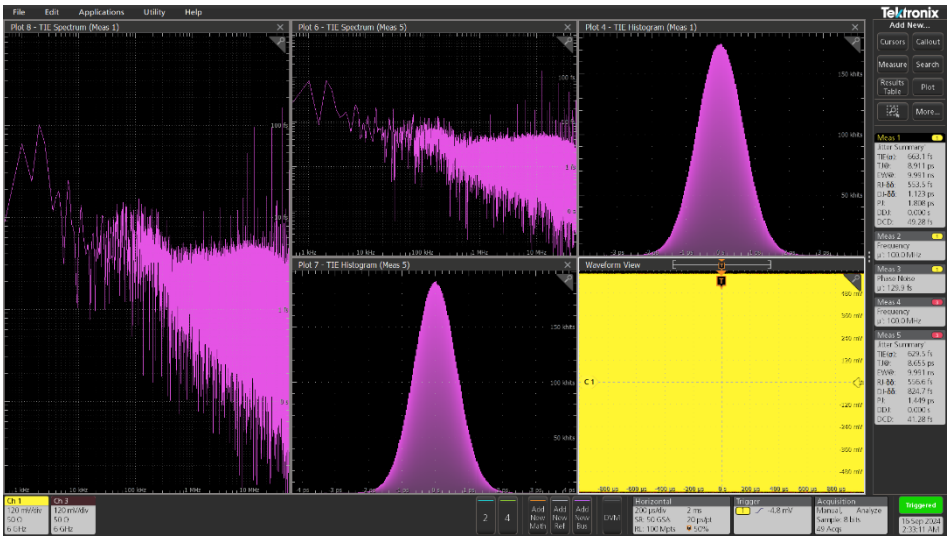

Figure 6-14. Screenshot of the TIE histogram, TIE spectrum and time domain of LMK05318B outputs.

TIE(σ) = 663.1 fs @ 100 MHz (CH-1)

TIE(σ) = 629.5 fs @ 100 MHz (CH-3)

Sample Rate = 50 Gs/s

Record Length = 100 Mpts

Additional measurements were perfromed on the second EVM-LMK05318B board (at IPQ) using the same technique based on high speed oscilloscope. Both the oscilloscope and the EVM LMK05318B board were linked to the same 10 MHz signal coming from a caesium atomic clock of the Lab.

The board was set to generate two clocks at 10 MHz and 100 MHz, respectively.

Table 6.2 reports the jitter measurement results on the 10 MHz reference signal and outputs of the EVM LMK05318B board. The results are expressed in the time domain as standard deviation of the TIE (Time Interval Error).

A galvanic insulation was also tested using a Common Mode SMD line filter (Wurth Elektronik-SL1). The filter was applied to the output signal of the EVM at the corresponding input in the oscilloscope channel (see Figure 6-15).

From the results, it is observed that the Jitter values obtained for the Board Outputs are one order of magnitude lower (~4 ps and ~2 ps for 10 MHz and 100 MHz, respectively) than the value of the 10 MHz input reference (~31 ps). This is in line with the expected “jitter cleaning” function of the LMK05318B clock generator. The 100 MHz output shows lower Jitter than 10 MHz. When this solution of galvanic insulation is used, the Jitter value increases by 20 % and 25 % for 10 MHz and 100 MHz, respectively.

Figure 6-15. Galvanic insulation mounted in a support to BNC connectors at the Oscilloscope input 3 of one of the signals from the Evaluation Board.

Table 2. Jitter values obtained for the input reference signal and the output signals of the EVM-LMK05318B board of 10 MHz

Signal	Frequence MHz	Nbr of measurements	With galvanic insulation	TIE(σ) ps
Input reference	10	10 M	---	30.7
Output 4_P	10	5 M	No	3.6
		350 K	Yes	14.4
Output 7_P	10	5 M	No	3.6
Input reference	10	5 M	---	37.2
Output 4_P	100	1 M	No	2.2
		2.6 M	Yes	11.4
Output 7_P	100	2.5 M	No	2.45

6.3.3. Jitter comparison

In order to compare the platform performance on jitter, both were measured together, connecting them as depicted in Figure 2-14 section 2.6, the FPGA provide a 10 MHz clock reference to the LMK board and a trigger signal for the oscilloscope.

A 10 MHz clock reference from the atomic clock was plugged to the oscilloscope input clock reference at its back. The setup is shown on figure 6-16 and the histogram is shown on figure 6-17 where the comparison can be observed.

This measurement result show that the LMK05318B has better jitter than the FPGA and its performance was not degraded by the FPGA clock jitter. Therefore, the LMK05318B is a good option to deliver clock and trigger signals to the project's ADC platform. As noted, the jitter of the EVM LMK05318B timing platform is about one order of magnitude lower respect to the FPGA board, because such a board is equipped with dedicated jitter cleaner circuitry.

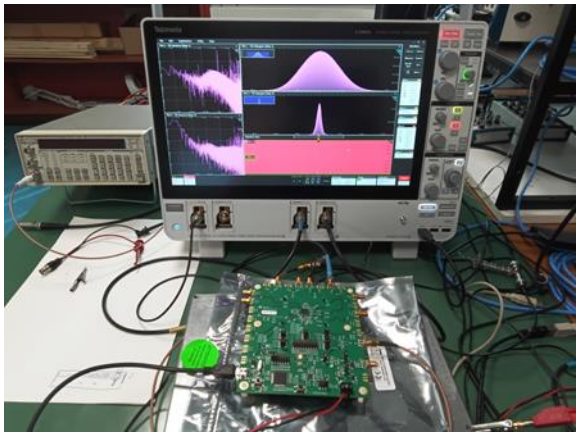

Figure 6-16. Test bench for jitter measurements on FPGA and EVM LMK05318B

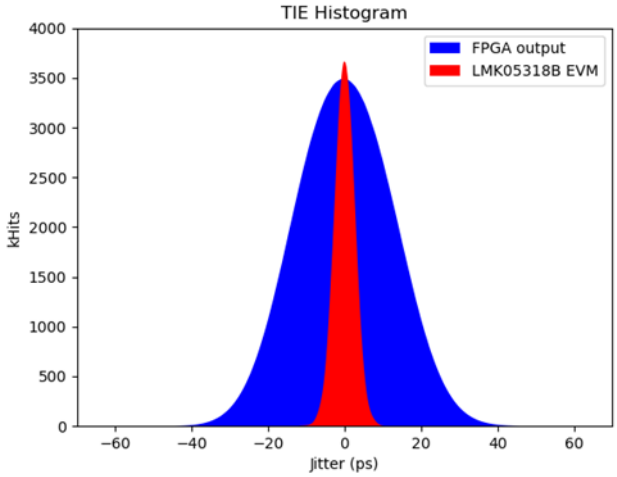

Figure 6-17. TIE histogram of LMK051318B and FPGA platforms.

6.4. Clock stability

The measurement of the clock stabilities related to the developed timing platform was performed as described in the section 5.2.

Since in all the test performed, the stability of the various clock signals was measured with instruments linked to the 10 MHz reference signals, it is mandatory to show the stability of such signals measured with the same counter used in the whole measurement campaign.

Figure 6-18 shows the Allan variation of the distributed 10 MHz reference signal, in one of the NMIs - in this case INRiM. All the measurement results were compared with the stability of the laboratory 10 MHz reference source which was derived from the internal distribution reference clock traceable to the national atomic time and frequency standard. The clock stability was measured at the output of the optical link used as galvanic isolator.

The measure was performed in the following conditions:

- 10 MHz distributed signal connected to the Ref In port of the DDS clock generator;
- DDS clock generator programmed to deliver 10 MHz signal at its output port.
- Ref out port of the DDS clock generator connected to the Ref In port of the counter;
- The CH1 channel of the counter set up to measure the 10 MHz reference clock and the CH2 set up to measure the 10 MHz provided by the DDS clock source. Gate time of the counter set to 1 s and the total number of acquisitions was about 7200 (2 h).

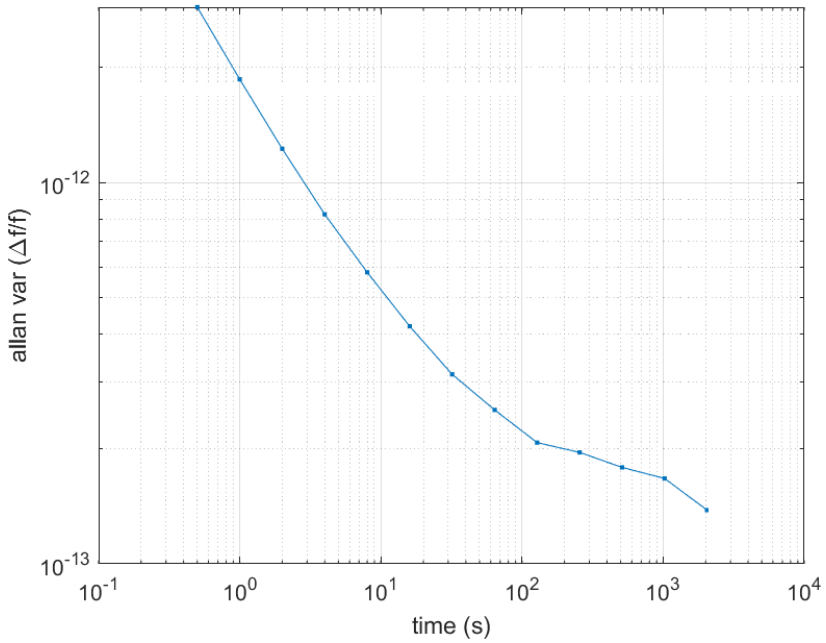

Figure 6-18. Allan variation of the 10 MHz reference distributed signal used to assess the frequency stability of the timing platform.

6.4.1. Clock stability on FPGA board

Figure 6-18 reports the measurement results of the clock signals generated with the FPGA timing platform. All the results are normalized with respect to the frequency nominal value.

The investigated frequencies were 10 MHz and 100 MHz. Even if the FPGA board has not frequency locked to an external reference clock its short time stability and accuracy is within 0.1 µHz/Hz, which in a first approximation seems very promising.

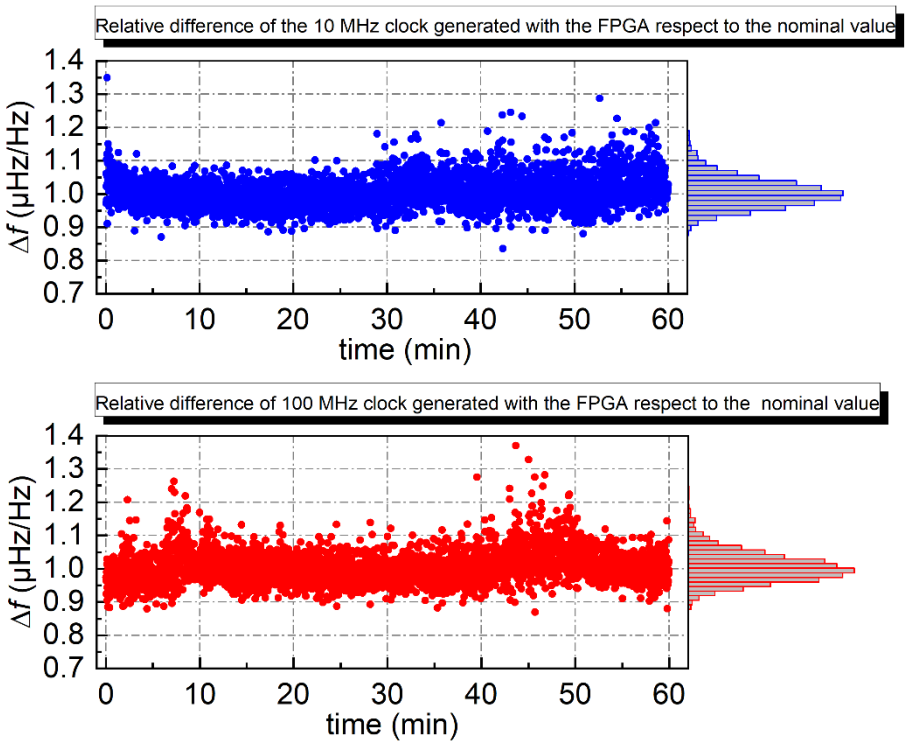

Figure 6-19. Time domain measurements showing the accuracy and time stability of 10 MHz and 100 MHz clock signals generated by means of the FPGA platform. The FPGA board is not frequency locked to an external reference clock.

6.4.2. Clock stability on EVM-LMK05318B

For the characterization of clock stability on the EVM LMK05318B, the Ref In clock port was supplied with a 10 MHz reference clock traceable to the atomic frequency standard. Two outputs of the EVM LMK05318B, and in particular Out 4 and Out 5, were set to 10 MHz and 100 MHz clock signals, respectively. The gate time of the counter was setup to 500 ms.

Figure 6-12 shows the clock stability of both signals in terms of relative difference with respect to the 10 MHz and 100 MHz nominal values. As can be shown from the figure, the accuracy of clock generated is three orders of magnitude better than the FPGA platform and the peak-to peak oscillations are lower that 0.01 ppb.

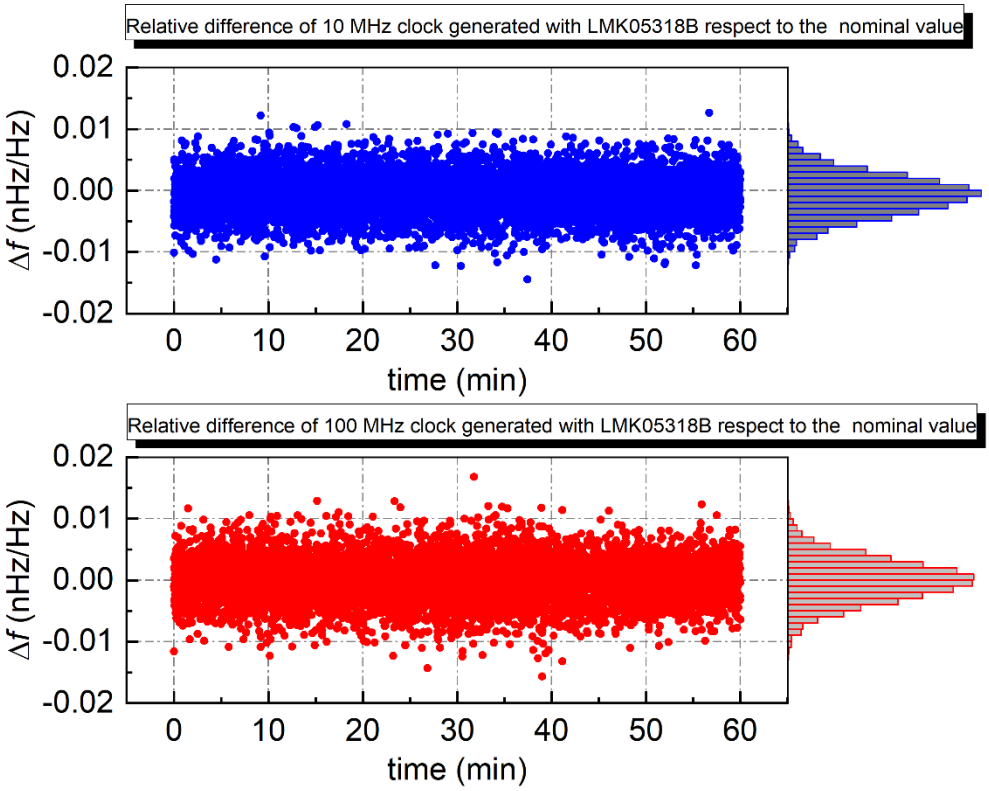

Figure 6-20. Time domain measurements showing the accuracy and time stability of 10 MHz and 100 MHz clock signals generated with the LMK05318B, which was frequency locked to an external 10 MHz reference clock

Moreover, the stability over time of the output clock signal from the EVM-LMK05318B board was measured using a Phase Noise Test Set from Timing Solutions, model TCC 5115A.

The phase difference over time between the 10 MHz reference signal from the atomic clock and a 10 MHz signal from the EVM LMK05318B was measured over a period of 16 hours.

The phase difference is shown in Figure 6-18. The first hour measurement is not displayed (warm-up of the system). For the long-term stability, it is possible to observe a very low relative frequency drift of the order of 2.6×10^{-17}.

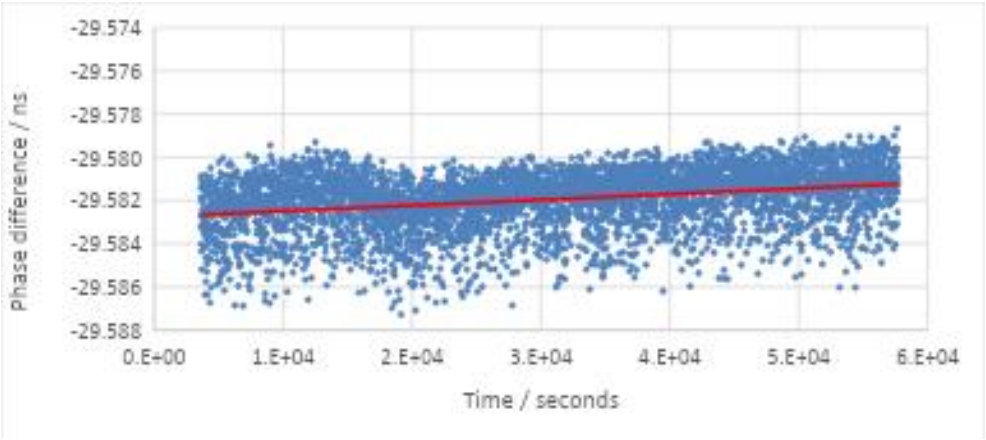

Figure 6-21. Phase difference measurements between the 10 MHz reference signal from the atomic clock and a 10 MHz signal output from the Evaluation Board.

For the short-term stability, Figure 6-19 shows the consecutive differences (residuals) of the Phase Difference where the spread of the measurements is lower than 8 ps.

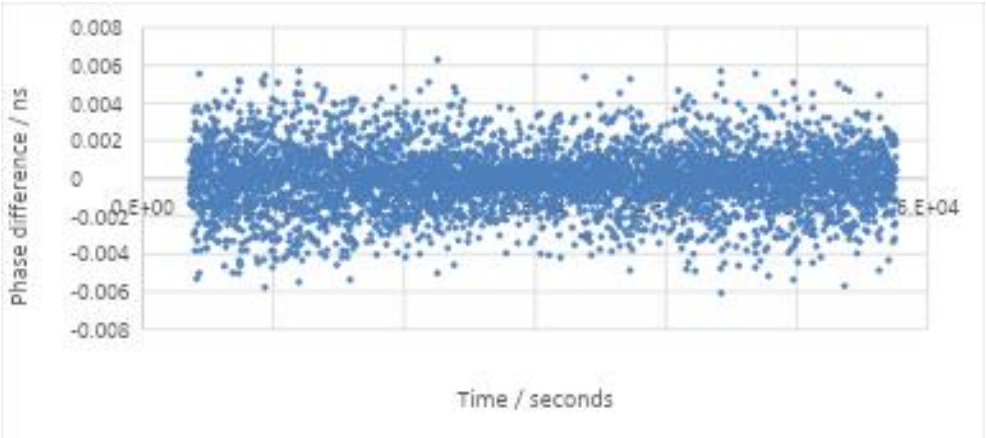

Figure 6-22. Consecutive differences (residuals) of the Phase difference measurements between the 10 MHz reference signal from the atomic clock and a 10 MHz signal output from the EVM LMK05318B.

Figure 6-20 shows the Allan Deviation as a function of *tau*. The Allan Deviation value for *tau* equal to 11 seconds (the time interval of the Phase Difference measurements) is 1.1×10^{-12}, which agrees with the specifications for the short-term stability of the atomic clock signal used (Microchip 5701A, high performance), $\leq 3.5 \times 10^{-12}$ for *tau* = 10 s.

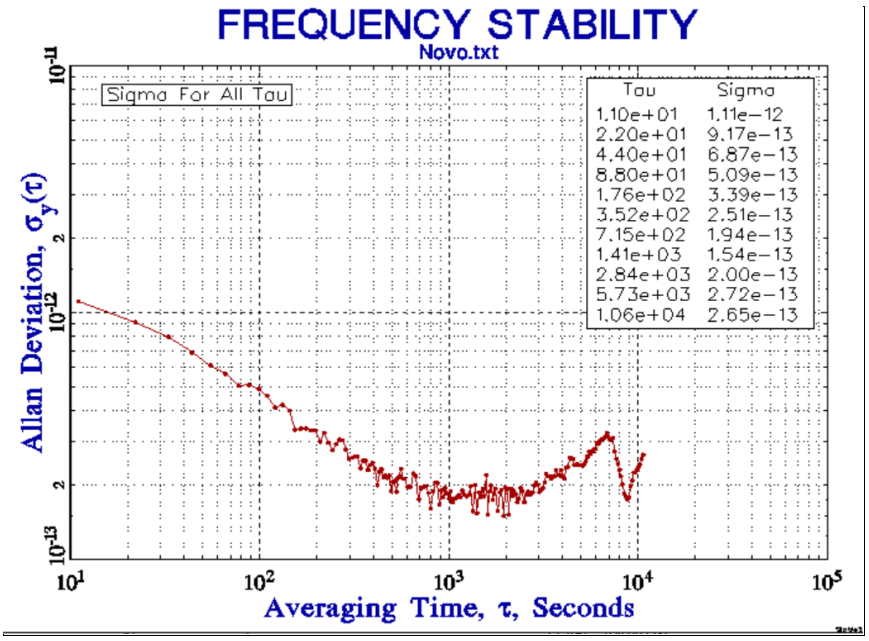

Figure 6-23. Consecutive differences (residuals) of the Phase difference measurements between the 10 MHz reference signal from the atomic clock and a 10 MHz signal output from the Evaluation Board.

6.5. Conclusions

In conclusion, the comprehensive assessment of time delay, clock stability, and jitter on the timing platform developed for a new class of high-resolution and precision ADCs confirms its suitability for demanding precision and synchronization measurement applications.

The time delay measurements demonstrated consistent and predictable latency across the system with picosecond resolution, which is essential for synchronized sampling and time-critical data acquisition. Further improvements are possible, although they would require a more complex timing hardware structure - such as the integration of programmable time delay lines. In theory, sub-picosecond time delays could be achieved, but this would necessitate significant effort and further development.

Clock stability measurements on both the FPGA-based system and the EVM LMK05318B timing platform revealed excellent short- and long-term frequency consistency. This is a crucial factor in ensuring reliable and repeatable measurements over extended periods.

Jitter analysis also confirmed low phase noise and minimal timing uncertainty, which directly impacts the effective resolution and accuracy of ADC performance. Notably, the EVM LMK05318B platform exhibited outstanding jitter performance, paving the way for its consideration or equivalent devices as a foundational synchronization device in future extended timing platforms. These future timing platforms would also incorporate the necessary hardware for comprehensive ADC driver management.

Additionally, the galvanic solutions implemented and tested in the timing platform met the project’s design requirements. Their contribution to overall jitter noise was limited to just a few picoseconds, making them highly suitable for further miniaturization and integration into the next timing platform.

Together, these results demonstrate that the current timing platform fulfills the rigorous specifications established at the project's outset, achieving an overall jitter performance of less than 50 ps. Its synchronization to external 10 MHz or 100 MHz has been demonstrated with and without galvanic isolation. It provides a robust and scalable foundation for the development of next-generation, metrology-grade digitizers aimed at high-precision and traceable measurements.