22RPT02 True8DIGIT

Deliverable D4:

Report on the assessment of at least 2 designs for novel amplifiers (composite operational amplifiers (COPAs)) for integrator and front-end digital circuitry with zero drift, extremely high gain, low noise and error below 1 ppm. This includes the development of the metrological tools to evaluate their performance and the results from this evaluation.

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Due date of the deliverable: 30 Nov 2025

Actual submission date of the deliverable: 16 Jan 2026

Confidentiality Status: PU - Public, fully open (remember to deposit public deliverables in a trusted repository)

Deliverable Cover Sheet

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European Partnership Co-funded by the European Union

METROLOGY PARTNERSHIP EURAMET

The project has received funding from the European Partnership on Metrology, co-financed from the European Union's Horizon Europe Research and Innovation Programme and by the Participating States.

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1 Summary

This document describes the work relating to the design and characterisations of composite operational amplifiers (COPAs) to be used as integrators and front-end circuitry in high precision digitisers. The most critical parameters for these COPAs are zero-drift, extremely high open loop gain, low noise, sufficient but limited bandwidth and excellent stability (sub-ppm error). Wherever relevant, these parameters have been measured and evaluated for both the COPA-based integrator and COPA-based front-end circuitry. Several measurement techniques were deployed to make the requisite measurements including a novel multi-tone method to measure harmonic distortion. It is hoped that the latter measurements will contribute to an improved version of the standard IEC 60748-4-3.

The report content flow is as follows:

In Chapter 2, the initial designs and tests of two COPA designs are described. The evaluation used both direct measurements and simulations. These two designs were inspired by the input amplifier in the HP/Agilent/Keysight 3458A digital voltmeter which constituted a benchmark for the development of COPAs described in this report.

In Chapter 3, the development of a new front-end COPA is described. The design took the designs presented in chapter 2 as a vantage point for the improvements and used best-pick linear components whenever their performances were critical in the COPA circuit. The component selection was based on a previous study within the project (Deliverable D3). This chapter also describes the simulations and measurements of the four units that were fabricated of new front-end COPA, including multitone testing. The analysis of the multitone testing of the COPAs is underway and the results are being analysed but are not included in this report.

In Chapter 4, the development and characterisation of a new COPA-based integrator is presented.

Chapter 5 presents the overall conclusions drawn from the research.

The authors wish to gratefully acknowledge the significant contribution of the project collaborators John Pickering (Metron Designs Ltd) and Vojtech Janasek (JanasCard) who contributed very significantly to the design, construction and testing of the integrator COPA described in Chapter 4.

2 Initial Designs and Tests of COPAs

2.1 Initial Design of front-end COPA

Two identical boards were designed by INTI, built by CTU and delivered to PTB for testing. These will be referred to as Board #1 and Board #2 in the following text.

Both boards are based on the schematic circuit depicted in Figure 1, the original schematic circuit can be seen at reference [3]. The circuit is based on the original input amplifier of the DVM HP3458A [2]. A photograph of the completed COPA is shown in Figure 2.

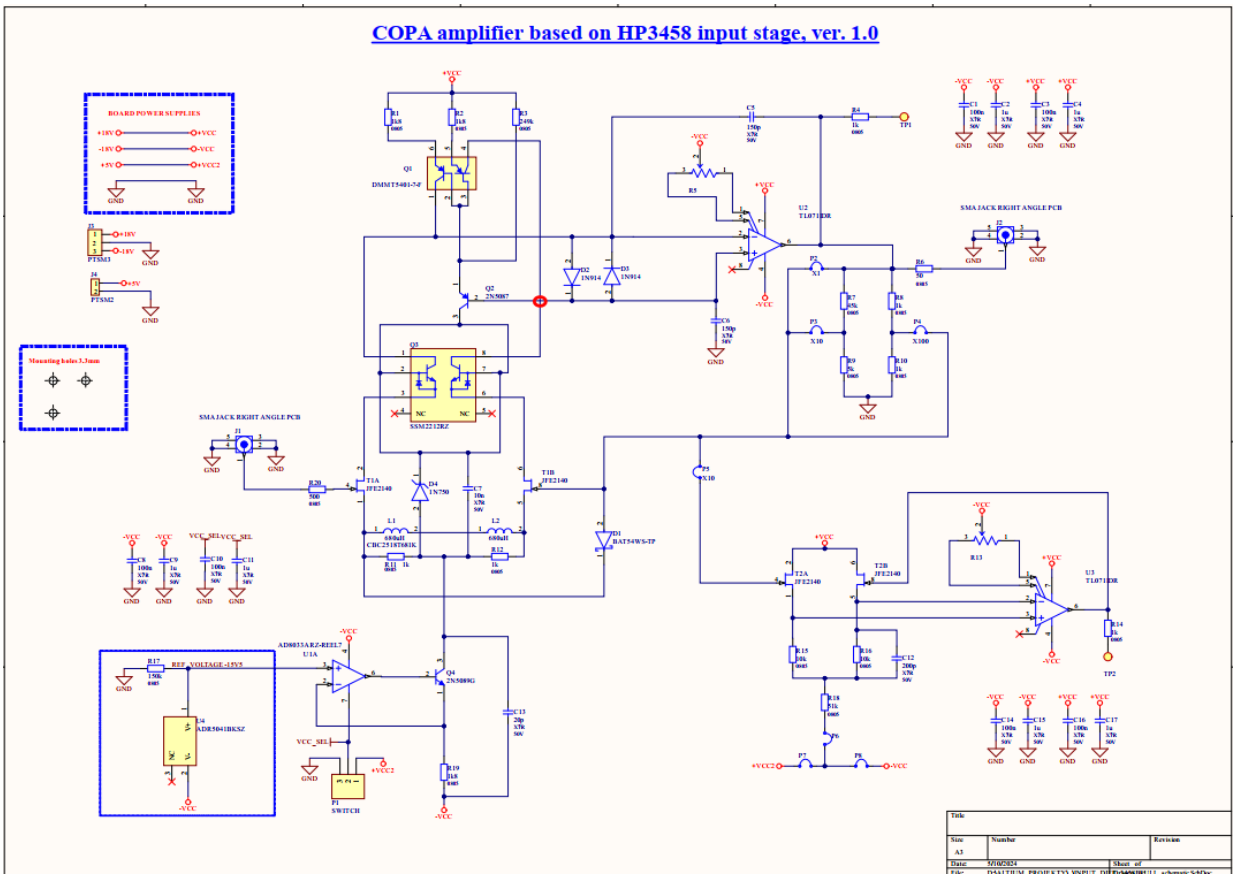


Figure 1: Schematic circuit based on LTSpice schematic ([3] and [1])

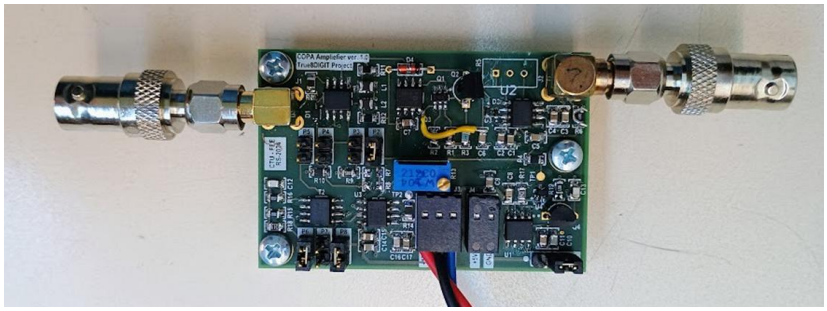
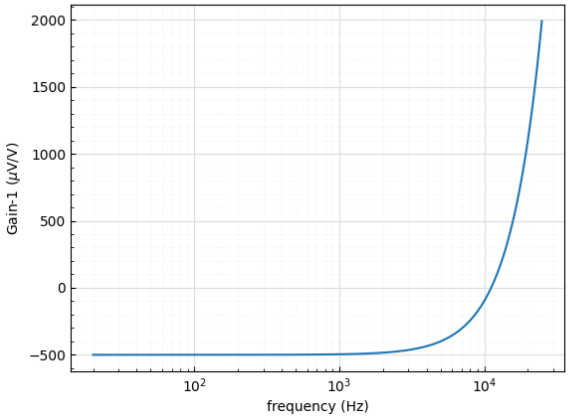


Figure 2: COPA construction

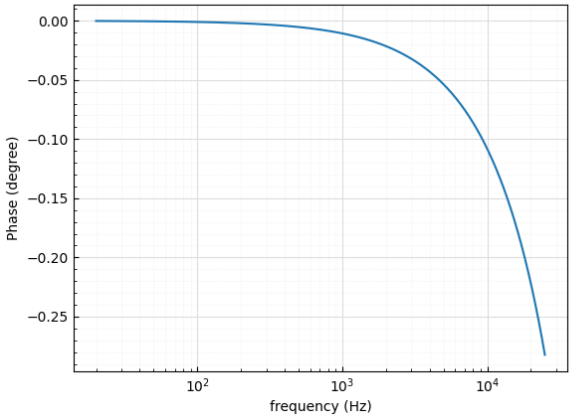
2.2 LT Spice Simulations

Simulations of the COPA performance were carried out the results are shown in the figures below.

2.2.1 Gain and Phase



(a) Simulated Gain



(b) Simulated phase displacement

Figure 3: COPA Simulated Gain and Phase

2.2.2 Simulated output spectrum and total harmonic distortion

The simulated harmonic amplitudes and phases for an input signal of 7.07 V (RMS) at a frequency of 1 kHz are given in Table 1 and the complete simulated output spectrum is shown in Figure 4

The calculated THD (dB) is equal to 0.000032% (-129.83 dB).

Table 1: Table of harmonic amplitudes for 1 kHz input signal N-Period=80 Fourier components of V(vo) DC component:1.21365e-005

Harmonic Number	Frequency (Hz)	Peak Amplitude (V)	Normalised Amplitude	Phase (◦)	Normalised Phase (◦)
1	1000	9.995	1.000	-0.01	0.00
2	2000	3.071e-06	3.073e-07	5.80	5.80
3	3000	9.070e-07	9.074e-08	-84.95	-84.94
4	4000	3.200e-07	3.202e-08	-172.64	-172.64
5	5000	1.215e-07	1.216e-08	98.86	98.87
6	6000	4.834e-08	4.836e-09	10.39	10.40
7	7000	1.979e-08	1.980e-09	-78.29	-78.28
8	8000	8.263e-09	8.267e-10	-166.94	-166.93
9	9000	3.509e-09	3.510e-10	104.07	104.07

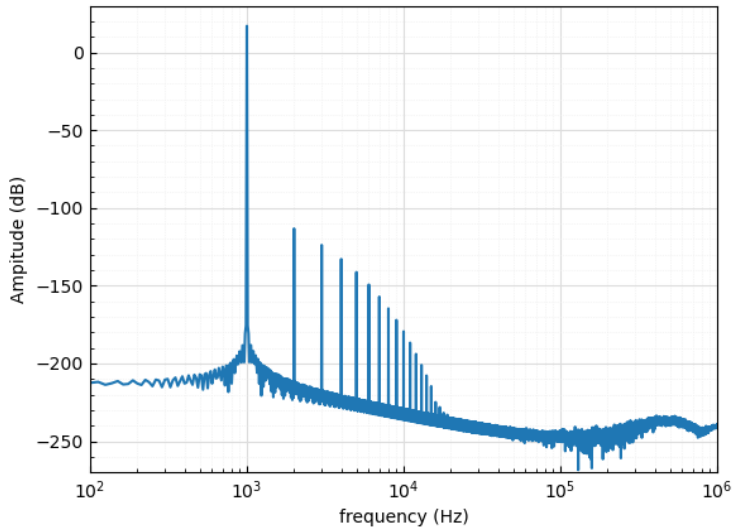


Figure 4: COPA amplifier simulated output spectrum for an input signal of 7.071 V RMS and 1 kHz frequency

2.2.3 Simulated Input Impedance

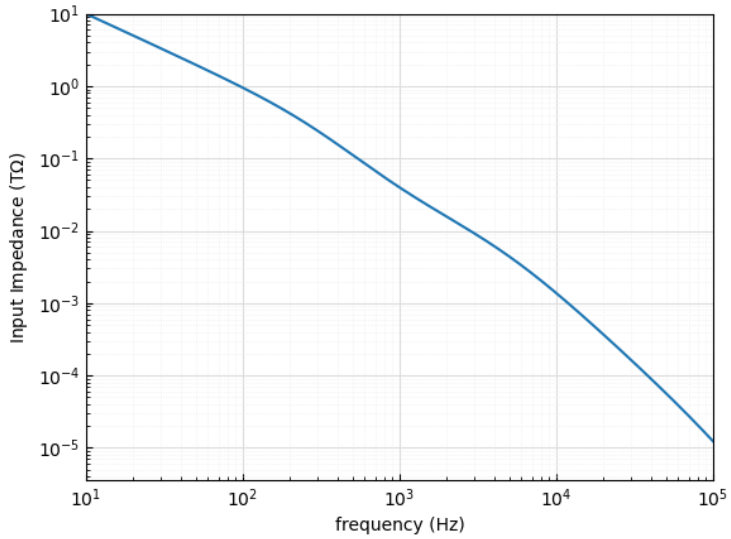


Figure 5: Simulated Input Impedance of the COPA

2.2.4 Voltage Noise

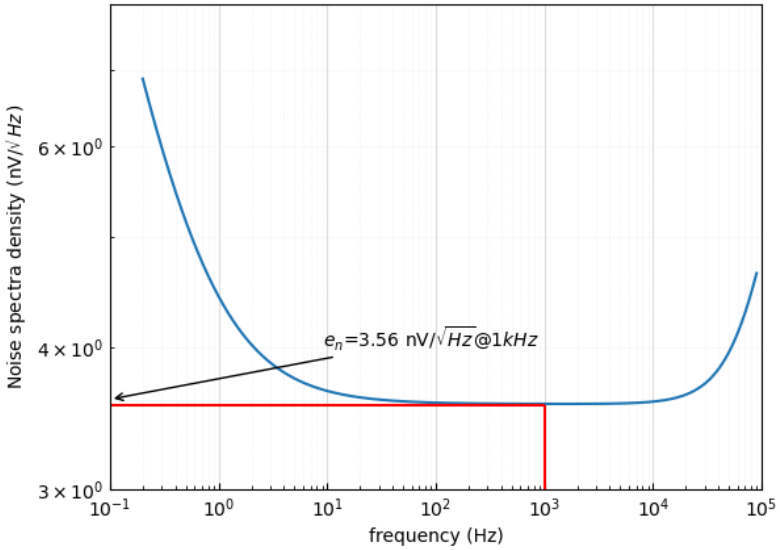


Figure 6: COPA amplifier simulated Input referred voltage noise

2.3 Testing of Board #2

The gain, phase and total harmonic distortion (THD) as a function of input frequency were measured using the Audio Precision APx555 audio analyser. Because one the of the digitizing channels is modified to have a high input impedance, the tests were run using channel two which has a selectable input impedance of 300 Ω, 600 Ω and 100 kΩ. Therefore, two sets of measurements were performed interchanging the input and output of the COPA.

A photograph of the test set-up is shown in Figure 7.

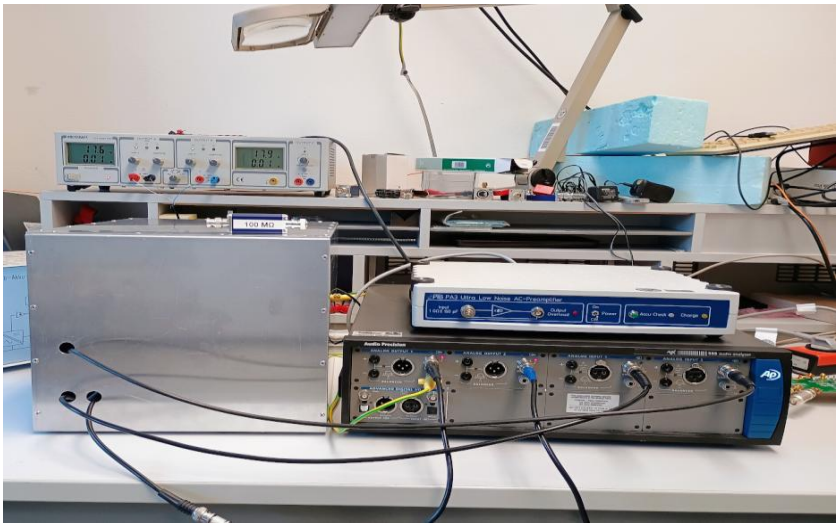


Figure 7: Photograph of test set-up

2.3.1 Gain and Phase Measurements of Board #2

A frequency sweep was set in order to measure the gain and phase of the COPA amplifier, ranging from 20 kHz down to 20 Hz in a linear sweep of 2000 points in total, keeping the signal amplitude fixed at the full scale value of 7.071 V to cover the full input range of the COPA (± 10 V).

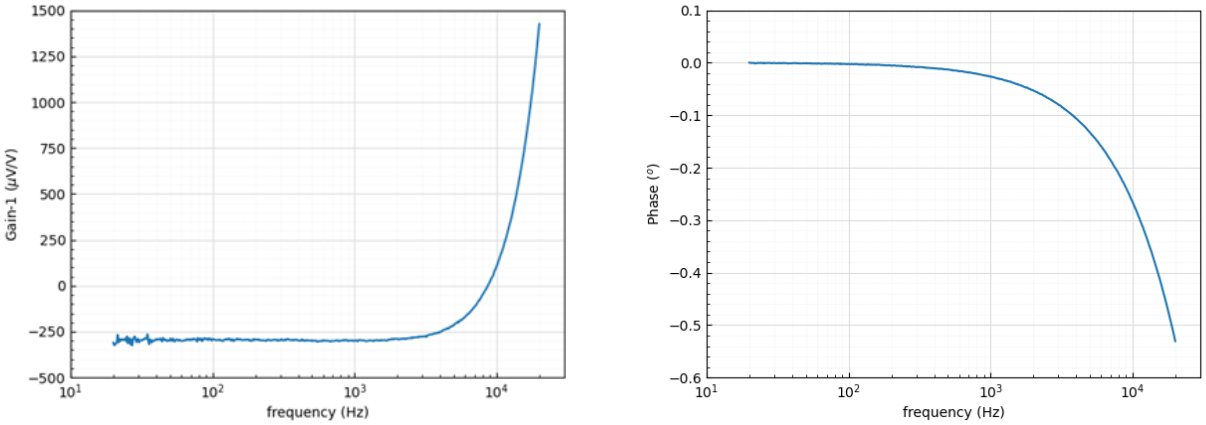


Figure 8: Gain and Phase of board #2

2.3.2 Total Harmonic Distortion Measurements

To measure the total harmonic distortion of the COPA, the APx555 channel 2 was used to measure first the input and then the output at the frequencies listed in Table 2. A full-scale amplitude signal was applied to the amplifier input, that is an RMS amplitude of 7.071 V. Then the THD was obtained covering frequencies up to the 5th harmonic unless limited by the acquisition bandwidth.

Table 2: Harmonic Distortion results for the input and output of the amplifier including the bandwidth resulting from the sampling rate used.

Frequency (Hz)	Input THD (dB)	Output THD (dB)	Bandwidth
62.5	-150.41	-143.59	DC-90 kHz
125	-147.16	-138.61	
625	-149.28	-127.87	
1000	-146.91	-123.81	
2000	-142.02	-117.43	
5000	-136.02	-108.56	
10000	-130.61	-99.00	
20000	-126.16	-88.38	
50000	-118.43	-73.15	DC-500 kHz
100000	-109.37	-46.15	

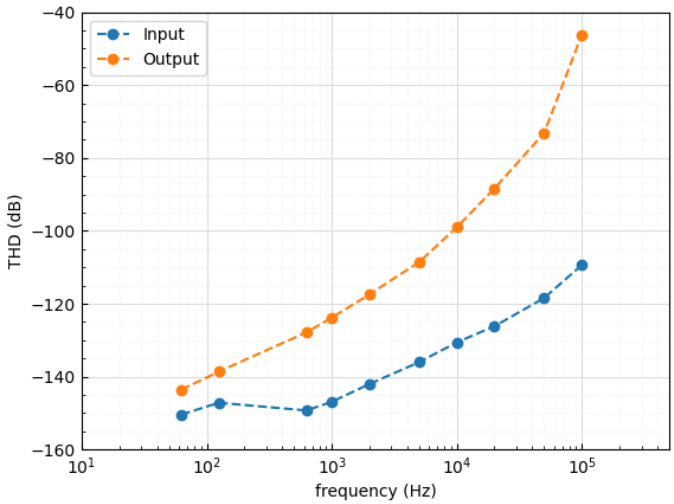


Figure 9: Total Harmonic Distortion of the COPA (Board #2) as a function of frequency

2.4 Modification and Testing of Board #1

Board #1 was modified as follows: the gain setting feedback resistors were removed to prevent performance degradation of the amplifier due to loading and leakage, therefore only Gain = 1 was possible. The bootstrap circuit was disconnected from the main amplifier output because the bootstrap signal was not routed on the PCB to avoid interference on the signal path. Figure 10 depicts the modified circuit. Note that the output includes a 50 Ω resistor in series.

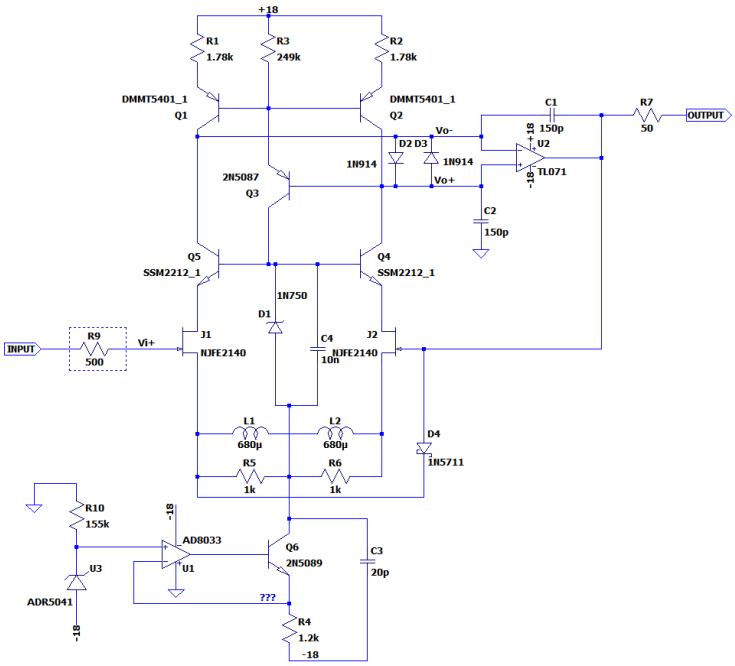


Figure 10: Schematic circuit of modified board #1

2.4.1 Gain and Phase Measurements of Modified Board #1

The gain and phase were measured for a full scale amplitude. The results are shown in Figure 11.

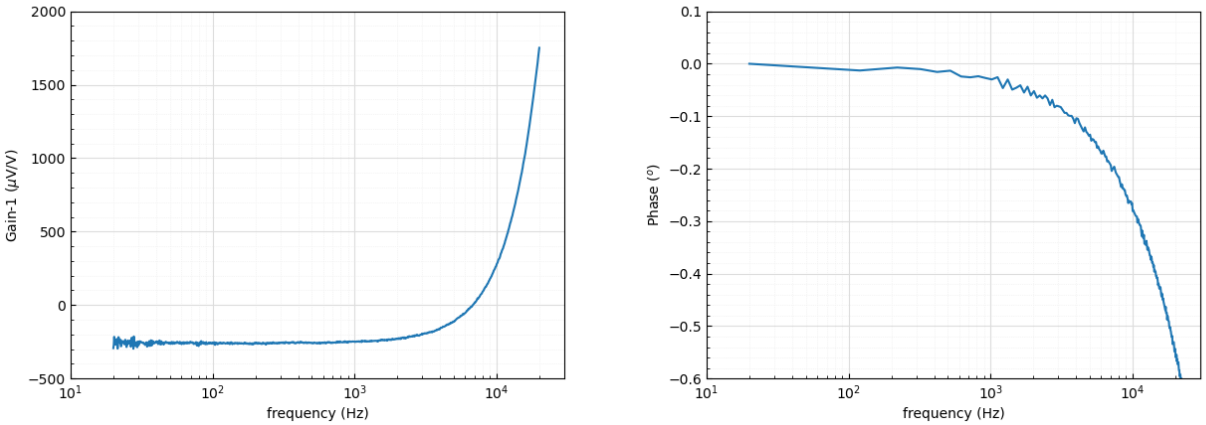


Figure 11: Measured Gain and Phase of modified Board #1 as a function of frequency

2.4.2 Total Harmonic Distortion of Modified Board #1

The total harmonic distortion of the modified Board #1 was measured as in section 2.3.1 above, covering the frequency range up to the 5th harmonic unless limited by the acquisition bandwidth. The results are shown in Table 3 and Figure 12.

Table 3: Harmonic Distortion results for the input and output of the amplifier including the bandwidth resulting from the sampling rate used.

Freq (Hz)	Input THD (dB)	Output THD (dB)	Bandwidth
62.5	-151.22	-148.51	DC-90 kHz
125	-147.47	-144.36	
625	-151.36	-137.55	
1000	-147.92	-134.14	
2000	-142.79	-127.30	
5000	-135.40	-115.48	
10000	-130.60	-103.88	
20000	-125.85	-92.42	
50000	-118.87	-76.48	DC-500 kHz
100000	-109.63	-45.13	

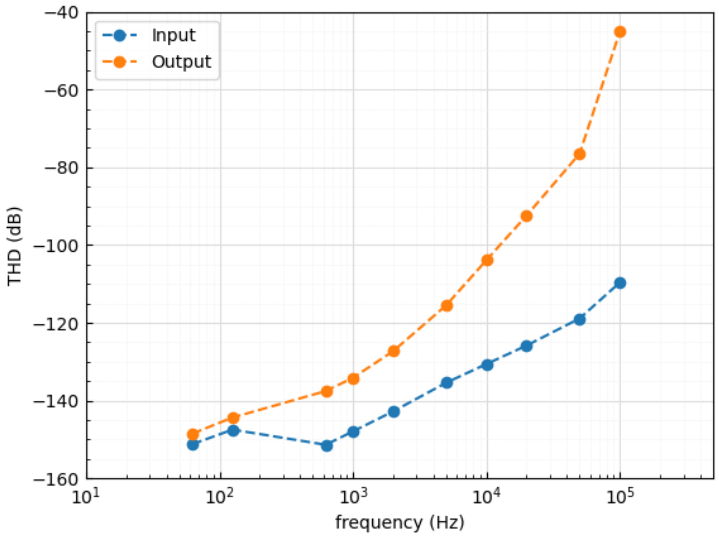


Figure 12: Total Harmonic Distortion of the circuit in figure 10 as a function of frequency

2.4.3 Comparison of Total Harmonic Distortion of modified Board #1 and Board #2

A comparison of the THD of the modified Board #1 and Board #2 is shown in Table 4 and Figure 13. It is clear to see the improvement that resulted from when removing the gain resistors and disconnecting the bootstrap circuit.

Table 4: Total Harmonic Distortion differences. THD 1 - THD 2

Freq (Hz)	Diff. (dB)
62.5	4.92
125	5.75
625	9.68
1000	10.33
2000	9.87
5000	6.92
10000	4.88
20000	4.04
50000	3.34
100000	-1.02

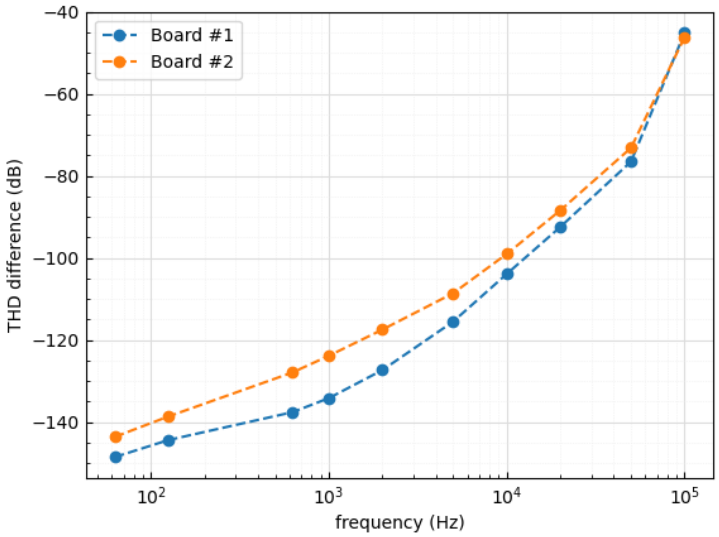


Figure 13: Comparison of THD of modified Board #1 and board #2

2.4.4 Harmonic distortion at different input signal levels and frequencies

To characterize the harmonic distortion of board #1 at different input signal frequencies and levels the THD was measured at input frequencies of 5, 10, 20, 50 and 100 kHz at input signal levels in the range 0.2 V to 7.701 V (RMS). The results are shown in Figure 14.

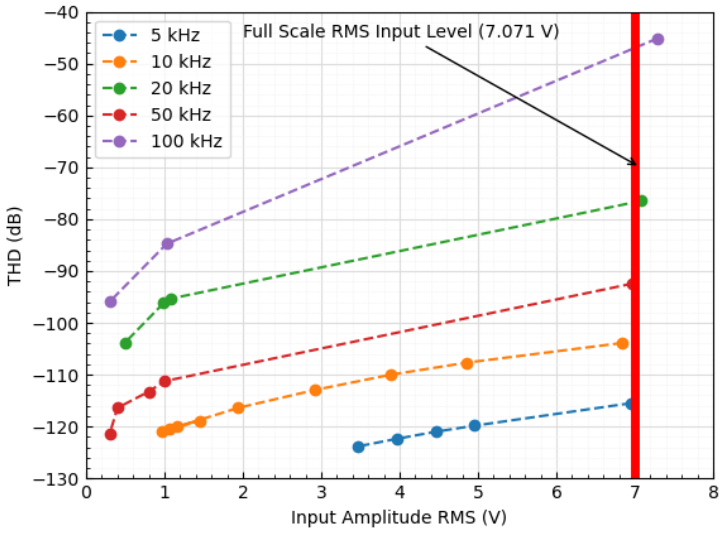
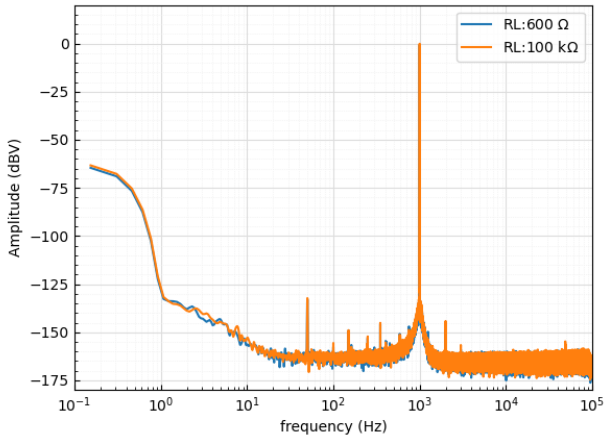


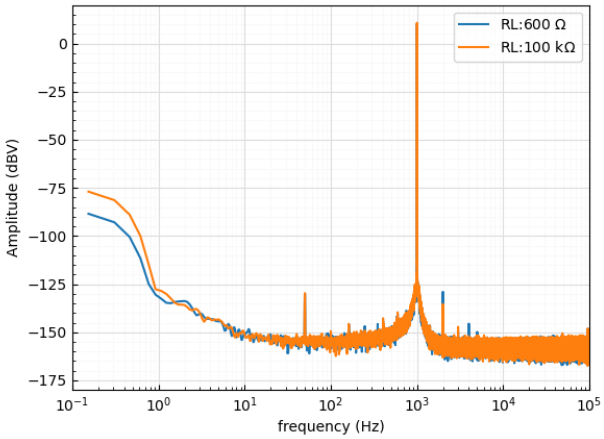
Figure 14: Total harmonic distortion vs input signal level for board #1

2.4.5 Loading effect on the output spectrum

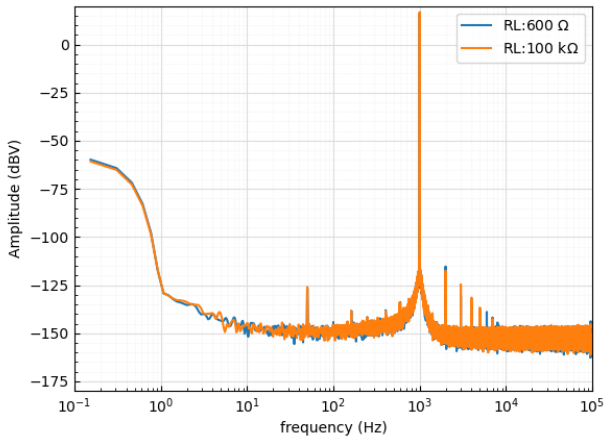
To evaluate the effect of loading at the output of the amplifier after the 50 Ω series resistor, the input impedance of the APx555 digitizer was changed between 600 Ω and 100 kΩ while a 1 kHz pure sinewave signal was applied to the amplifier input. The resultant spectra of the are shown in Figure 15 (a) to (c) for input amplitudes of 1 V, 3.5 V and 7.07 V (RMS) respectively.
The amplitudes of the harmonics are given int Table 5, Table 6 and Table 7. The intermediate level was chosen to match the full-scale value of the AD4630-24 SAR whose performance was analysed in other parts of the project.



(a) Input Amplitude = 1 V (RMS)



(b) *Input Amplitude = 3.5 V (RMS)*



(c) *Input Amplitude = 7.07 V (RMS)*

Figure 15: COPA output spectra for different loads and input amplitudes

Table 5: Output levels at different frequencies for an input amplitude 1 V at 600 Ω and 100 kΩ loads

Harm. #	Freq (Hz)	100 kΩ		600 Ω		Delta
		Amp (dB)	Amp	Amp (dB)	Amp	
fo	1000.20	-0.12816	0.985353 V	-0.82809	0.909066 V	76 mV
2fo	2000.20	-144.15	62 nV	-149.05	35.3 nV	26.7 nV
3fo	3000.30	-156.63	14.7 nV	-159	11.2 nV	3.52 nV
4fo	4000.10	-162.09	7.86 nV	-162.08	7.87 nV	-4.48 pV

Table 6: Output levels at different frequencies for an input amplitude 3.5 V

Harm. #	Freq (Hz)	100 kΩ		600 Ω		Delta
		Amp (dB)	Amp	Amp (dB)	Amp	
fo	1000.15	10.748	3.446672 V	10.049	3.180168 V	267 mV
2fo	2000.15	-135.39	170 nV	-128.985	355 nV	-185 nV
3fo	3000.30	-147.197	43.7 nV	-149.577	33.2 nV	10.5 nV
4fo	4000.46	- 154.121	19.7 nV	-145.531	52.9 nV	-33.2 nV

Table 7: Output levels at different frequencies for an input amplitude 7.07 V

2.3.	Freq (Hz)	100 kΩ		600 Ω		Delta
		Amp (dB)	Amp	Amp (dB)	Amp	
fo	1000.15	16.859	6.965463 V	16.158	6.425398 V	540 mV
2fo	2000.15	-117.537	1.33 µV	- 115.307	1.72 µV	- 389 nV
3fo	3000.30	- 124.607	0.588 µV	- 130.852	0.287 µV	302 nV
4fo	4000.46	- 131.498	0.266 µV	- 135.219	0.173 µV	92.7 nV

The load dependence shows good agreement with the 50 Ω resistor. The values derived from the measurements are 50.7, 50.6 and 50.8 Ω.

2.4.6 Noise Level Measurements

Since the input noise of the APx555 is comparable to the expected noise from the COPA, PTB's PA3 ultra-low noise AC pre-amplifier was used to amplify the output noise of the COPA. The measurement set-up, shown in Figure 16 was connected as follows: the COPA amplifier input was shorted, and the output connected to the PA3 pre-amplifier. Both the COPA and the pre-amplifier were powered by batteries. The PA3 output was connected to CH2 of the APx555 analyser. The AP software was configured to sample the data at 192 kHz (bandwidth DC to 90 kHz), averaging 64 windows of 1.2 M data points with rectangular windows (no window function on the software). PA3 nominal gain = x60, measured gain = x59.2 and voltage noise = 0.53 nV/√ Hz. Figure 17 shows the amplitude spectrum density of the measured signal divided by the PA3 gain factor, The PA3 voltage

noise level does not affect COPA noise measurements. The equivalent input voltage noise level of the COPA at 1 kHz was determined to be 3.9 nV/√ Hz.

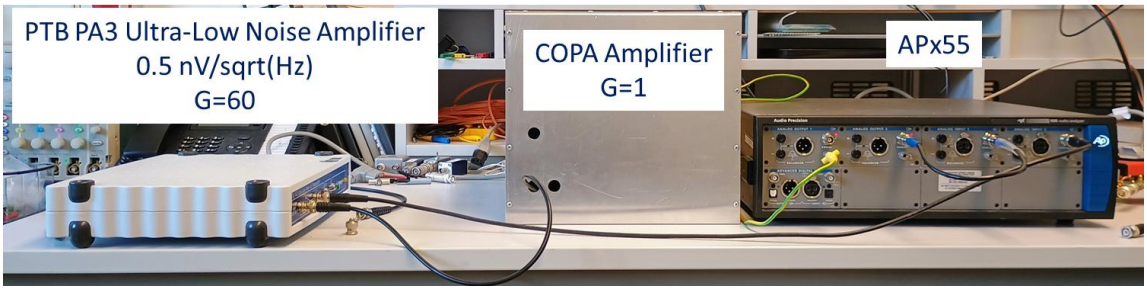


Figure 16: Noise measurement setup, using the PTB PA3 Ultra-low noise amplifier to amplify the noise from the COPA to be detected by the APx555

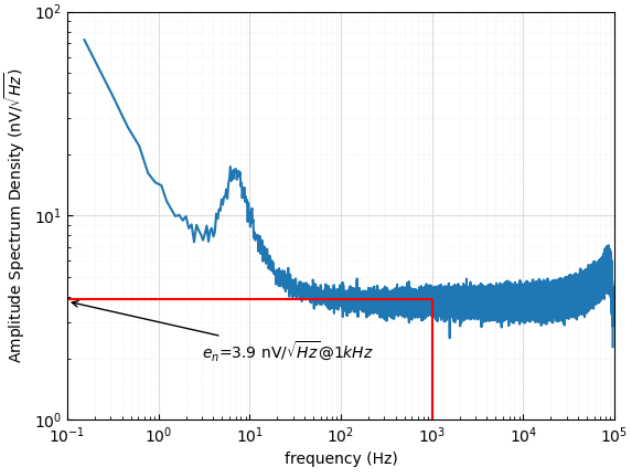


Figure 17: COPA amplifier board #1 input voltage noise

To measure the equivalent input current noise the short circuit was replaced by a screened 100 MΩ resistor Figure 18 shows the amplitude spectrum density of the COPA output signal divided by the PA3 gain and the value of the 100 MΩ resistance. The equivalent input current noise level at 1 kHz was determined to be 6.6 fA/√Hz.

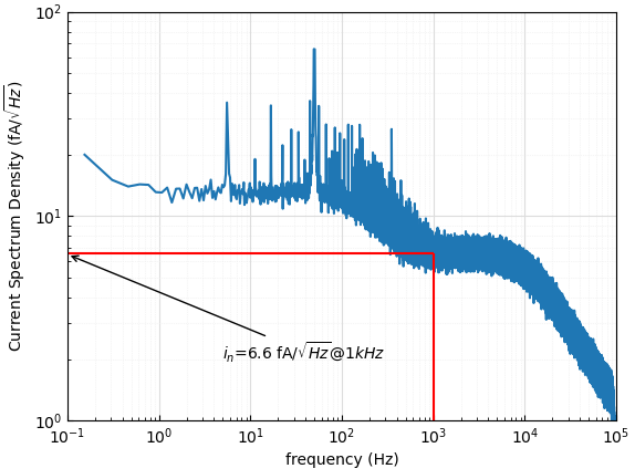


Figure 18: COPA amplifier board #1 input current noise

2.4.7 Input Impedance Measurement

The input impedance was measured by adding an external 100 MΩ in series between the output of the APx555 generator and the input of the COPA to form a voltage divider with the input impedance of the COPA, then the input impedance is calculated as:

$$Z_i = R_s \cdot \left(\frac{V_o}{V_o - V_i}\right)$$

where R_s is the 100 MΩ resistor value, V_o is the COPA output voltage and V_i is the COPA input voltage.

An input voltage of 5 V RMS was applied to the input, and then the amplifier input and output were measured by the AP on channel 2 in two steps: i) performing a frequency sweep from 20 Hz to 20 kHz (digitizer BW 90 kHz), ii) a second frequency sweep from 10 kHz up to 100 kHz (digitizer BW 250 kHz). Results are shown in Figure 19 and Table 8. The measured low frequency input impedance value was 920.31 MΩ. Modelling the input impedance as an RC parallel circuit and performing a fitting to zero frequency an input resistance, R_i, of 1.364 GΩ and an input capacitance, C_i of 6.38 pF were determined.

Table 8: Board #1 Input Impedance

Frequency (Hz)	Z_i (MΩ)
20	920.31
1000	18.56
10000	2.22
20000	1.50
50000	1.20
100000	1.17

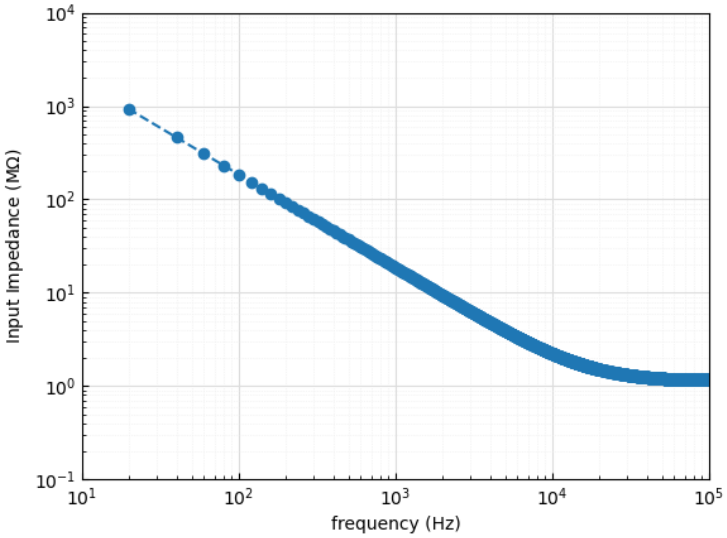


Figure 19: Board #1 input impedance in the frequency range from 20 Hz up to 100 kHz

Table 9: Input RC

R_i (GΩ)	C_i (pF)
1.364	6.38

2.4.8 Settling Time Measurements

To obtain the amplifier settling time, a function generator (Keithley 3390) with a specified rise/falltime of less than 10 ns was used as source. The amplifier input and output were captured using a high bandwidth, high-resolution digital oscilloscope (LeCroy, HDO4054) enhancing its resolution by +3 bits using a built-in facility. A square wave signal with a peak-to-peak amplitude of 10 V and frequency of 10 kHz was used to observe and calculate the settling time. In addition, the rise-time and fall-time were calculated. Figure 20 shows a photograph of the measurement set-up.

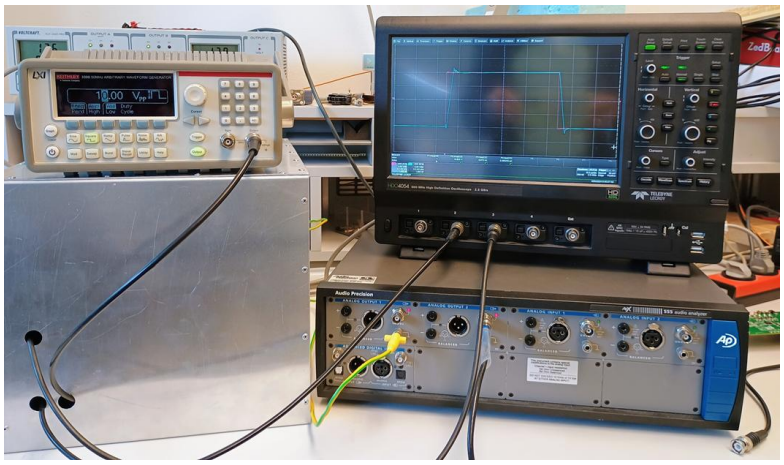
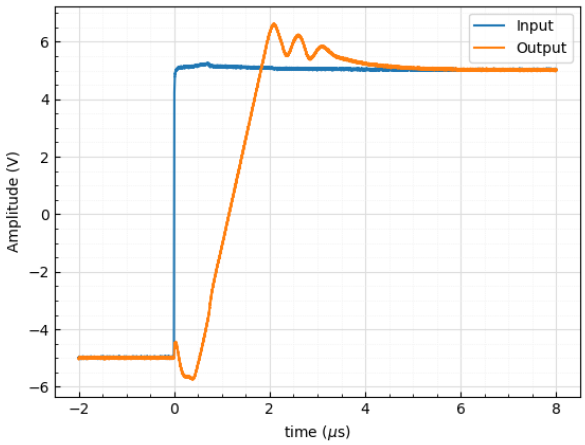


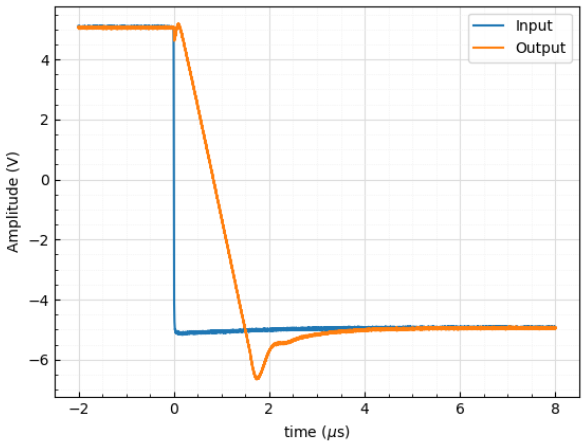
Figure 20: Setup used to measure the input settling time of the COPA

The measured waveforms are shown in Figure 21 (a) to (d). As shown in Figure 21(a) and Figure 21(b) the observed rise and fall times (10% to 90%) which are limited by the slew rate of the amplifier's second stage, were both 1 µs. The settling time of 8 µs can be seen in Figure 21(d).

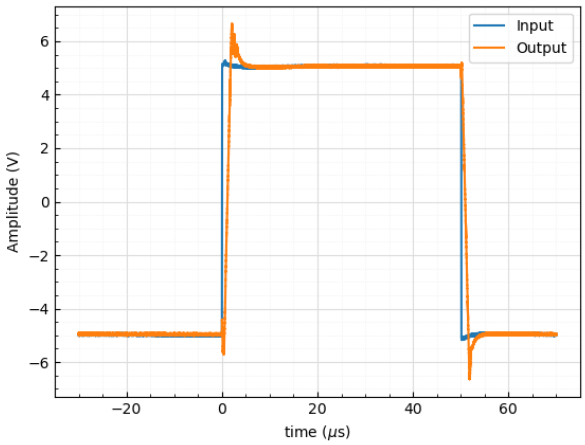
It was concluded that an improved performance of the COPA could be achieved by replacing the TL071 op-amp by an op-amp with a higher slew rate.



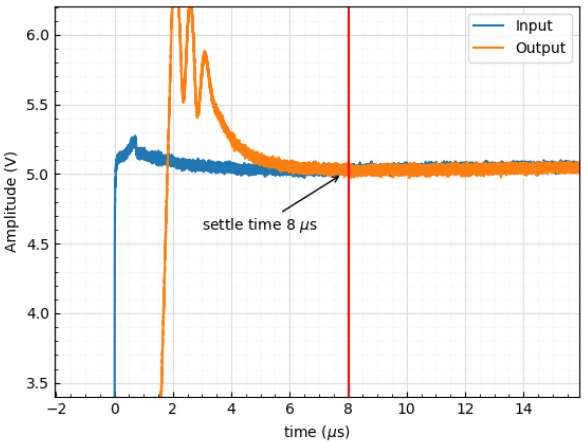
(a) Amplifier Rise time determined to be 1 µs



(b) Amplifier Fall time determined to be 1 µs



(c) Half period of the square wave signal



(a) Measured settling time to 0.17 % in 8 µs

Figure 21: Rise-time, fall-time and settling time results

2.5 Modification of Board #2 – replacement of TL071 by OPA1655

To study the performance of the COPA with a high slew rate op-amp such as the OPA1655, board #2 was modified in the same manner as board #1 (e.g, removing the feedback resistors and the bootstrapping circuit). Then the original second stage op-amp, TL-071, was replaced by the OPA 1655.

The total harmonic distortion of the modified board #2 was measured at frequencies 1 kHz, 5 kHz and 10 kHz with a signal amplitude of 7.071 V (RMS). Results are shown in Table 10and Figure 22.

Table 10: THD of board #2 with OPA1655. Column with heading Ciff stands for the THD difference from board # 1

Freq (Hz)	THD of board #2 (dB)	Diff. (dB)
1000	-123.547	-10.59
5000	-108.116	-7.37
10000	-99.065	-4.81

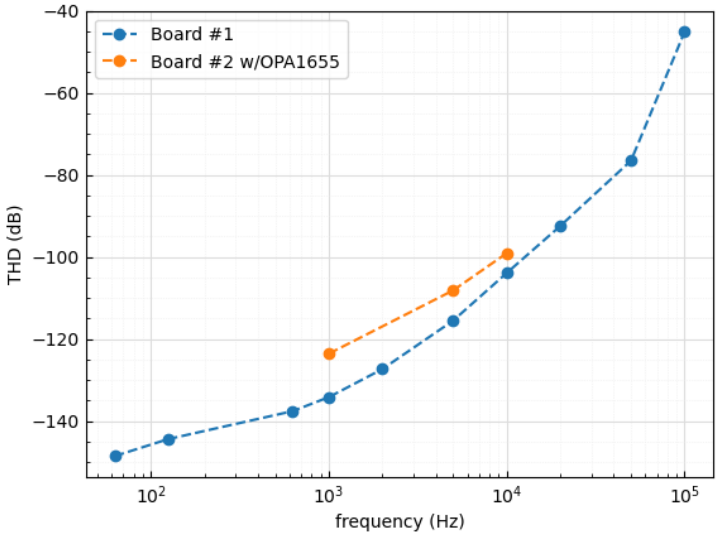
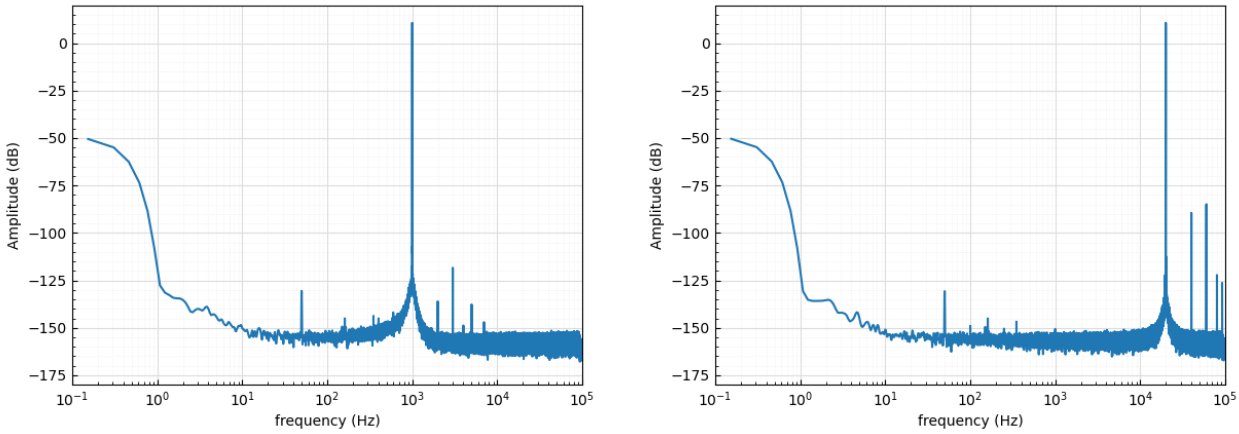


Figure 22: THD Board #1 and Board # 2 comparison

To measure the THD following OPA1655 datasheet specifications , its spectrum was calculated for input signals of 3.5 V RMS at 1 kHz and 20 kHz. The resulting spectra are depicted in Figure 23(a) and Figure 23(b). The measured THD were -128.96 dB at 1 kHz and -94.27 dB at 20 kHz degrading the performance of the COPA (see Table 2)



(a) Board # 2 spectrum 1 kHz 3.5 V RMS *(b) Board # 2 spectrum 20 kHz 3.5 V RMS*

Figure 23: Output spectra of board # 2 with OPA1655 instead of TL071

2.6 Summary of performance of input stage COPA (Version 1)

Table 11 shows a summary of the measured features of the first version of the COPA intended for use as the input stage of the precision digitiser.

Table 11: Features measured results summary

Feature	Result
Gain @ 1 kHz	0.999750 V/V
THD @ 1 kHz	-134.14 dB
en @ 1 kHz	3.9 nV/√ Hz
in @ 1 kHz	6.6 fA/√ Hz
Zi (f=20 Hz)	1.364 GΩ // 6.38 pF 920.31 MΩ
settling time	(0.17 %) (8.0 µs)
rise time (10 % - 90 %)	1.0 µs
fall time (10 % - 90 %)	1.0 µs

References:

[1] CTU. Copa pcb project. Altium-Project-COPA-Design, 2024. [Online; accessed 2024].

[2] Hewlett Packard. HP 3458 Multimeter Component Level Information Packet. Technical report, Hewlett Packard, 2001.

[3] INTI. Copa schematic circuit. InputDiff-3458A-FULL-RJI-03-TP, 2024. [Online; accessed 2024].

[4] Texas Instrument. OPA 1655 SoundPlus ultra-low noise and distortion, Burr-Brown single audio operational amplifier. OPA1655, 2022.

[5] Texas Instrument. TL07xx Low-Noise FET-Input Operational Amplifiers. TL071, 2023.

3 Development of new front-end COPA

3.1 Introduction

Following the design and characterisation process of the modified HP3458A input COPA described in chapter 2, a new COPA design was proposed by INTI and Janascard. The PCB design was then made by JV and four PCBs were produced by CTU. For characterisation and comparisons, one board was sent to IPQ, one to INRIM and two to JV. JV received two boards to allow for the multi-tone testing.

3.2 New COPA Schematic

The new design was made from the previously modified HP3458A input COPA and adding a boot-strap technique to form a shield for the signal path in the COPA. Figure. 24 shows the schematic of the new COPA design, where a voltage follower has been used to realise the bootstrap guard for the signal path. The source and drain resistors on the input stage of the COPA was determined to be critical circuit elements to ensure good gain stability and low drift, so it was decided to use Vishay metal-foil resistor networks in these instances.

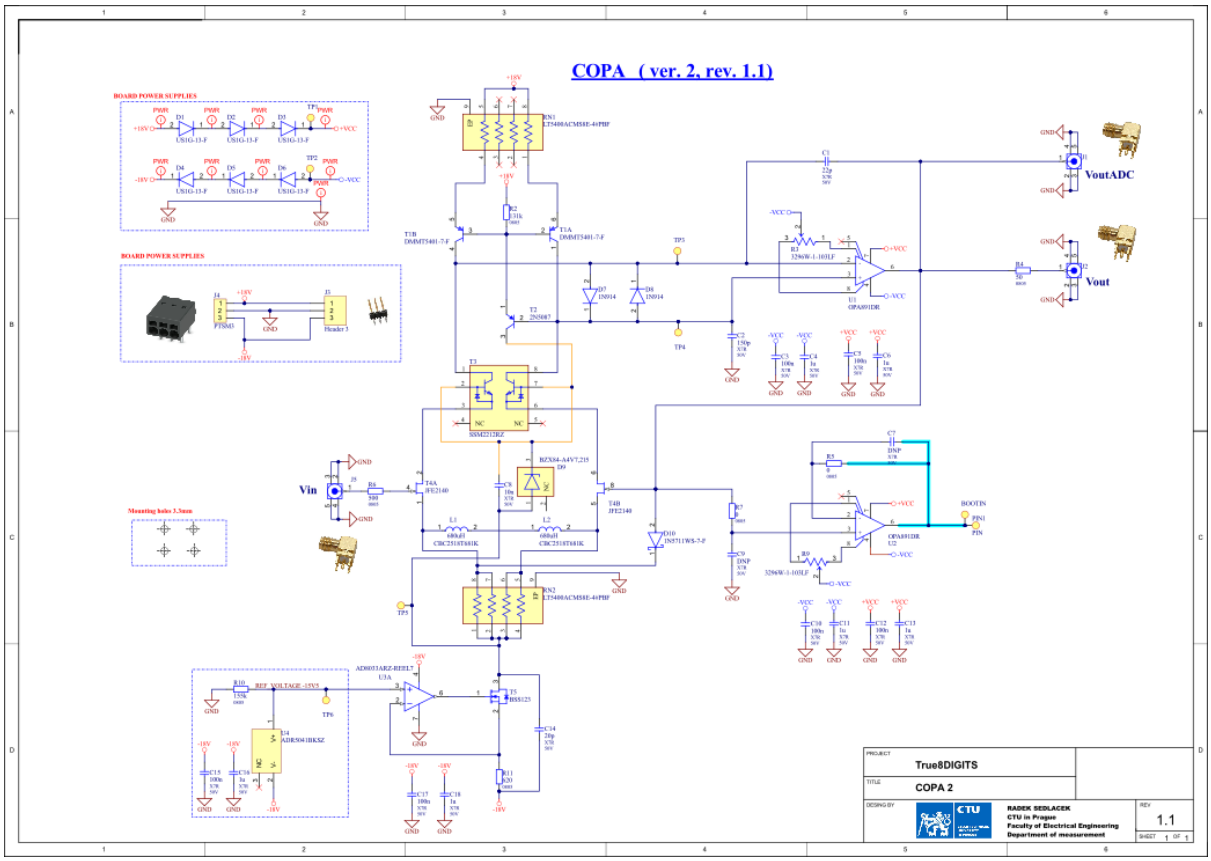


Figure 24 Schematic of the new COPA design

3.3 New COPA PCB design

The PCB designs of the new COPA was made in ALTIUM, of which four boards were manufactured. Board #1A was sent to IPQ and thence to INRIM, board #2A was sent to PTB and boards #3A and #4A were both sent to JV. The PCB layout can be seen in Figure. 25.

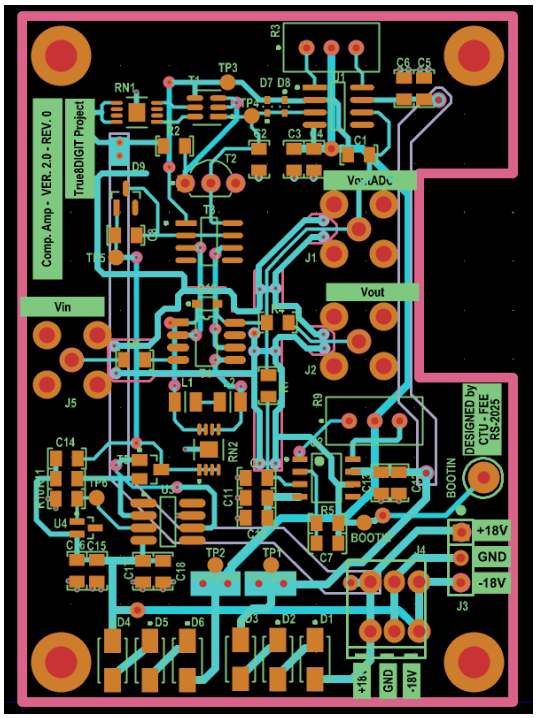


Figure 25 PCB layout of the new COPA design

Figure 26 Fabricated COPA of new design

3.4 Simulations

The gain and phase were simulated as a function of frequency, and THD was simulated at for 1 V RMS and 7.071 V RMS input voltage, both at 1 kHz. Input impedance and input noise were also simulated as functions of frequency.

3.4.1 Gain and phase simulation

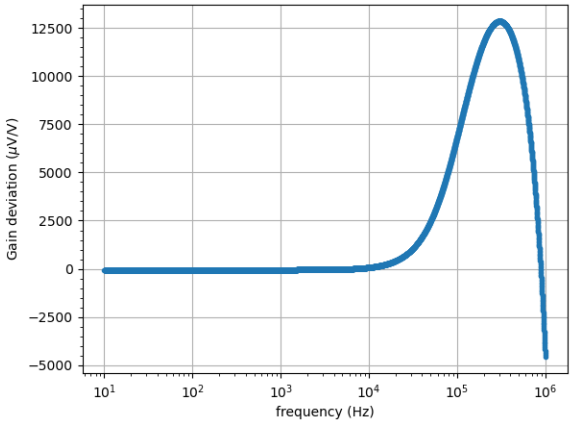


Figure 27 Simulated gain deviation vs frequency

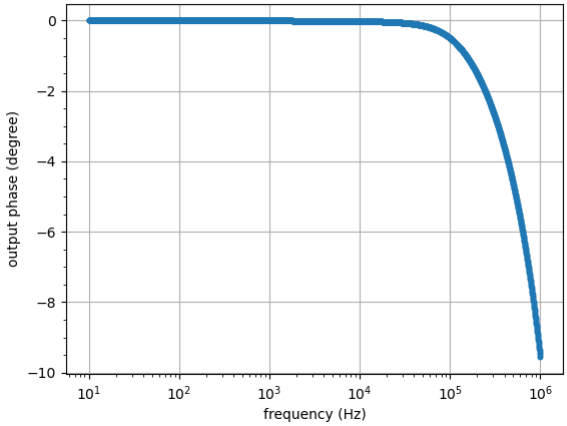


Figure 28 Simulated phase vs frequency

3.4.2 Total harmonic distortion simulation

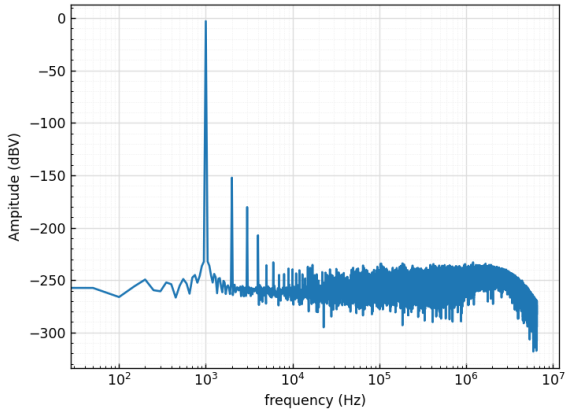


Figure 29 COPA amplitude simulated output (1 V RMS @ 1kHz)

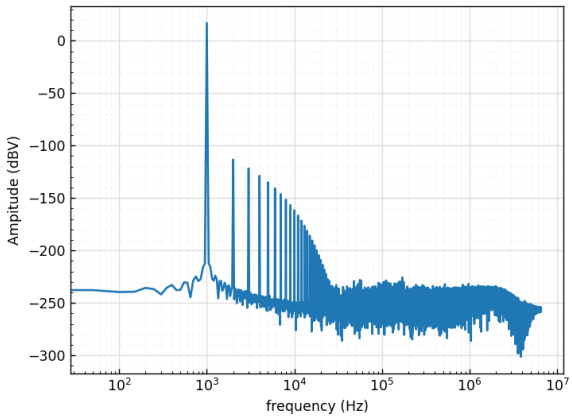


Figure 30 COPA amplitude simulated output (7.07 V RMS @ 1 kHz)

3.4.3 Input impedance simulation

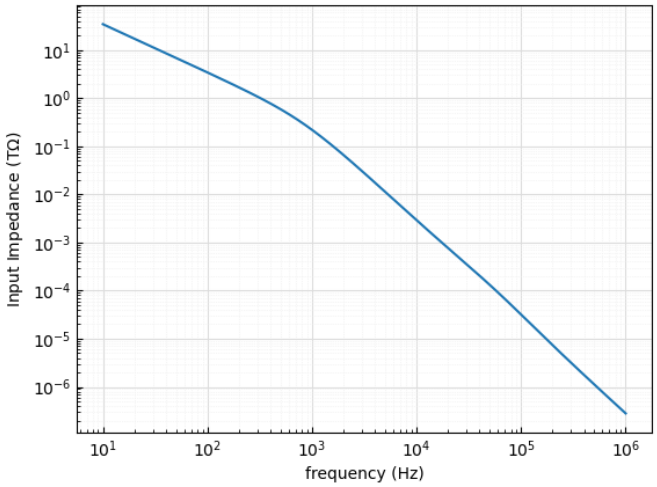


Figure 31 COPA V2 amplifier Input impedance vs frequency simulation

3.4.4 Voltage Input referred noise simulation

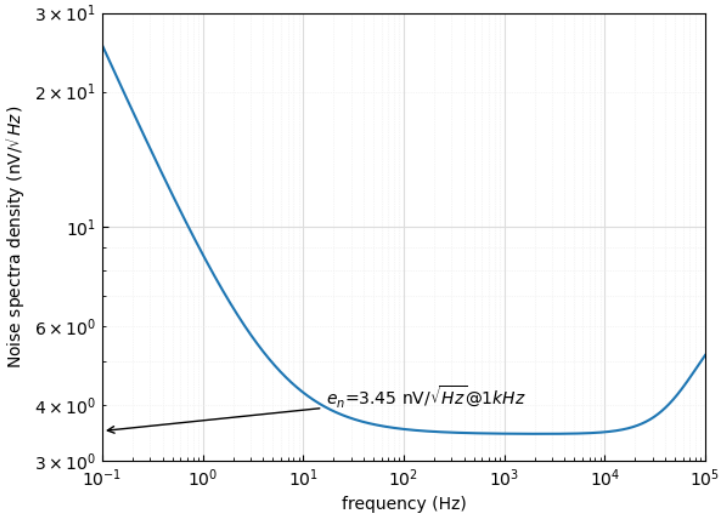


Figure 32 COPA V2 amplifier simulated Input referred voltage noise

3.5 Tests on Board #1A

The input impedance of Board #1A was measured at IPQ with the following results.

The input impedance was measured by two different methods.

In the first method, a voltage signal of 1 V generated by a calibrator Fluke 5730 was applied to a 100 MΩ resistor (Guildline, 9330) in series with the COPA's input signal (Figure 33). The drop voltage at the resistor was measured using a digital multimeter Fluke 8508A. The Input Impedance (Z_i) was calculated by the following expression:

$$Z_i w = R\left(\frac{U_{ref}}{(U_{ref} - U_{IN})} - 1\right)$$

where:

Applied voltage to the resistor: U_{ref}

Voltage at the COPA's input: U_{IN}

100 MΩ resistor in series with the COPA's input: R

In the second method, a voltage signal of 2 V generated by a calibrator Fluke 5730 was applied to a 100 MΩ resistor and the COPA's output voltage was measured using the digital multimeter Fluke 8508A. The Input Impedance Z_i was calculated by the following expressions:

$$Z = \frac{U_{IN} \times R}{U_{ref} - U_{IN}}$$

$$U_{IN} = \frac{U_{OUT}}{G}$$

here:

U_{ref} Applied voltage to the resistor

U_{IN} COPA's input voltage

U_{OUT} COPA's output voltage

G Gain previously measured

R 100 MΩ resistor in series with the COPA's input

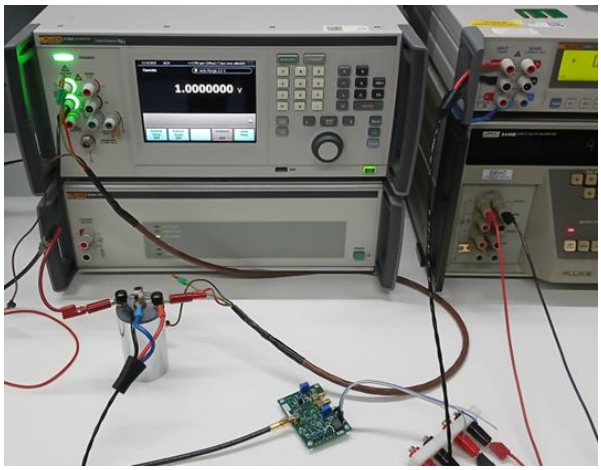


Figure 33 Setup to characterize the Input Impedance

The measurements and calculated input Impedance, Z_i, are presented in Tables 12 and 13 to the 1 V (first method) and 2 V (second method) applied signal, respectively.

Table 12 : Input Impedance results for 1 V input signal

U_{ref}	Freq	U_{ref} - U_{IN}	Standard Deviation	R	Z_i
V	Hz	V	µV/V	MΩ	GΩ
1	0	0,000622	43756	100,0132	161
		0,000161	46337		622
	20	0,196657	60		0,409
		0,195218	74		0,412
	100	0,659813	1430		0,052
		0,659642	1383		0,052
	1000	0,881438	124		0,013
		0,881423	123		0,013
	10000	0,88502	12		0,013
		0,88499	7		0,013
	20000	0,884928	8		0,013
	50000	0,884727	11		0,013
	100000	0,885378	14		0,013

Table 13 Input Impedance results for 2 V input signal

U_{ref}	Freq	U_{OUT}	Standard deviation	R	U_{IN}	Z
V	Hz	V	µV/V	MΩ	V	GΩ
2	0	2,000572	7	100,0132	1,999665	597
	20	1,303766	66		1,303832	0,187
	100	0,390713	1258		0,390732	0,024
	1000	0,217301	2388		0,217312	0,012
	10000	0,214956	2102		0,214935	0,012
	20000	0,215091	1808		0,21498	0,012
	50000	0,215183	2150		0,214583	0,012
	100000	0,215310	2187		0,213864	0,012

3.6 Gain and Phase Displacement Measurements on Board #1A

At IPQ the following method was use to characterize the gain. A voltage signal from a Calibrator Fluke 5730 was applied to the COPA's input and the COPA's output voltage (50 Ω impedance) was measured by a digital multimeter Fluke 8508A (Figure 34). The board was powered by a power supply with a stable voltage of + 15 V / -15 V.

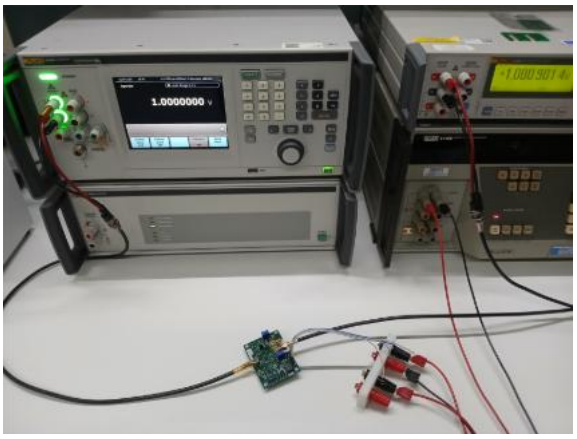


Figure 34 Set-up at IPQ for gain measurements of Board #1A

Figure 35 shows the value of the measured gain as a function of the signal frequency from 20 Hz to 100 kHz. For 20 Hz to 100 kHz, the Gain results show a good agreement between the 1V and 2 V signals. The maximum difference between the Gain at 2 V at 1 V was -11 µV/V at the 50 kHz.

For DC, a difference of -448 µV/V was found between the Gain for 1 V and 2 V input signal. This expected value has no explanation for now and further investigation was not possible to due to time limitations.

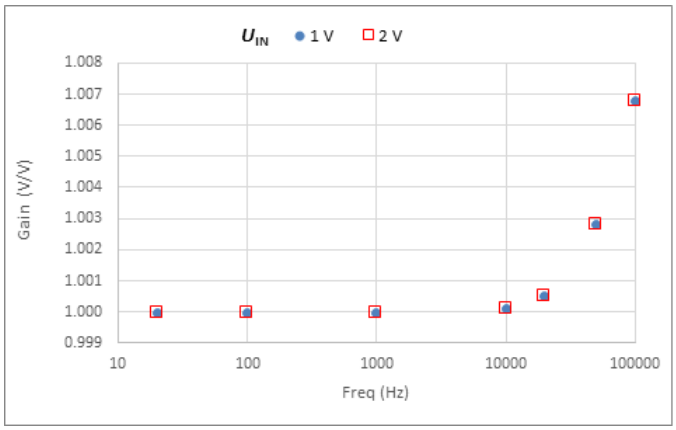


Figure 35 : Results to the Gain for input signal of 1 V and 2 V as function of frequency from 20 Hz to 100 kHz

Gain and phase displacement measurements of Board#1A were also carried out by INRIM with the following results:

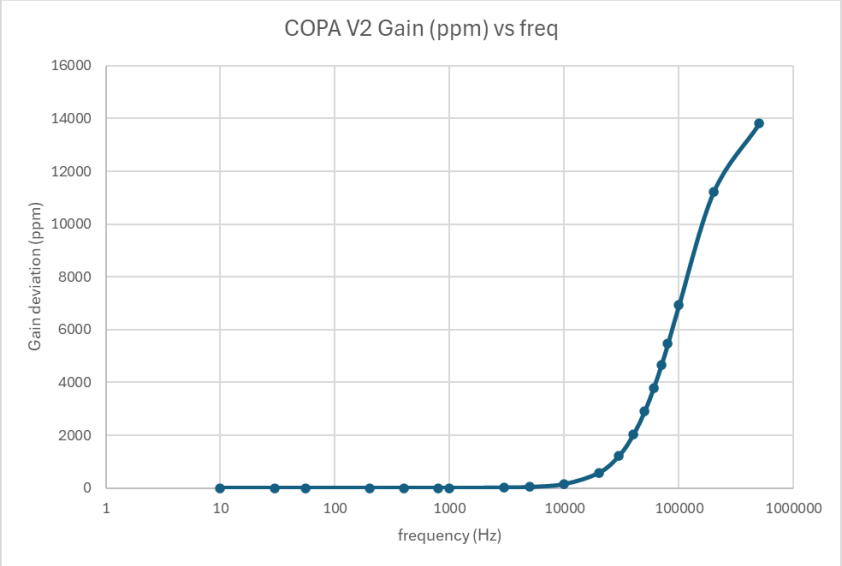


Figure 36 Gain deviation vs. input frequency for Board #1A

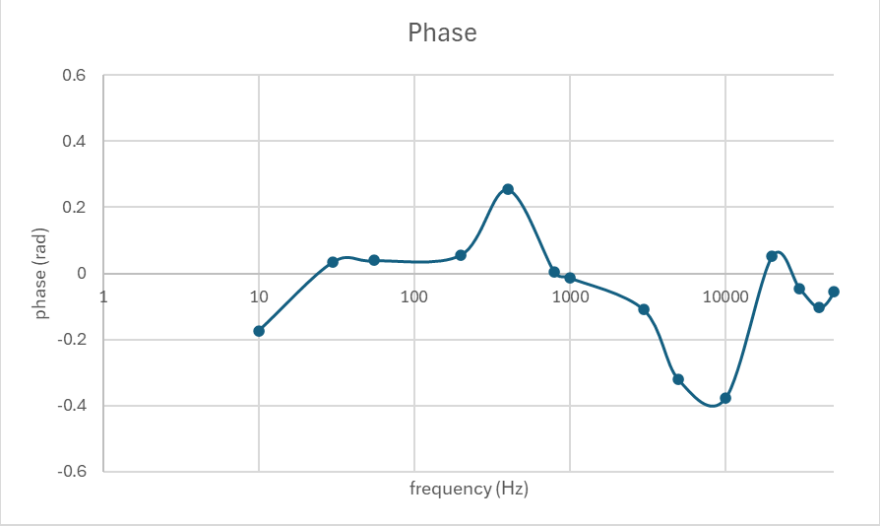


Figure 37 Phase displacement vs. Input frequency for Board #1A

3.7 Tests on Board #3A and #4A

Testing of Boards #3A and #4A was carried out by JV with the following results.

3.7.1 Gain measurements of COPA boards #3A and #4A

The gain of the COPAs was measured as AC-DC voltage difference using a set of thermal voltage converters (TVCs) and range resistors (RRs) in an AC-DC voltage bridge. This bridge measures the relative difference in AC-DC response between a reference(REF) (here a TVC or an RR in front of a TVC) side and a device-under-test (DUT) side (here a COPA board #3A, #4A or SMA(m)-to-SMA(m) union loaded by a TVC or a RR in front of a TVC). The measurements using the SMA(m)-to-SMA(m) union serve as the reference measurement for the system, which is subtracted from the measurements involving the COPA board #3A and #4A to get the response of the COPAs. A simplified schematic of the COPA in the AC-DC voltage difference bridge is shown in Figure 38.

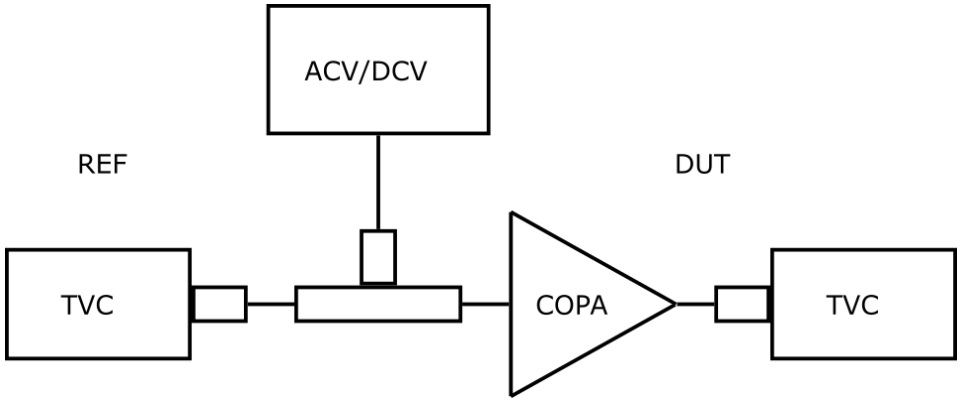


Figure 38 Setup of the gain measurement of the COPAs #3A and 4A

Signals with nominal voltages of 1 V, 5 V and 7 V in the frequency range of 10 Hz – 1 MHz were used. The TVC s used were as follows:

1 V : A pair of 600 Ω / 3 V TVCs from NIST

5 V: A pair of 1 kΩ / 5 V TVCs from NIST,

7 V: A pair of 800 Ω RRs from Ballantine, one in front of the before-mentioned 600 Ω / 3 V TVCsfrom NIST.

The measured relative gains of Boards #3A and #4A are shown in Figure 39.

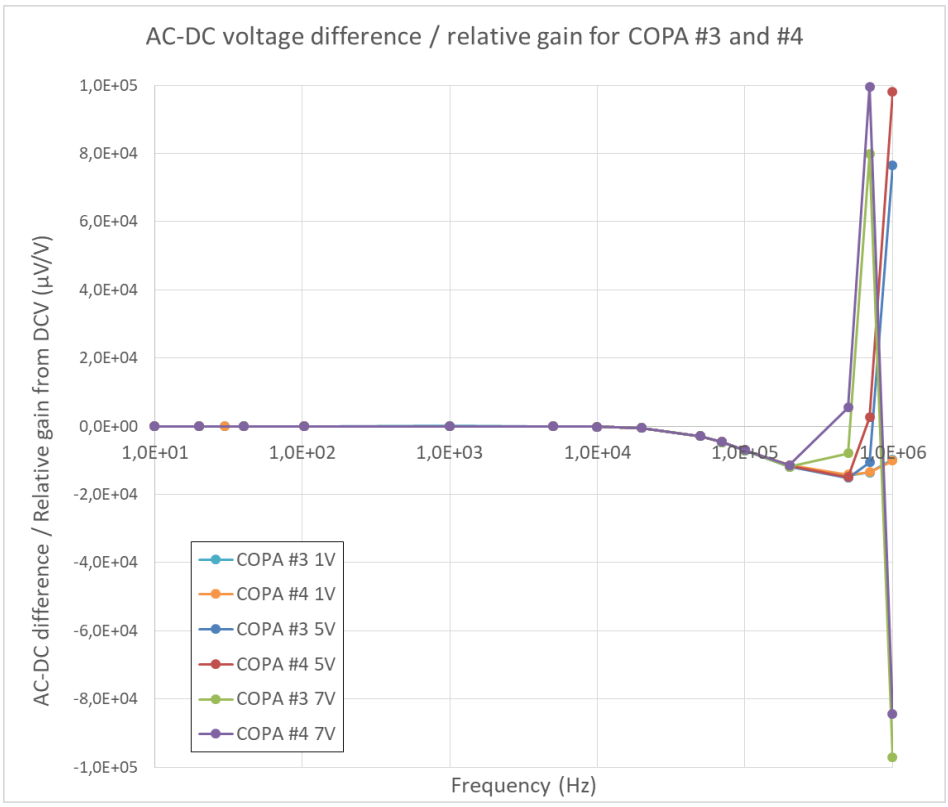


Figure 39 39 AC-DC voltage difference / relative gain from DCV for COPA #3 and #4 at 1 V, 5 V and 7 V.

3.7.2 THD measurements of COPA boards #3A and #4A

Four ultra-pure oscillators from JanasCard, generating frequencies of 103 Hz, 1 kHz, 10 kHz, and 20 kHz, were used for harmonic distortion measurements. The oscillator THD was calculated from measurements taken by connecting the oscillators directly to the QA403 audio analyser.

The setup for THD measurements of boards #3A and #4A is shown in Fig. 40. The input of the board was connected to the oscillator output, while the board output was connected to the internal notch filter of the oscillator. The output of the notch filter was then measured using the QA403 audio analyser.

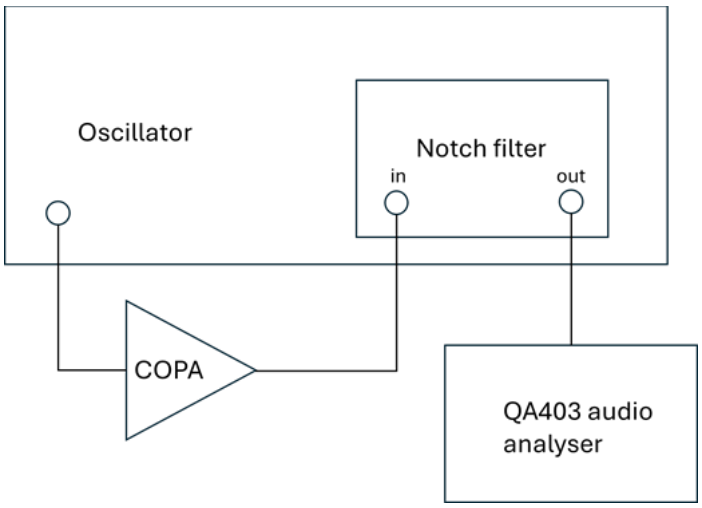


Figure 40 Setup of the THD measurements of the COPAs #3A and 4A

According to the oscillator user manual, the second and third harmonics are attenuated by 9 dB and 5 dB, respectively, when the internal notch filters are used. After the notch filter, the signal is amplified by a stage with a gain of 46 dB. Consequently, 37 dB must be subtracted from the measured second-harmonic level, 41 dB from the measured third-harmonic level, and 46 dB from the remaining harmonic levels. These corrections were used to calculate the THD for boards #3A and #4A.

For the THD calculation of the oscillator, its output is connected to the input of the notch filter. After applying the necessary correction, the filtered output is used to determine the oscillator's THD.

Due to the limitations of the QA403 audio analyser, only the first four harmonics were observed in the tests using oscillator 10 kHz and 20 kHz. Therefore, the THD calculation was based on harmonics up to the fourth order. The results are presented in Table 14 and Figure 41.

Table 14 Total harmonic distortion results for the oscillators at 1 V amplitude, Board 3A and Board 4A including the bandwidth resulting from the sampling rate used.

fundamental frequency (Hz)	Input THD (dB)	Output THD of COPA 3A (dB)	Output THD of COPA 4A (dB)	Bandwidth (kHz)
103	-144.12	-144.58	-143.91	24
1000	-142.71	-145.25	-141.92	
10000	-138.10	-131.75	-122.57	48
20000	-130.22	-119.67	-118.01	96

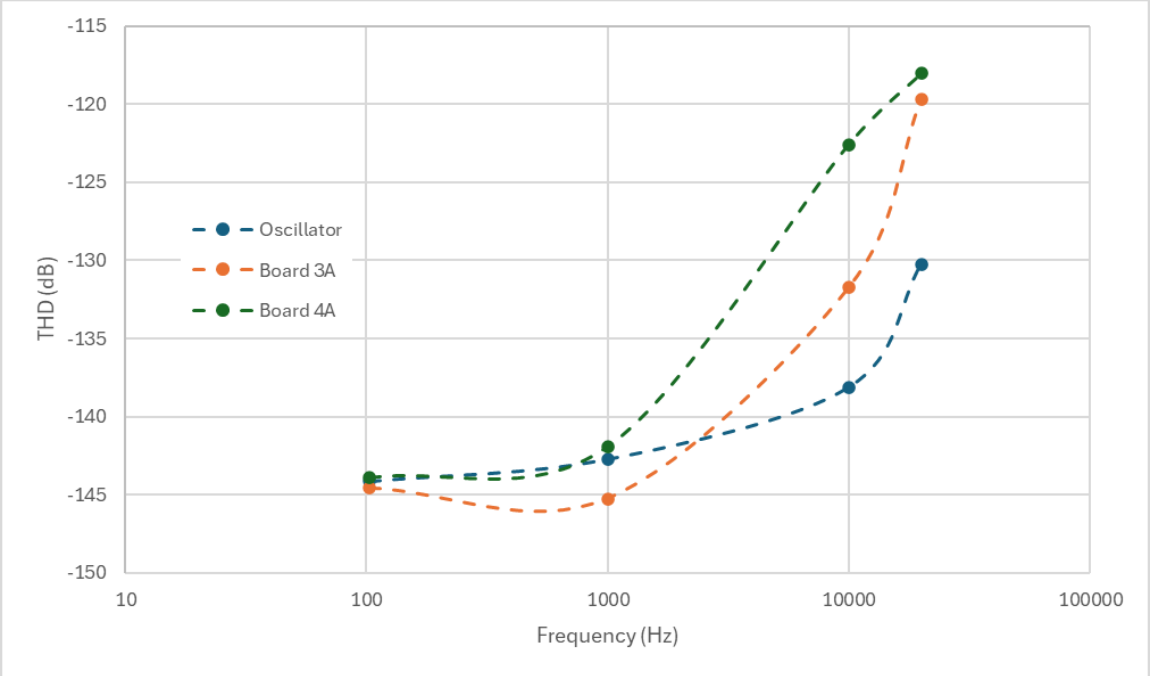


Figure 41 Total Harmonic Distortion of the oscillators, the Board 3A and Board 4A as a function of frequency

The Board THD results at 103 Hz and 1 kHz are not reliable, as their upper bound falls within the range of the oscillator's THD. In contrast, the results at 10 kHz and 20 kHz are more robust, since the oscillator's THD is noticeably lower than the Board THD at these frequencies.

3.7.3 Noise Measurement

Following the same procedure as in section **2.3.6**, the new COPA voltage and current noise was measured for board #2A at PTB. The results are shown in Figures 42 and 43. Figure 43 is the measured output of the COPA with a 100 MΩ resistor connected to its input and another unit of PTB's PA3 low noise amplifier as in section 2.4.6. The equivalent voltage noise voltage noise at 1 kHz was measured to be 3.5 nV/√Hz (red line on Figure 42). The current noise using the 100 MΩ resistance was measured to be 6.23 fA/√Hz

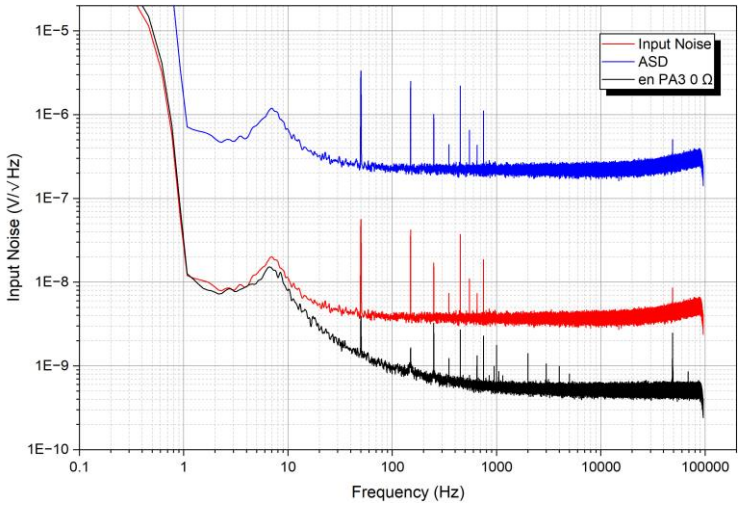


Figure 42 Measured equivalent voltage noise of Board #2A

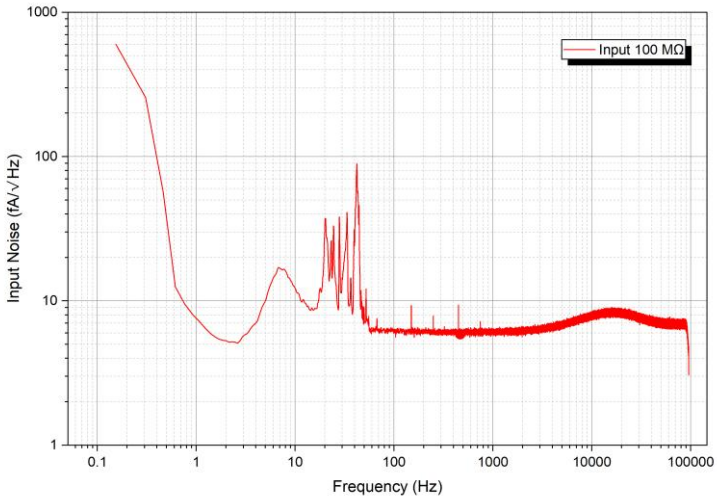


Figure 43 Measured COPA output voltage of Board #2A with 100 MΩ connected to the input

4. Design and performance verification of the composite amplifier integrator

4.1 Requirements for an integrator in a high-resolution AD converter

The basic integrator is shown in Figure 44.

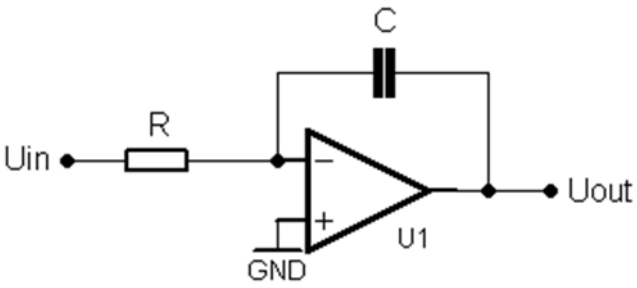


Figure 44 A basic integrator

Its transfer function is:

$$A_i = \frac{1}{2\pi f RC}$$

with an ideal operational amplifier with infinite gain and bandwidth. The natural frequency of the integrator is:

$$f_i = \frac{1}{2\pi RC}$$

A real amplifier has a limited open-loop gain (A_o) and a limited bandwidth (GBW), and its gain margin Gm at middle frequencies is:

$$G_m = \frac{GBW}{f_i}$$

and is frequency independent with the amplifier with standard 20 dB/decade roll-off. At lower frequencies, it is limited by the open-loop gain A_o; at higher frequencies, it is limited by the GBW. Precision integrators require a more complex circuit with two amplifiers as shown in Figure 45 because the gain margin of only one amplifier G_m is insufficient for higher accuracy applications.

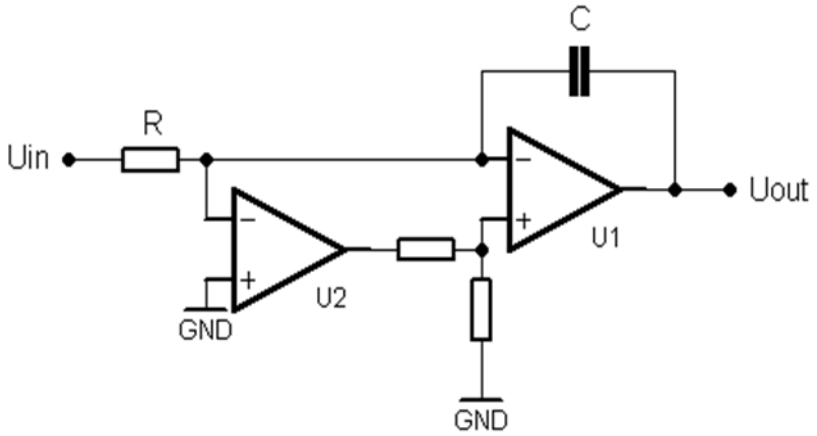


Figure 45 A precision integrator

A very important parameter is the response to an input step. The error voltage amplitude V_{err} on the virtual ground of the inverting amplifier's input is given by the following formula:

$$V_{err} = \frac{V_{in} \cdot Z_o}{R}$$

where V_{in} is the amplitude of the input step and Z_o is open loop impedance of the amplifier U_1. This error voltage settles to zero over a time constant of T_i:

$$T_i = \frac{1}{2\pi GBW}$$

Therefore, a fast amplifier with a high GBW and a low Z_o is necessary for fast settling. This settling time determines the shortest possible input pulse width, typically the shortest width of the reference pulse.

The noise of an integrator comes from two sources: the noise of the input resistor and the noise of the amplifier. The voltage noise density e_r of the resistor is:

$$e_r = \sqrt{4kTR},$$

where k is Boltzmann's constant, T is the absolute temperature in degrees kelvins and R is resistance. And total input referred noise e is:

$$e = \sqrt{e_r^2 + e_v^2 + R_{in}^2}$$

where e_v is input voltage noise density of the amplifier and R_{in} is input current noise density. With a typical resistor value in the range of 10 to 4 kΩ, the resistor noise is in the range of 12.6 to 28.3 nV/√Hz. This noise source usually dominates if a low-noise FET-based amplifier is used. For a complex amplifier composed of two or three amplifiers, an exact analytical description becomes rather complicated, so SPICE simulation is the best approach.

4.2. Analysis of the HP3458 integrator

A simplified schematic of the HP3458 integrator is shown here. A detailed schematic was taken from the HP3458 documentation and redrawn in LTSpice for detailed analysis.The entire circuit follows the basic connection shown in Figure 45 but with several modifications. Three amplifiers were used instead of two. Two fast amplifiers, U2 (AD848) and U3 (LM6361), were connected. These amplifiers are bipolar with a high input current and high input current noise. Therefore, their negative inputs are isolated from the common summing node with the JFET J1 (U308). These amplifiers form the fast part of the integrator and are DC stabilised by precision amplifier U1 (LT1001). There is a problem with using the AD848: this amplifier is stable with a closed-loop gain of over 5, but the integrator requires stability with a gain of 1. Additional components (C3, C4, R5, C12 and R17) were therefore added to ensure stability. Figure 46 shows the schematic and open-loop amplitude and phase characteristics. GBW of the whole circuit is about 35 MHz.

The noise performance of the whole circuit isn't very good: the AD848 has an e_n of 5 nV/√Hz, the LM6361 is significantly worse at 15 nV/√Hz, the compensation capacitors increase the noise gain, and Q110 has an attenuation of 2 dB. The resulting input referred noise plot is shown in Figure 47. At frequencies of up to 100 Hz, noise is dominated by the LT1001, achieving a minimum value of around 32 nV/√Hz. However, it increases rapidly at higher frequencies, reaching 2 µV/√Hz, as well as at very low frequencies, due to the 1/f voltage and current noise of the LT1001.

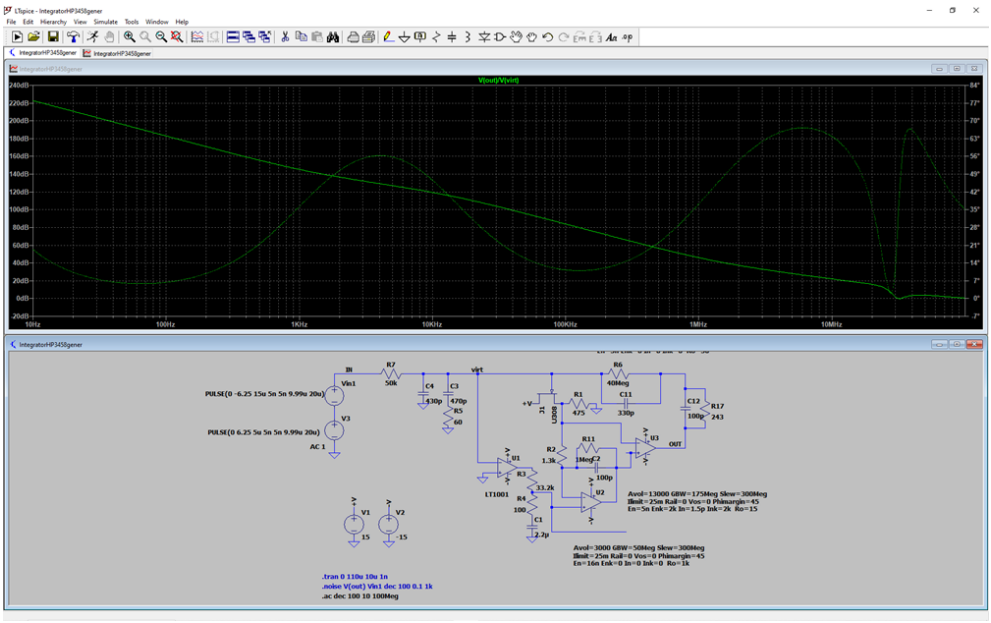


Figure 46 Open loop gain of the HP3458 integrator

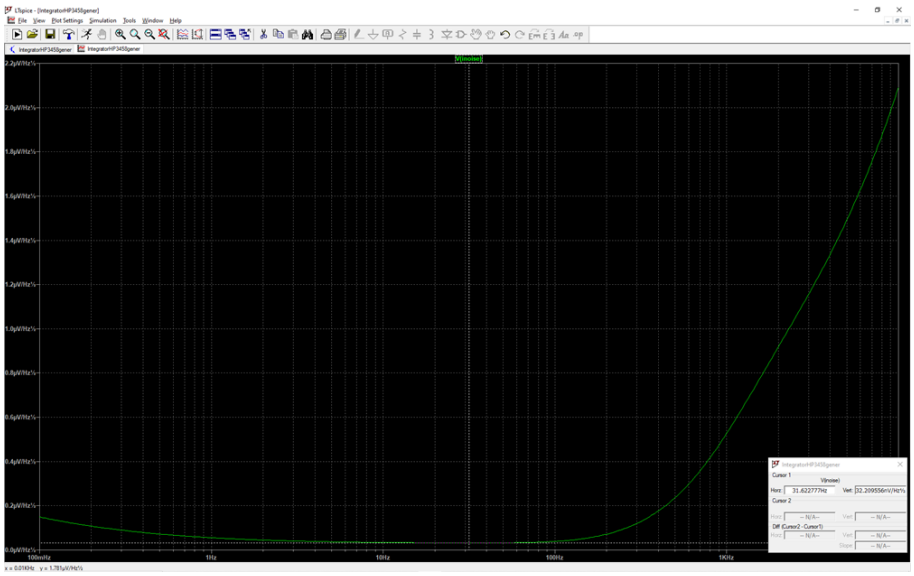


Figure 47 . Noise performance of the HP3458 integrator

Figure 48 shows the voltage spike at the summing node during a 12.5 V step in the input voltage. This is equivalent to switching a 250 µA reference current. The voltage settles within about 250 ns.

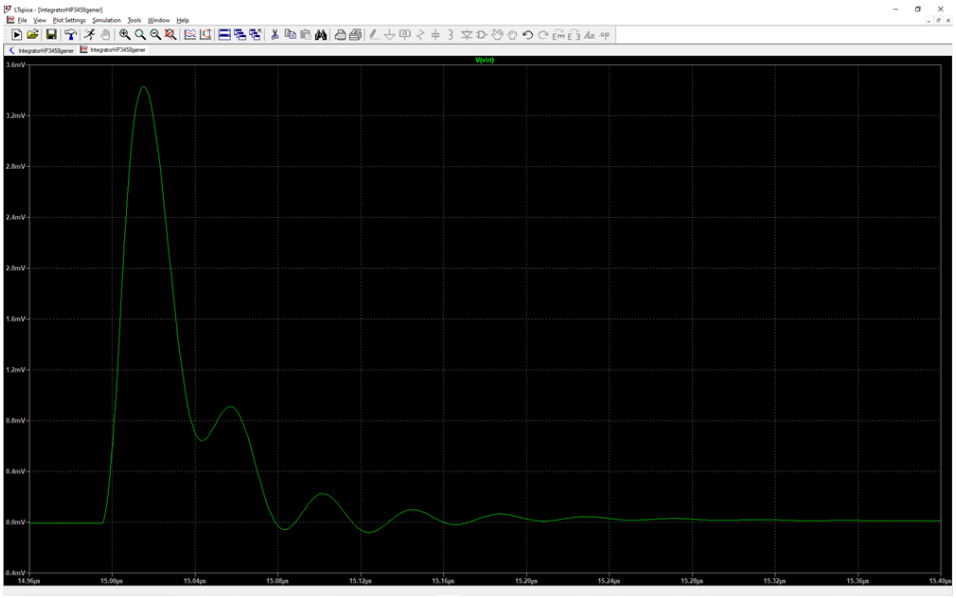


Figure 48 Transient analysis of the HP3458 integrator

4.3. Design of a new integrator

The project collaborator, John Pickering of Metron Designs Ltd., designed a very fast integrator with a power supply of ±12 V. The response to an input current step is shown in Figure 49. This figure

shows an excellent step response, with a settling time below 50 ns. The main drawback of this circuit is that it uses an AD8065 with a maximum power supply of ±12 V, resulting in a maximum output swing of ±10 V for the integrator.

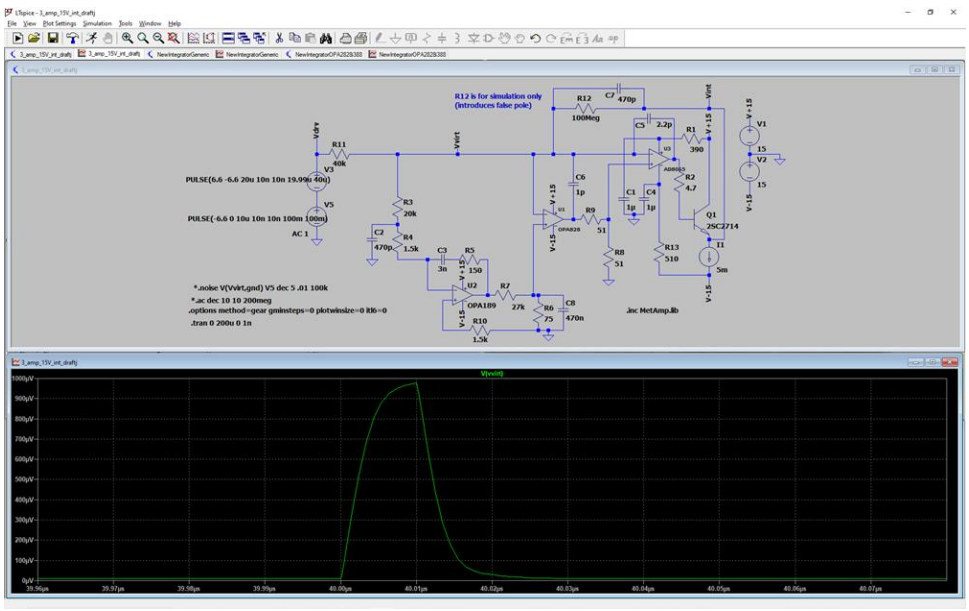


Figure 49 . Step response of integrator designed by John PIckering

A new version of the integrator based on John Pickering's design has been developed. The main change was the redesign for use with a ±15V power supply, which required different amplifiers. The circuit comprises three op amps: two fast OPA1656s, which are DC stabilised by a chopper OPA388. The output emitter follower Q1 reduces the open-loop output impedance, thereby reducing the amplitude of the spike during current switching.

Figure 50 shows the AOL versus frequency characteristic. The GBW is approximately 50 MHz, which is the same as the OPA1656's own GBW. The gain at 10 Hz is an incredible 300 dB.

Figure. 51 shows noise performance of the new integrator. The minimum noise level is 33 nV/√Hz, which is comparable to that of the HP3458. However, noise at lower frequencies is better due to the use of a chopper amplifier with no 1/f noise. The noise at higher frequencies (52 nV/√Hz at 10 kHz) is approximately 40 times lower than that of the HP3458 integrator (2 µV/√Hz at 10 kHz).

Fig. 52 shows detail of the step response of the new integrator. The settling time of the new circuit is about 250 ns. This is worse than John Pickering's circuit, but still faster than the original HP circuit.

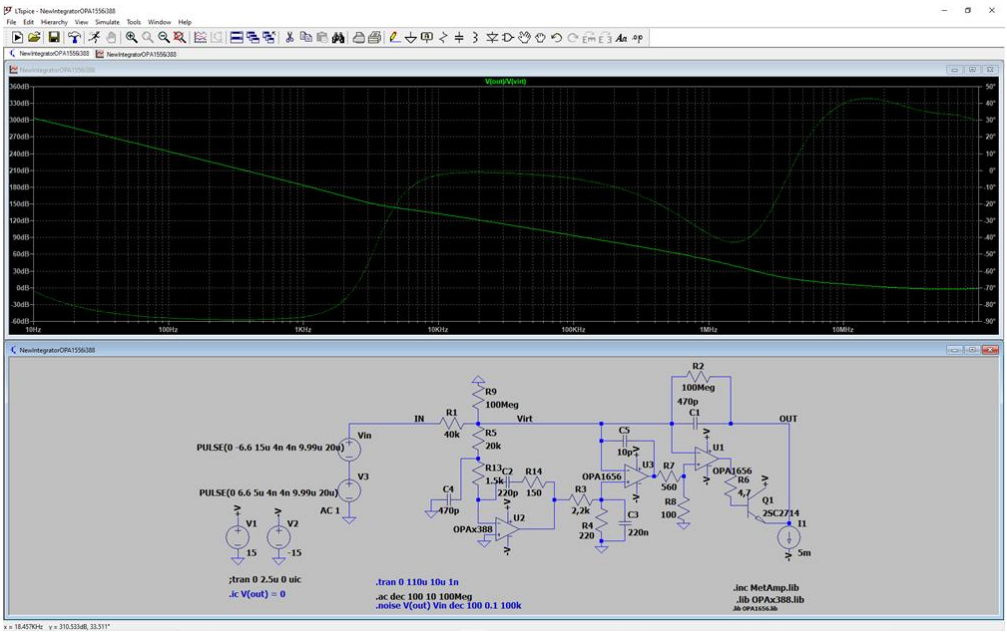


Figure 50 Open loop gain of the new integrator

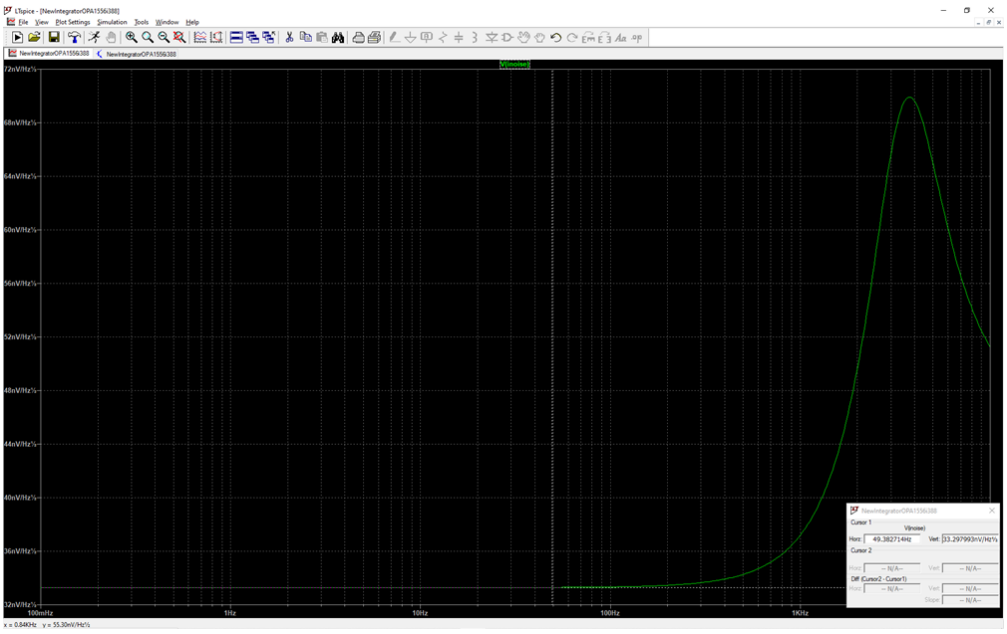


Figure 51 Noise of the new integrator

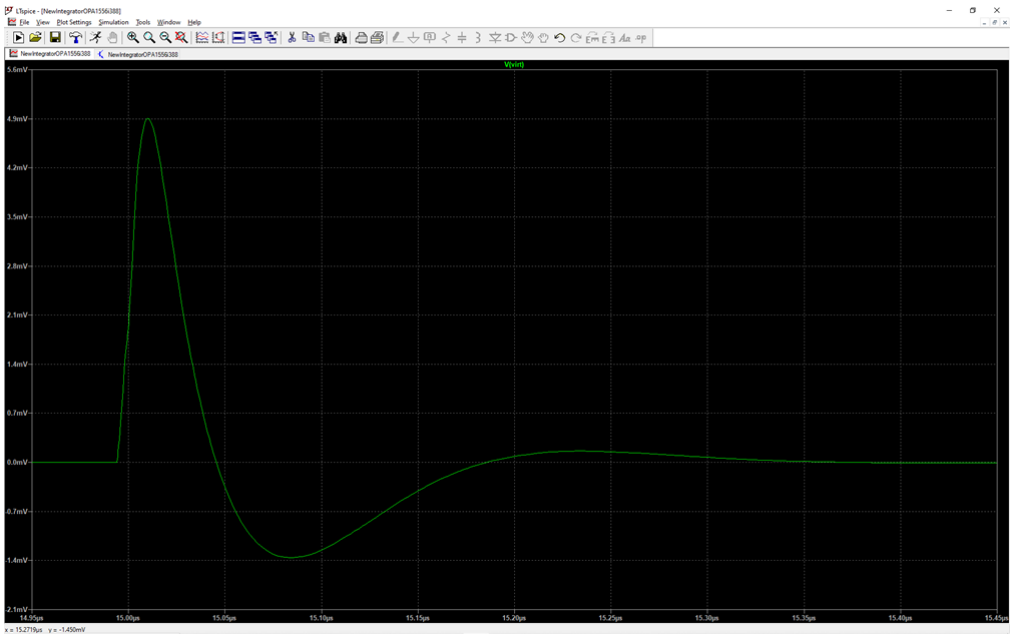


Figure 52 Detail of the transient analysis of the new integrator

4.4. Realisation of the new integrator

The new integrator described in the previous chapter has been implemented. A full schematic can be found in Figure 53 and the PCB layout in Figure 54. The main change is the addition of switches for charge injection testing.

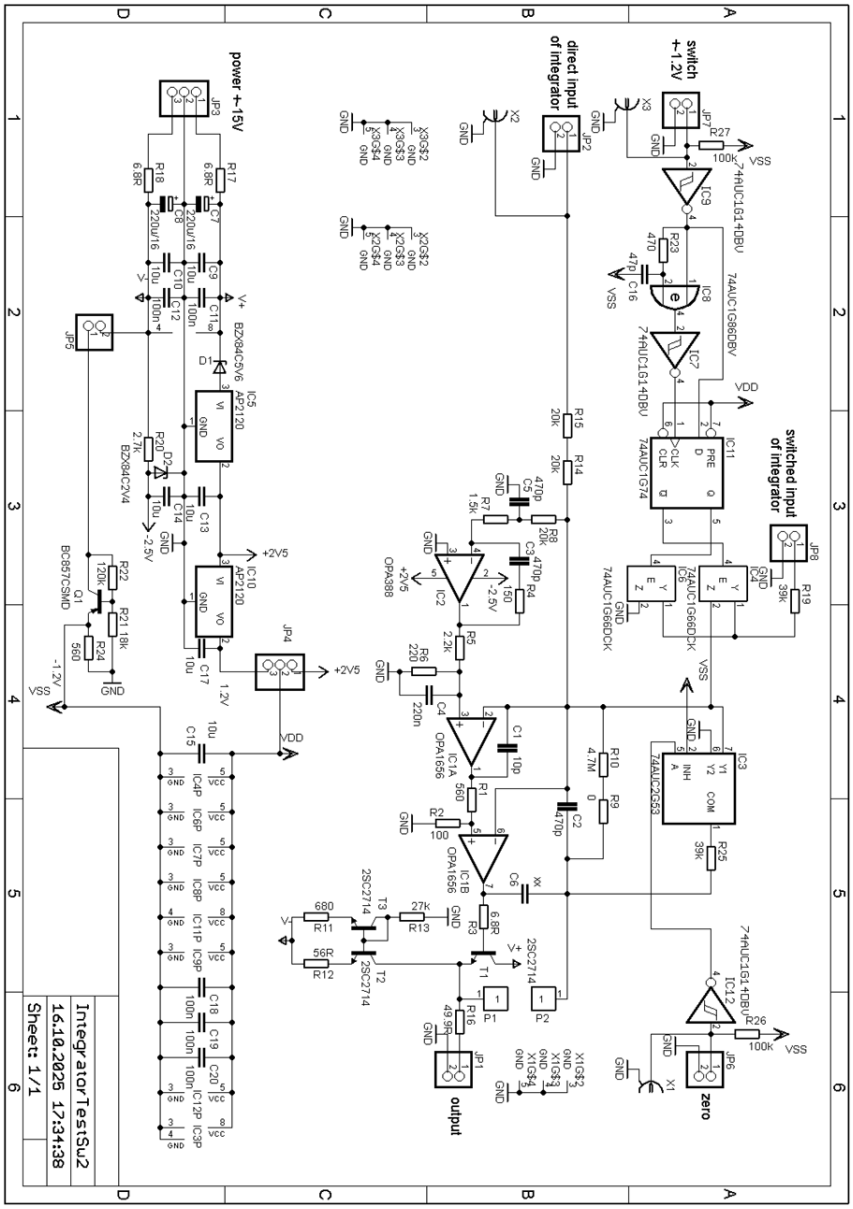


Figure 53 Circuit diagram of the new integrator

As was discovered in earlier experiments, charge injection from switches connected as a current steering switch on the input differs significantly from the standard charge injection test described in the switches' data sheets. The second reason is that the switches used (74AUC1G66 and 74AUC2G53) have no specified charge injection.

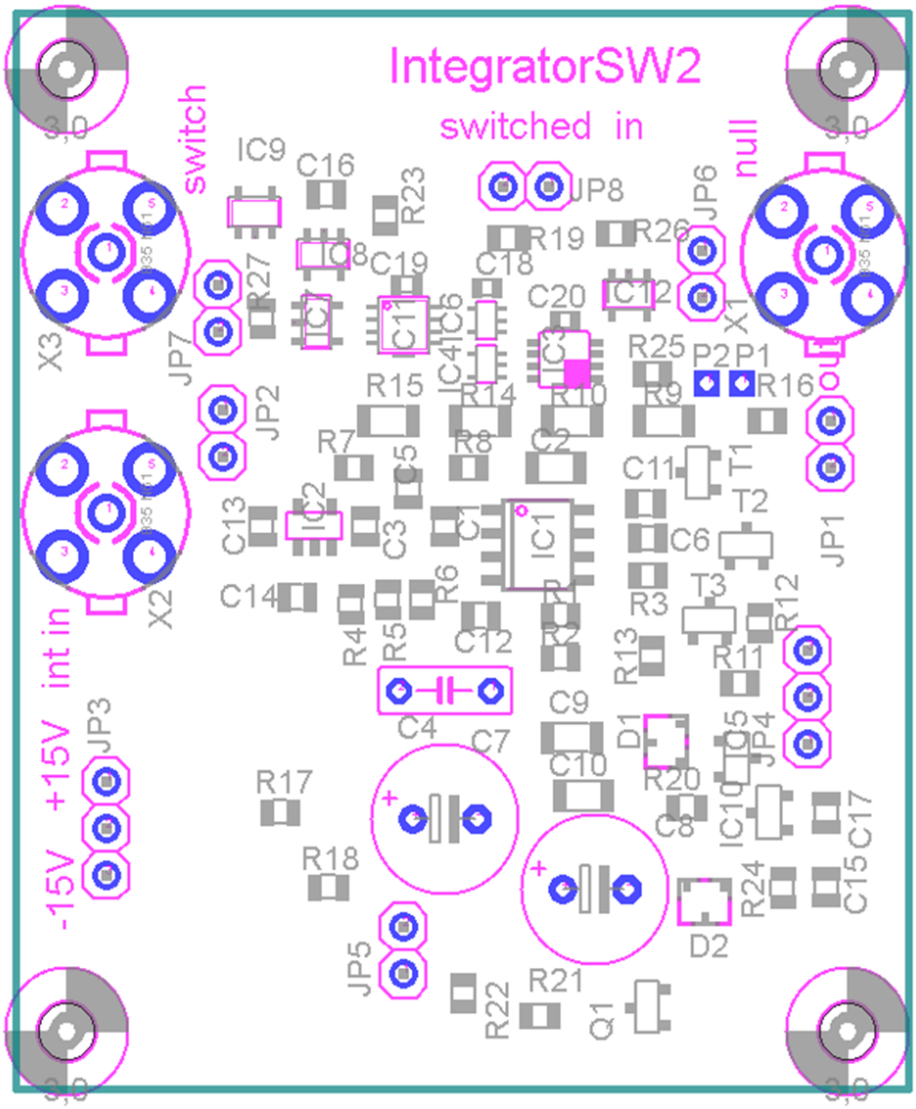


Figure 54 PCB layout of the integrator

4.5. Testing of the new integrator

The integrator is a key component in the planned AD converter integration. Testing it as a standalone component is difficult due to its unstable nature, so a resistor with a value of 4.7 MΩ (R10) was added to stabilise it. Three tests were conducted with a prototype of the integrator: 1. Stability of the entire integrator. 2. Response to a square wave signal. 3. Charge injection of both types of switches.

4.5.1. Stability test

The proposed integrator is a complex structure. It consists of three op-amps and an emitter follower. These are connected in series and closed with a single feedback loop. Although the LTSpice simulation shows that the entire circuit is stable, it is necessary to verify this on a prototype. Checking with a 350 MHz RTB2004 oscilloscope shows no parasitic oscillations on the output or the internal nodes of the integrator (i.e. the outputs of the operational amplifiers).

4.5.2. Response to a square wave signal

A square wave signal input to the tested integrator produces a triangular output signal. Deviation from the perfect response is very low and cannot be observed on the output by an oscilloscope. Therefore, an error voltage on the virtual ground was checked instead, as in the LTSpice simulation. A Rigol DG992 arbitrary generator operating at 100 MHz was used to generate the square wave signal. The parameters of the square wave were: The amplitude was 13.2 V_{pp}, which corresponds to the assumed step of the reference current of 0.33 µA. The frequency was set to 50 kHz to prevent the integrator from saturating. The rise time was 40 ns, which is a bit slow. A LTSpice simulation was also performed with this slower risetime, and it shows that the results are still valid; only the amplitude of the error voltage is slightly reduced. Figure 55 shows the measured voltage.

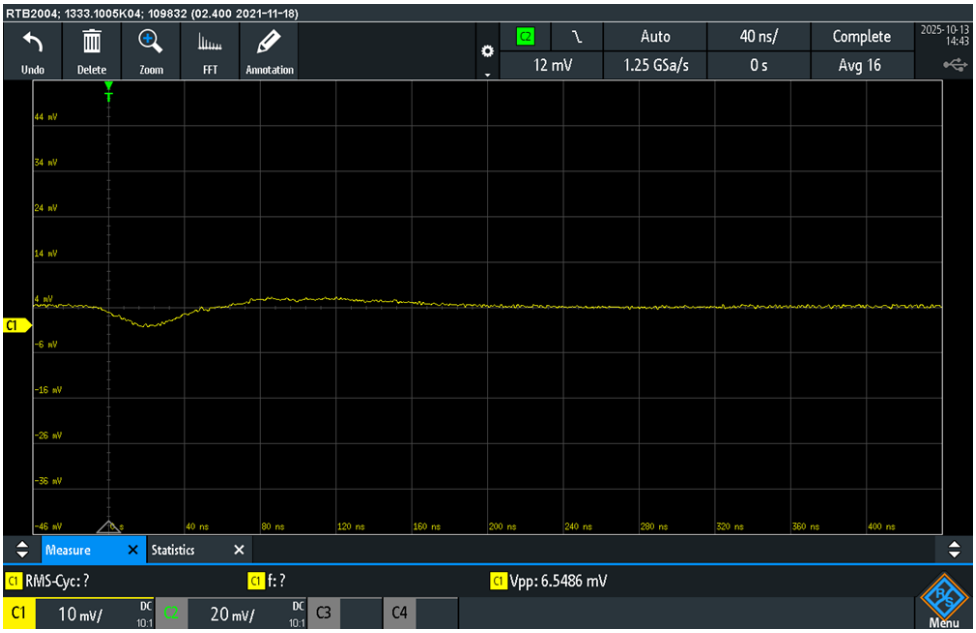


Figure 55 Error voltage at the Virt node

It shows that the voltage settles to zero in approximately 250 ns. Therefore, the minimum pulse width of the reference current is 250 ns, but 300 ns is preferable to allow for some margin.

4.5.3. Charge injection test

Current steering switches are a very important part of the integrator. They should be fast and have low R_{on} and charge injection. The speed and R_{on} are specified in the datasheet, but the charge

injection is often not specified. Even when specified, the commonly used test method differs significantly from the use of the switch for current steering and produces overly optimistic results, so testing them in a real integrator is necessary. There are two current steering switches: - IC4 and IC6 (74AUC1G66), which switch the input current from R19 between the integrator input and ground and IC3 (74AUC2G53), which resets the integrator via R25. Both switches require a positive signal to switch the current to the integrator input. They require a bipolar signal of +1.2 V and -1.2 V on the inputs X3 (JP7) and X1 (JP6), respectively. A dual-channel generator DG992 with a rectangular signal, with a period of 500 µs, a width of 100 µs, and a phase shift of 180° between the outputs was used. The results are shown in Figure 56. trace C1 - integrator output, trace C2 control switch 1G66.

time 0 us - external current on (auc1g66) step 1 mV = 0.5 pC
time 100 us - external current off (auc1g66) step -0.2 mV = -0.1 pC
time 250 us - zero on (auc2g53) step 1.8 mV = 0.85 pC
time 350 us - zero off (auc2g53) step -0.7 mV = -0.33 pC
Total charge is 0.4 pC for AUC1G66 and 0.5 pC for AUC2G53.

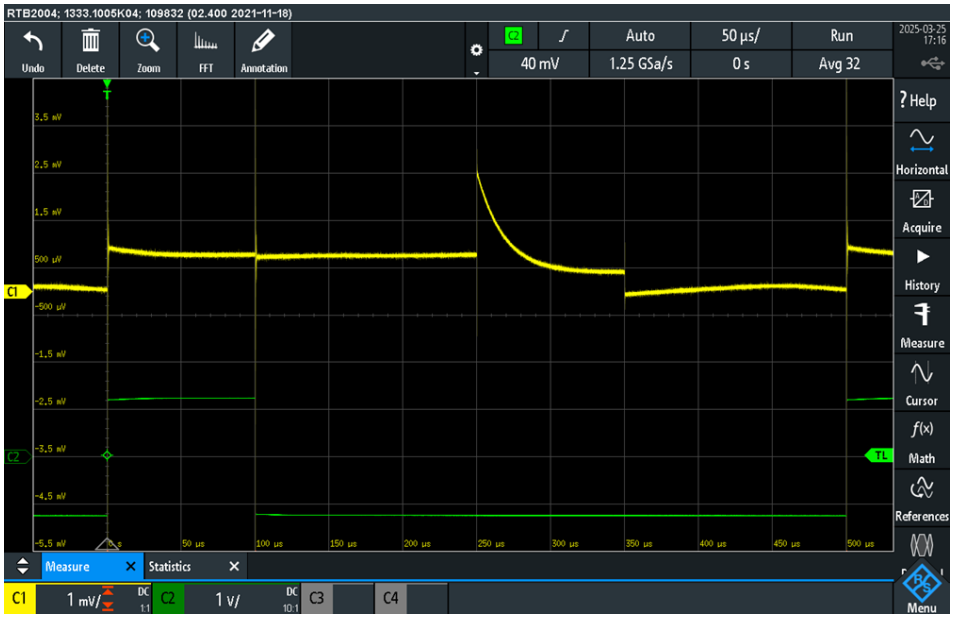


Figure 56 Charge injection test

5. Conclusion

In this report in the development and testing of COPAs to be used for integrator and front-end circuitry of a high-precision digital voltmeter has been described. The input COPA of the HP 3458A and the integrator designed by John Pickering have been used as stepping-stones to develop new and improved COPA designs.

As a first step two boards whose design was based on that used in the front-end circuitry of the HP 3458A were produced. Characterisation methods were developed to characterise the COPAs' gain, phase, total harmonic distortion (THD) and input current and voltage noise. The preferred method was to use the Audio Precision APx555B to apply 7.071 V RMS signals to the COPAs and measure the responses. For gain and phase, the frequency was swept from 20 Hz to 20 kHz. The gain was measured to be 0.999750 V/V gain at DC-1 kHz and 1.001500 V/V at 20 kHz, and the phase was measured to 0° to –0.6° in this sweep. THD was measured to -134.14 dBc at 1 kHz input signal. The input voltage noise (shorted input on COPA) and current noise (100 MΩ on COPA input) were measured at 1 kHz to 3.9 nV/√ Hz and 6.6 fA/√ Hz, respectively. The equivalent circuit input impedance was also measured to 1.364 GΩ || 6.38 pF.

Based on the test results of the initial design a new COPA design was made, using an operational amplifier as a voltage follower to make a bootstrap guard for the signal path. The source and drain resistors for the input stage of the COPA were considered critical components for maintaining gain linearity and low drift. It was therefore decided to use Vishay metal foil resistor networks that had previously been characterised in Deliverable D3 in this project.

Four prototype boards were produced of the new COPA design. The boards were produced and circulated among the partners for testing. IPQ measured the input impedance of board #1A to be >100 GΩ for DC and >12 MΩ for frequencies up to 100 kHz and the gain from DC to 100 kHz, finding it to be flat from 20 Hz to 1 kHz and lower than 7000 µV/V at 100 kHz. INRIM measured the gain deviation of board #1A to be flat up to 10 kHz and at about 7000 µV/V at 100 kHz and measured the phase displacement to be within 0.4 rad at 10 Hz – 20 kHz. JV used an AC-DC voltage bridge to measure the relative gain deviation from DCV of boards #3A and #4A to be within 150 µV/V for applied voltages of 1 V RMS, 5 V RMS and 7 V RMS for frequencies up to 10 kHz and about 7000 µV/V for all applied voltages at 100 kHz, just like the results from INRIM's measurements for board #2A. JV measured the THD of boards #3A and #4A to be mostly well below –145 dB and –120 dB for input signals at 103 Hz – 1 kHz and 10 kHz – 20 kHz, respectively.

A new integrator has been developed, simulated, and tested. This new version is faster and produces less noise, especially at higher frequencies than the original HP integrator. Several types of switches were tested for use as current steering switches, and the types with the lowest charge injection were selected. Together with the switches, the proposed integrator is a key element of the planned integrating AD converter