22RPT02 True8DIGIT

Deliverable D3:

Report on metrological methods for characterisation of resistors and capacitors for their stability, tracking and non-linear behaviour down to and below -120 dB THD and of electronic switches for their injection currents and transients' stability, as well as results obtained on a selected set of high-grade resistors and capacitors

Organisation name of the lead participant for the deliverable:

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Deliverable Cover Sheet

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1. INTRODUCTION

This document describes investigations relating to the evaluation of some key components used in a high precision digitisers. The most critical parameters, namely precision, linearity and temperature/humidity dependence were measured and evaluated.

The report content flow is as follows:

In Chapter 2, the evaluation of the non-linear behaviour of resistors and capacitors is described. The evaluation used both direct measurements and simulations. The modified quadrature bridge setup, designed and developed within the project, that was used to measure these distortions with enhanced accuracy is described in detail.

In Chapter 3, the focus is on the characterization of resistor elements, specifically the stability and tracking of the resistance value (or ratio of two resistor elements) with temperature and humidity. Four different types of resistors (by technology and package), but of the same nominal values, were investigated.

Chapter 4 deals with the evaluation of capacitors. Measurements of the temperature coefficient of capacitance are presented, as well as measurements of other critical characteristics (temperature coefficient of loss component, sensitivity of capacitance to changes in relative humidity and sensitivity of loss component to changes in relative humidity). The set-up which was developed to measure dielectric absorption is described and some results, including the modelling of the capacitor, are presented

In Chapter 5, the results of the evaluation of electronic switches are presented. The focus was on Toshiba MC74HC4051A Analog Multiplexer / Demultiplexer as a typical representative of this type of device. Measurements were focused on critical parameters for this application such as on-resistance, input/output capacitance, delay time, rise time and charge injection.

Finally, in Chapter 6 and Chapter 7, the focus is on charge injection of digital switches. This parameter, which is an important parameter that can limit the performance of a digitizer, was measured and evaluated for two electronic switches.

2. MEASUREMENT OF RESISTOR AND CAPACITOR DISTORTIONS USING A MODIFIED QUADRATURE BRIDGE

2.1 Introduction

The measurement of non-linear distortions in resistors is essential for applications requiring high-precision components, such as a precision low-frequency digitizer. While most capacitors and resistors are designed to be linear, certain applications reveal minor non-linearities that can affect overall circuit performance. This report explores a modified quadrature bridge setup designed to measure these distortions with enhanced accuracy.

2.2 Modified quadrature bridge

Digitally assisted and fully digital impedance ratio quadrature bridges [1] are used in metrology for accurate impedance measurements [2]. Such bridges are energised by a two-channel phase-locked pure sine wave generator [3], where the upper and lower bridge arms are supplied with equal but opposite-phase

sine wave signals. However, these bridges have not yet been employed to measure capacitor non-linearity. Nevertheless, in its simpler form, a double source powered bridge has already demonstrated its ability to measure capacitor nonlinearity [4], where two sources have equal amplitude and are in quadrature phase lock, e.g. one source is lagging the other by 90°. When in balance at the given excitation signal frequency, this bridge provides nominally zero differential and common-mode output. With the given components used to construct the bridge, it can only be balanced at one frequency. Even then, harmonic components generated by the two sources still appear as a common-mode signal at the bridge output.

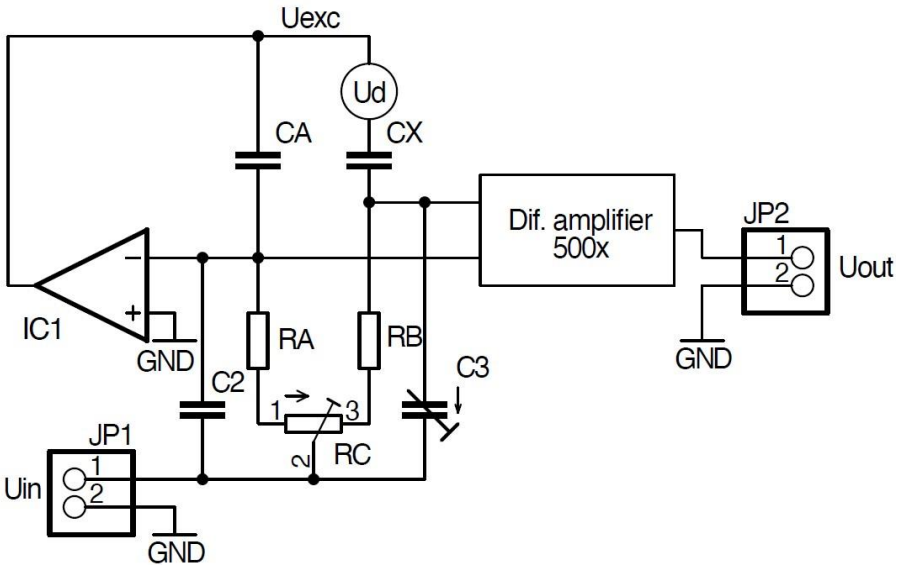


Figure 2-1: Block diagram of the proposed quadrature bridge for measuring capacitor nonlinearity

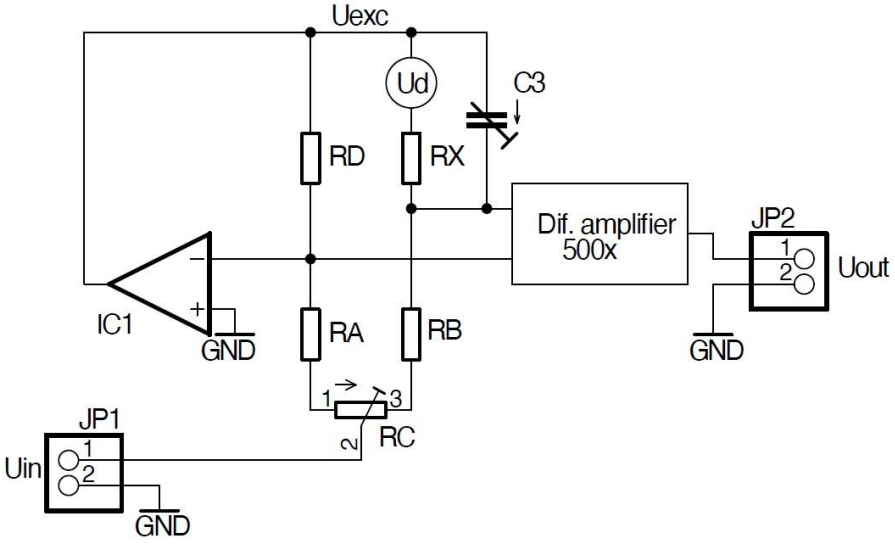


Figure 2-2: Block diagram of the proposed bridge for measuring resistor nonlinearity

Based on this concept, a simplified bridge is proposed. The basic measurement setup is shown in Figure 2-2 for the resistance bridge and in Figure 2-1 for the capacitance bridge. The following discussion applies to the capacitance bridge. The bridge consists of capacitors C_A and C_X in the upper arms and resistors R_A and R_B in the lower arms. U_d represents a residual voltage source due the non-linearity of C_X. R_C is used to balance the real part of the bridge, while C_2 and C_3 are used to balance its imaginary part. A sine wave signal from an external source is connected to the lower arm of the bridge. A fast low-distortion amplifier IC_1 operates as an integrator and generates an excitation signal U_{exc} for the upper arm of the bridge:

Eq. 2-1: $$U_{exc} = -\frac{1}{C_A(R_A+R_C/2)} \int U_{in} \sin(2\pi f t) dt,$$

which gives

Eq. 2-2: $$U_{exc} = \frac{U_{in}}{2\pi f C_A(R_A+R_C/2)} \cos(2\pi f t) + const,$$

U_{exc} is therefore generally not of the same amplitude as U_{in}. Using the capacitive bridge elements described above, U_{exc} lags U_{in} by 90°. The main advantage of the proposed bridge setup is the removal of the requirement to use two signals of equal amplitude operating in quadrature, as the second signal U_{exc} is generated by IC_1, following the signal U_{in}. This fact significantly simplifies the excitation of the bridge and enables the use of a single signal source. Furthermore, U_{exc} keeps the required phase lag and amplitude, which is no longer required to be equal to U_{in}, through the IC_1 feedback loop that keeps the left arms of the bridge in balance not only at the U_{in} fundamental frequency but also at all harmonics. Having the bridge nulled to have the left and right sides in balance at one signal frequency and amplitude, the Uin signal parameters can be changed, and the proposed bridge still remains in balance. As this mechanism is simultaneously true for the Uin harmonic components, these components no longer appear as a common mode at the output of the bridge. Consequently, the effect of the finite common-mode rejection ratio (CMRR) of the differential amplifier sensing the output of the bridge is greatly reduced. The effectiveness of this common-mode suppression technique has been demonstrated for different types of bridge circuits [5]. For perfectly linear components C_A, R_A and R_B, U_{out} contains only the amplified signal generated by the C_X non-linearity that can be digitized and analysed for its spectral content.

An additional benefit of the proposed simplified bridge is the ability to generate any phase lag in the upper arms, as dictated by the upper arm impedance seen by the IC_1 feedback loop. Therefore, the same bridge can be used to measure resistor non-linearity, when C_A is replaced with a reference resistor and C_X is replaced with the tested resistor.

2.2.1 Modified bridge design implementation

Detailed implementation of both bridges is shown in Figure 2-3 for the capacitance bridge and in Figure 2-4 for the resistance bridge.

Practical realisations of capacitance bridge are shown in Figure 2-5 for fundamental frequencies from 200 Hz to 20 kHz. Resistance bridge, shown on Figure 2-6 for high frequency (from 200 Hz to 20 kHz fundamental frequency) and on Figure 2-7 for low frequency (from 5 Hz to 1 kHz fundamental frequency) follows the same approach.

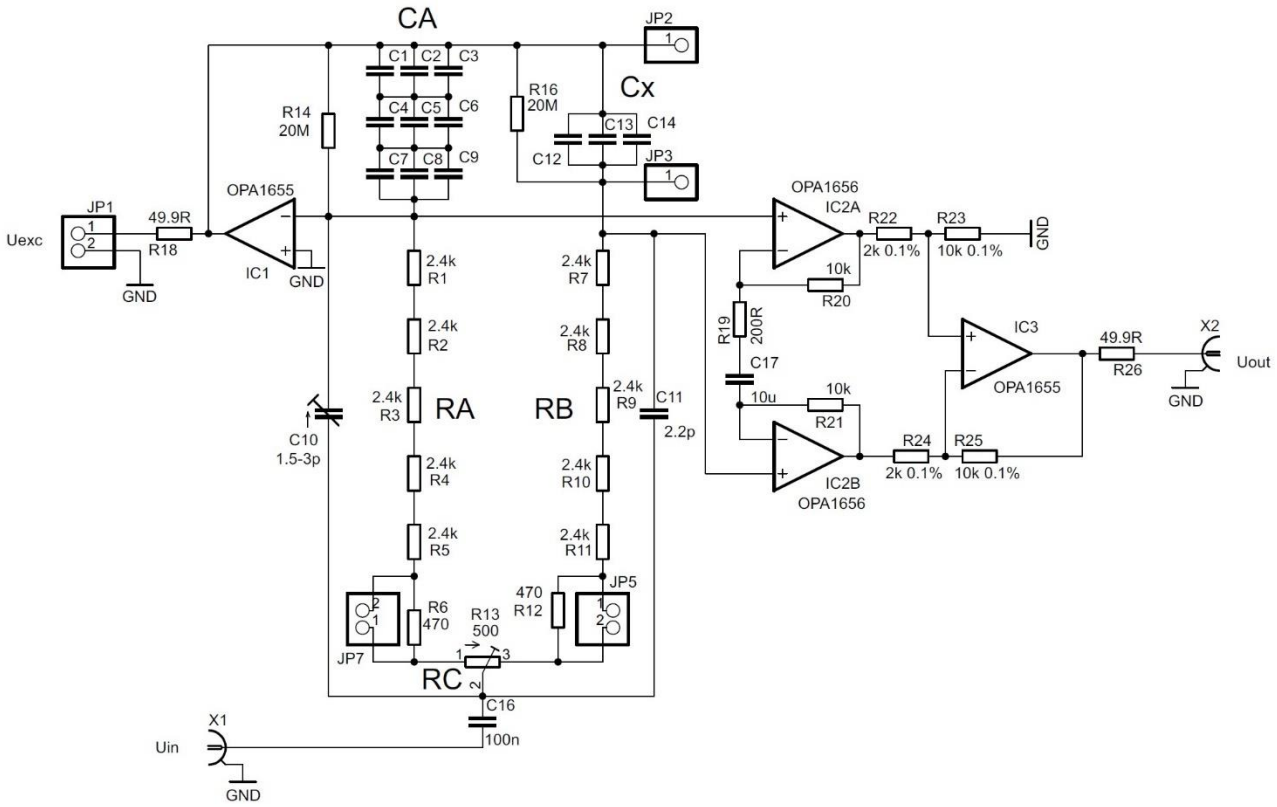


Figure 2-3: Detailed circuit diagram of the proposed capacitor quadrature bridge. C_X is shown as a parallel combination of three capacitors C_{12}, C_{13} and C_{14}, which serve to accommodate different capacitor sizes used as a C_X. Only one capacitor is attached for each measurement.

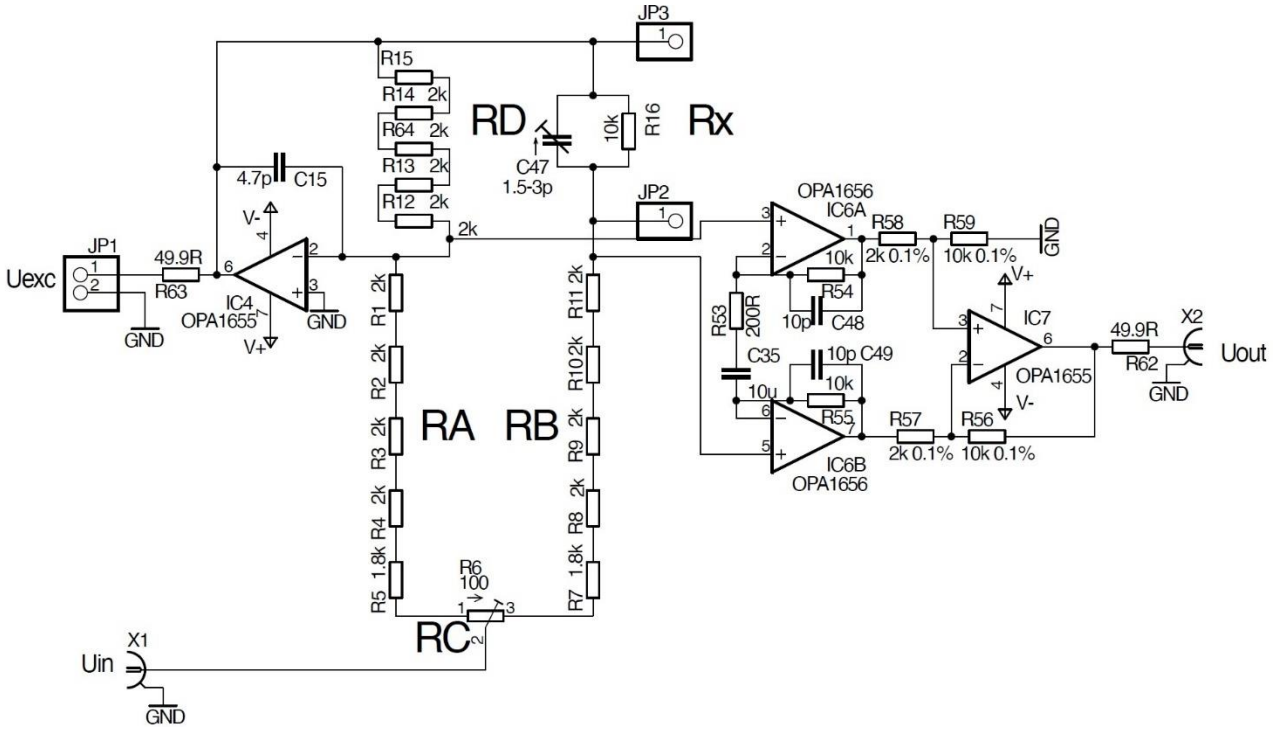


Figure 2-4: Detailed circuit diagram of the proposed resistor bridge. Instead of C_A (Figure 2-3), R_D is used, realised as a series of five equal resistors.

2.2.2 Basic properties and interpretation of measurement results

2.2.2.1 Capacitance bridge

If C_X distortion is modelled as an additional voltage source U_d (see Figure 2-1), before it is amplified by the differential amplifier, it is high-pass filtered by the R_C filter consisting of C_X and R_B, with a transfer function given by

Eq. 2-3: $$k_n = \frac{R}{\sqrt{R^2+(2\pi n f C_X)^{-2}}}$$

where n is the harmonic number and *f* is the fundamental frequency. High pass filter attenuation for the first two harmonics at fundamental frequencies used is given in Table 2-1. The measured distortion components are then calculated from the measured spectral amplitudes U_{outn} using

Eq. 2-4: $$U_{hn} = \frac{U_{outn}}{G_{da} \cdot k_n}$$

and the harmonic ratio in dB is obtained from

Eq. 2-5: $$HD_n = 20 \cdot log_{10}\left(\frac{U_{hn}}{U_{exc}}\right).$$

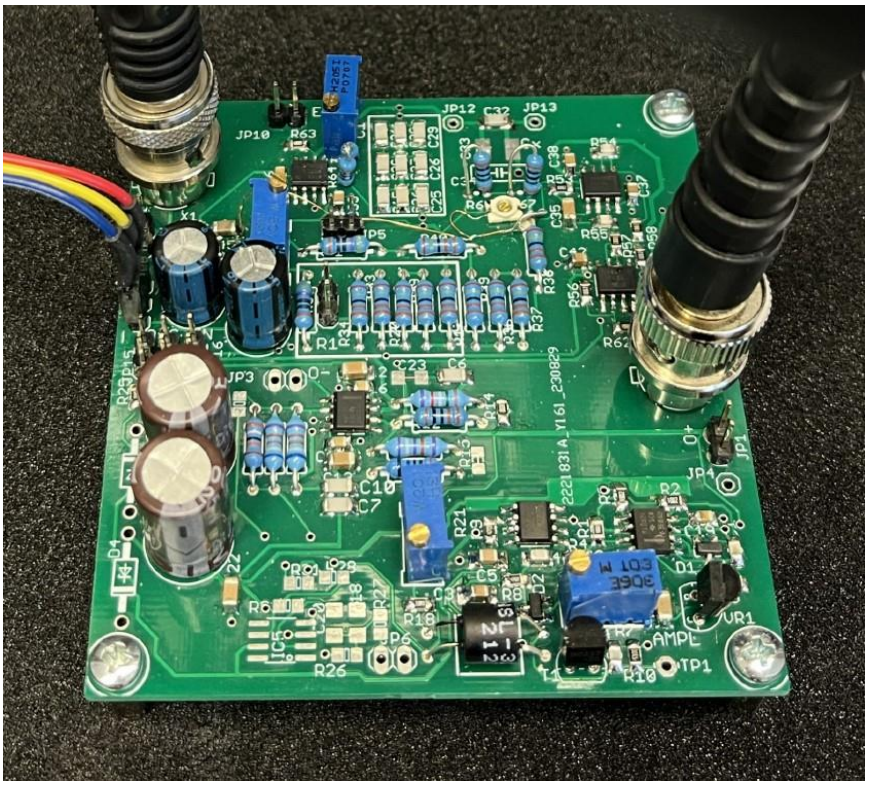


Figure 2-5: Realisation of capacitance bridge where C_{32} is the measured capacitor

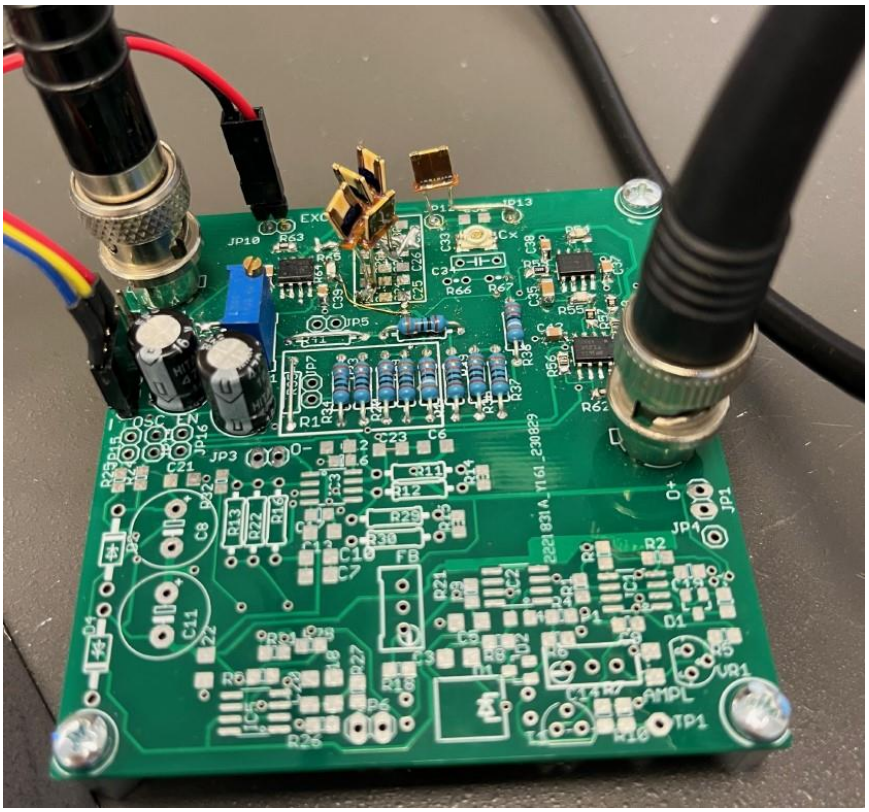


Figure 2-6: Realisation of high-frequency resistance bridge with Vishay bulk metal film 10 kΩ resistors used for reference (2 x 2) and test resistor.

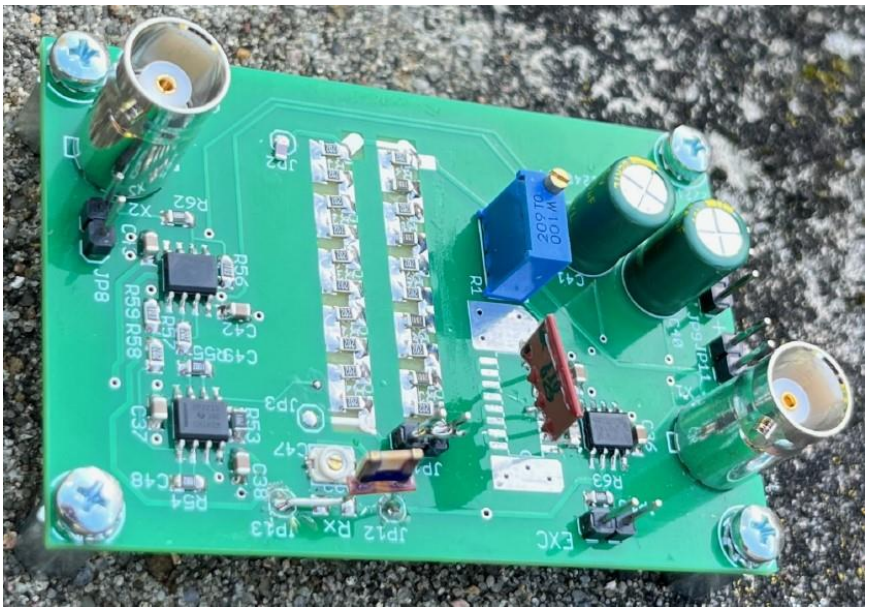


Figure 2-7: Realisation of low-frequency resistance bridge with Vishay bulk metal film 10 kΩ resistor used test resistor.

f (kHz)	2^{nd} harm. (dB)	3^{rd} harm. (dB)
5	−9.1	−6.2
10	−4.4	−2.5
20	−1.6	−0.8

Table 2-1: Capacitor bridge harmonic attenuation relative to selected fundamental frequencies.

The same result (in dBc) can be obtained by adding all ratios in decibels using

Eq. 2-6: $$HD_n = HD_{nm} - G_{da} - k_n - U_{exc}$$

where HD_{nm} is measured harmonic amplitude in dBV, G_{da} is equal to 53.98 dB, k_n is given in Table 2-1 and U_{exc} is bridge upper arm voltage in dBV. HD_n represents the actual capacitor nonlinearity harmonic component when the ideal reference capacitor is used. The effect of reference capacitor is discussed in Chapter 2.2.3.1, which is valid for both resistance and capacitance bridge.

2.2.2.2 Resistance bridge

The resistance bridge does not have any filtering function kn, so its measured harmonic ratio is given in dBc by

Eq. 2-7: $$HD_n = HD_{nm} - G_{da} - U_{exc}$$

Again, this is valid for an ideal reference resistor. The effect of reference resistor is discussed in Chapter 2.2.3.1.

2.2.3 Modelling resistor current nonlinearity

Assume the current model for a non-linear resistor:

Eq. 2-8: $$I = V \cdot (G_1 + G_2 \cdot V + G_3 \cdot V^2),$$

where: G_1 is the nominal conductance, G_2 is the first-order nonlinearity, G_3 is the second-order nonlinearity.

By applying $V(t) = V_0 \cos(\omega t)$ across the resistor, we can substitute $V(t)$ into the current expression:

Eq. 2-9: $$I(t) = V_0 \cos(\omega t) \cdot (G_1 + G_2 \cdot V_0 \cos(\omega t) + G_3 \cdot (V_0 \cos(\omega t))^2)$$

which can be expanded into

Eq. 2-10: $$I(t) = G_1 V_0 \cos(\omega t) + G_2 V_0^2 \cos^2(\omega t) + G_3 V_0^3 \cos^3(\omega t)$$

Using trigonometric identities

Eq. 2-11: $$\cos^2(\omega t) = \frac{1}{2} + \frac{1}{2}\cos(2\omega t)$$
$$\cos^3(\omega t) = \frac{3}{4}\cos(\omega t) + \frac{1}{4}\cos(3\omega t)$$

and substituting them into **Error! Reference source not found.**, current through the nonlinear resistor is given b y

Eq. 2-12: $$I(t) = G_1 V_0 \cos(\omega t) + G_2 V_0^2 \left(\frac{1}{2} + \frac{1}{2}\cos(2\omega t)\right) + G_3 V_0^3 \left(\frac{3}{4}\cos(\omega t) + \frac{1}{4}\cos(3\omega t)\right)$$

The like terms can be combined to isolate the harmonic components:

- DC Component

Eq. 2-13: $$\frac{G_2 V_0^2}{2}$$

- fundamental Component (ω):

Eq. 2-14: $$I_\omega(t) = \left(G_1 V_0 + \frac{3 G_3 V_0^3}{4}\right)\cos(\omega t)$$

which can be immediately simplified for all practical purposes

Eq. 2-15: $$I_\omega(t) \approx G_1 V_0 \cos(\omega t)$$

- second Harmonic Component (2ω):

Eq. 2-16: $$I_{2\omega}(t) = \frac{G_2 V_0^2}{2}\cos(2\omega t)$$

- third Harmonic Component (3ω):

Eq. 2-17: $$I_{3\omega}(t) = \frac{G_3 V_0^3}{4}\cos(3\omega t)$$

The RMS values for each harmonic are then given by fundamental RMS:

Eq. 2-18: $$I_{\omega,test} = \frac{G_1 V_0}{\sqrt{2}}$$

- second Harmonic RMS:

Eq. 2-19: $$I_{2\omega,test} = \frac{G_2 V_0^2}{2\sqrt{2}}$$

- third Harmonic RMS:

Eq. 2-20: $$I_{3\omega,test} = \frac{G_3 V_0^3}{4\sqrt{2}}$$

The second and third harmonic distortions are then given by:

Eq. 2-21: $$h_2 = \frac{I_{2\omega,test}}{I_{\omega,test}} = \frac{G_2 V_0}{2 G_1}$$

and

Eq. 2-22: $$h_3 = \frac{I_{3\omega,test}}{I_{\omega,test}} = \frac{G_3 V_0^2}{4G_1}$$

2.2.3.1 Reference resistor

To analyse how the second and third harmonic distortions in a resistance bridge are affected when the reference resistor configuration compensates for the test resistor's distortion, we need to evaluate how the harmonic distortions are shared and how they impact the overall measurement.

In the bridge configuration, the reference resistors are in a series-parallel combination with the same nonlinearity model, each seeing half the test voltage for four resistors or one-third the test voltage for nine resistors used. Let us assume that the number of reference resistors in series is m and the number of resistors used for a reference is m^2. This means each resistor sees V_0/m voltage that also generates distortion currents and there are m current sources in parallel. Currents for a reference resistor are given by

Eq. 2-23: $$I_{\omega,ref} = \frac{G_1 V_0}{m\sqrt{2}} m = \frac{G_1 V_0}{\sqrt{2}}$$

$$I_{2\omega,ref} = \frac{G_2 V_0^2}{2m^2\sqrt{2}} m = \frac{G_2 V_0^2}{2m\sqrt{2}}$$

$$I_{3\omega,ref} = \frac{G_3 V_0^3}{4m^3\sqrt{2}} m = \frac{G_3 V_0^3}{4m^2\sqrt{2}}$$

Predicted R bridge measurement correction

Clearly, phases of the harmonic currents do not change with the voltage applied across the resistor using this model. This gives us the net harmonic currents for the bridge:

Eq. 2-24: $$I_{2\omega,net} = I_{2\omega,test} - I_{2\omega,ref} = \frac{G_2 V_0^2}{2\sqrt{2}} - \frac{G_2 V_0^2}{2m\sqrt{2}} = \frac{(m-1) G_2 V_0^2}{2m\sqrt{2}}$$

and

Eq. 2-25: $$I_{3\omega,net} = I_{3\omega,test} - I_{3\omega,ref} = \frac{G_3 V_0^3}{4\sqrt{2}} - \frac{G_3 V_0^3}{4m^2\sqrt{2}} = \frac{(m-1) G_3 V_0^3}{4m^2\sqrt{2}}$$

Reduction of the second harmonic measured will be

Eq. 2-26: $$1 - \frac{I_{2\omega,net}}{I_{2\omega,test}} = 1 - \frac{m-1}{m} = \frac{1}{m}$$

and reduction of the third harmonic measured will be

Eq. 2-27: $$1 - \frac{I_{3\omega,net}}{I_{3\omega,test}} = 1 - \frac{m^2-1}{m^2} = \frac{1}{m^2}$$

Example reductions are given in Table 2-2. Measured results can be increased by this number to compensate for the influence of the reference resistor distortion.

m	h_2	h_3
2	50 % (6.02 dB)	25 % (2.50 dB)
3	33% (3.52 dB)	11 % (1.02 dB)

Table 2-2: Harmonic distortion measurement reduction due to reference resistor distortion.

2.2.4 Modelling capacitor current nonlinearity

The charge model for the capacitor is given by:

Eq. 2-28: $Q = VC_1 + V^2C_2 + V^3C_3$

where C_1 is the nominal capacitance, C_2 is a second order non-linearity component and C_3 is a third order non-linearity component.

When a sinusoidal voltage $V(t)$ is applied across the capacitor, harmonics are generated in the current. This derivation finds the second and third harmonic distortions as a function of the applied voltage amplitude.

Assume the applied voltage is:

Eq. 2-29: $V(t) = V_0\cos(\omega t)$

where V_0 is the peak voltage and ω is the angular frequency. Substituting $V(t)$ into the charge expression:

Eq. 2-30: $Q(t) = V(t)C_1 + V(t)^2C_2 + V(t)^3C_3$

and expanding this with $V(t) = V_0\cos(\omega t)$ gives:

Eq. 2-31: $Q(t) = C_1V_0\cos(\omega t) + C_2V_0^2\cos^2(\omega t) + C_3V_0^3\cos^3(\omega t)$

Using trigonometric identities:

Eq. 2-32: $\cos^2(\omega t) = \frac{1}{2} + \frac{1}{2}\cos(2\omega t)$

$\cos^3(\omega t) = \frac{3}{4}\cos(\omega t) + \frac{1}{4}\cos(3\omega t)$

we substitute these into $Q(t)$:

Eq. 2-33: $Q(t) = C_1V_0\cos(\omega t) + C_2V_0^2\left(\frac{1}{2} + \frac{1}{2}\cos(2\omega t)\right) + C_3V_0^3\left(\frac{3}{4}\cos(\omega t) + \frac{1}{4}\cos(3\omega t)\right)$

Expanding and combining terms, we get:

Eq. 2-34: $Q(t) = \left(C_1V_0 + \frac{3C_3V_0^3}{4}\right)\cos(\omega t) + \frac{C_2V_0^2}{2} + \frac{C_2V_0^2}{2}\cos(2\omega t) + \frac{C_3V_0^3}{4}\cos(3\omega t)$

Since $I(t) = \frac{dQ}{dt}$, differentiate each term with respect to time:

- The DC term $\frac{C_cV_0^2}{2}$ has zero derivative.
- The fundamental term $\cos(\omega t)$:

Eq. 2-35: $\frac{d}{dt}\left(\left(C_1V_0 + \frac{3C_3C_0^3}{4}\right)\cos(\omega t)\right) = -\omega\left(C_1V_0 + \frac{3C_3V_0^3}{4}\right)\sin(\omega t)$

- The second harmonic term $\cos(2\omega t)$:

Eq. 2-36: $\frac{d}{dt}\left(\frac{C_2V_0^2}{2}\cos(2\omega t)\right) = -\omega C_2V_0^2\sin(2\omega t)$

- The third harmonic term $\cos(3\omega t)$:

Eq. 2-37: $\frac{d}{dt}\left(\frac{C_3V_0^3}{4}\cos(3\omega t)\right) = -\frac{3\omega C_3V_0^3}{4}\sin(3\omega t)$

Thus, the current $I(t)$ becomes:

Eq. 2-38: $I(t) = -\omega\left(C_1V_0 + \frac{3C_3V_0^3}{4}\right)\sin(\omega t) - \omega C_2V_0^2\sin(2\omega t) - \frac{3\omega C_3V_0^3}{4}\sin(3\omega t)$

The harmonic components of *I(t)* are:

- Fundamental Component (*ω*):

Eq. 2-39: $$I_{\omega}(t) = -\omega\left(C_1 V_0 + \frac{3C_3 V_0^3}{4}\right)\sin(\omega t)$$

- Second Harmonic Component (2*ω*):

Eq. 2-40: $$I_{2\omega}(t) = -\omega C_2 V_0^2 \sin(2\omega t)$$

- Third Harmonic Component (3*ω*):

Eq. 2-41: $$I_{3\omega}(t) = -\frac{3\omega C_3 V_0^3}{4}\sin(3\omega t)$$

The RMS values for each harmonic component are:

- Fundamental RMS:

Eq. 2-42: $$I_{\omega,RMS} = \frac{\omega}{\sqrt{2}}\left(C_1 V_0 + \frac{3C_3 V_0^3}{4}\right)$$

- Second Harmonic RMS:

Eq. 2-43: $$I_{2\omega,RMS} = \frac{\omega C_2 V_0^2}{\sqrt{2}}$$

- Third Harmonic RMS:

Eq. 2-44: $$I_{3\omega,RMS} = \frac{3\omega C_3 V_0^3}{4\sqrt{2}}$$

If C_3 is small, the contribution to the fundamental component can be neglected, simplifying:

Eq. 2-45: $$I_{\omega,RMS} \approx \frac{\omega C_1 V_0}{\sqrt{2}}$$

The RMS values for the harmonic components remain:

Eq. 2-46: $$I_{2\omega,RMS} = \frac{\omega C_2 V_0^2}{\sqrt{2}} \text{ and } I_{3\omega,RMS} = \frac{3\omega C_3 V_0^3}{4\sqrt{2}}$$

The second and third harmonic distortions (h_2 and h_3) are defined as the ratios of the RMS values of the second and third harmonic components to the RMS value of the fundamental component.

- Second Harmonic Distortion:

Eq. 2-47: $$h_2 = \frac{I_{2\omega,RMS}}{I_{\omega,RMS}} = \frac{\frac{\omega C_2 V_0^2}{\sqrt{2}}}{\frac{\omega C_1 V_0}{\sqrt{2}}} = \frac{C_2 V_0}{C_1}$$

- Third Harmonic Distortion:

Eq. 2-48: $$h_3 = \frac{I_{3\omega,RMS}}{I_{\omega,RMS}} = \frac{\frac{3\omega C_3 V_0^3}{4\sqrt{2}}}{\frac{\omega C_1 V_0}{\sqrt{2}}} = \frac{3C_3 V_0^2}{4C_1}$$

Predicted C bridge measurement correction

These expressions show that the second and third harmonic distortions in the capacitor current depend

on the nonlinearity coefficients C_2 and C_3, the nominal capacitance C_1, and the peak voltage V_0 the same way as given for reference resistors in Eq. 2-23. Therefore, the same ratios are established, and the same compensations apply for the capacitance bridge as given in Table 2-2.

2.3 Simulations using LTSpice

2.3.1 Using ideal components

Simulations were performed using ideal components to study the bridge response in comparison to digitally assisted bridge. The simulated circuit is shown in Figure 2-8. This simulation was designed to scan over most of the bridge component parameters, which are the same for TEST circuit and DIGITAL QUADRATURE bridge. For all simulations performed using any expected levels of source distortion, feedback amplifier distortion and bridge imbalances, no meaningful differences between TEST circuit and DIGITAL QUADRATURE bridge sections were observed. REFERENCE circuit was implemented to compare TEST circuit response with non-linear reference resistors to ideal reference resistors.

By sweeping the input voltage from 1 V to 10 V, the response in dBc relative to the input voltage (see Eq. 2-7) is shown in Figure 2-9. Figure 2-10 shows the ratio of TEST circuit to REFERENCE circuit response during this sweep. This result is in perfect alignment with the theoretical prediction given in Table 2-2. Another sweep shown here varies relative resistor distortion coefficients from 10^{-10} to 10^{-8}. The residual fundamental component measured would be −29 dB (R_d = 10.0001 kΩ, C_l = 2.1 pF), which was the level which was typically not crossed during the measurements.

By setting the bridge strongly out of balance (R_d = 10.02 kΩ, C_l = 2.5 pF), which is far more than is normally achieved, the resulting bridge behaviour is shown on Figure 2-12 and Figure 2-13. These results show that the bridge unbalance shall be kept small, with the resulting fundamental component measured at the output of the bridge at or below −20dBV.

Another example shows a possible effect when the reference resistor distortion is larger than the test resistor distortion. Both harmonic components for reference resistors were set to $R_{r2}/R_r = R_{r3}/R_r = 10^{-9}$, while the test resistor harmonic components ratios were steeped from 10^{-10} to 10^{-8}. The result is shown in Figure 2-14. As expected, the second harmonic is completely cancelled at 50% the reference resistor distortion level, while the third harmonic was completely cancelled at 25% the reference resistor distortion level, as given in Table 2-2. An important conclusion here is that the reference resistors shall be either with the same linearity as the test resistor and a correct harmonic compensation can be applied, or they should have much lower nonlinearity so that no correction is needed. Clearly, by knowing the reference nonlinearity components beforehand, good compensations can also be made. However, all this is true as long as harmonic phase relations remain the same for all resistors involved. A similar discussion is valid bridge lover hands. While they are identical, their non-linearity is practically not important. Any difference will show at a bridge output and can either increase or decrease the measured value. For that reason, it is best to select the best linear components also for lower arms or provide another test for their difference evaluation.

2.3.2 Using real components

LTSpice simulations were also run on a modified quadrature bridge using manufacturer models for operational amplifiers used. Additionally, separate calculations were performed to analyse the performance of the instrumentation amplifier to amplify bridge signals by a factor of 500. Spice simulations were performed to verify the modified capacitor bridge concept. All simulations were performed using LTSpice XVII [6]. The simulations were carried out using the circuit diagram shown in Figure 16, where ideal operational amplifier models were used for the instrumentation amplifier to increase the speed and reduce the simulation complexity. A classic instrumentation amplifier circuit topology was used [7], with 0.1% tolerance feedback and gain setting resistors. The performance of this instrumentation amplifier was simulated and its CMRR performance above 100 dB was confirmed, as shown in Figure 2-15. This ensures proper operation of the modified capacitance or resistance bridge, as the bridge itself removes common mode signal due to its feedback architecture. However, this is not the case in a classical digital-assisted bridge, which is powered by two signal sources.

Further analysis of the bridge imperfections of the modified quadrature bridge is given in Chapter 2.6. This analysis shows that the bridge can perform as intended for all measurement results presented in this report.

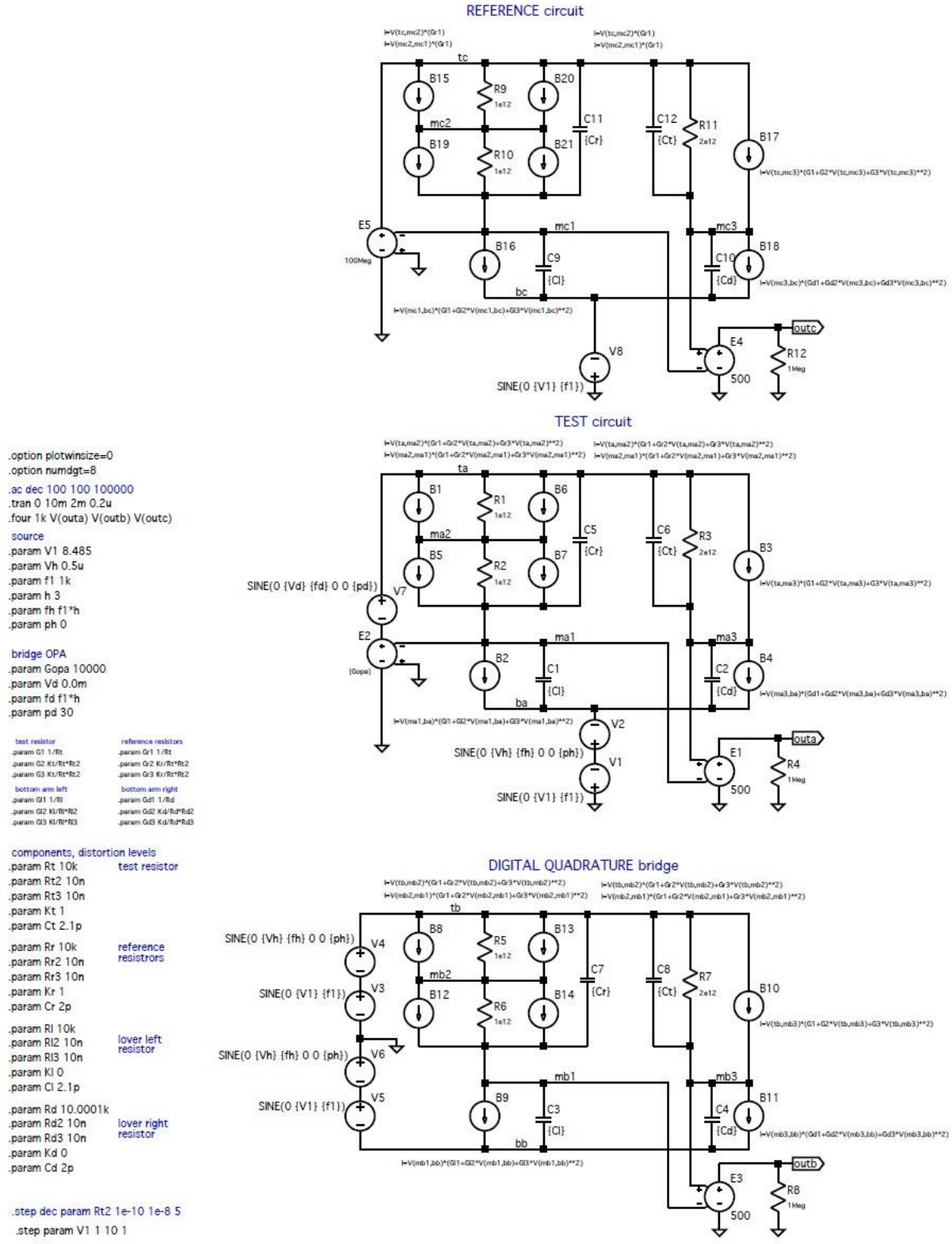


Figure 2-8: Resistor bridge simulation using ideal components and nonlinear resistors models given by Eq. 2-8.

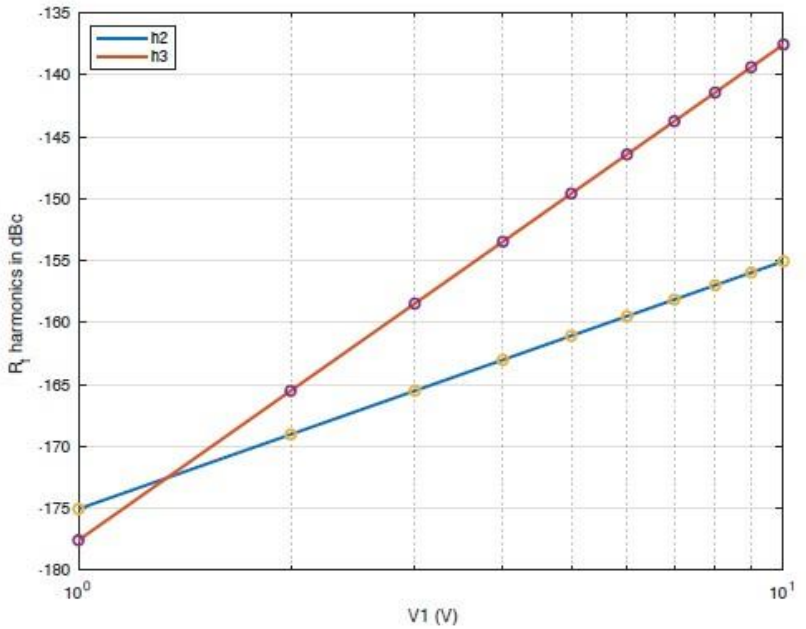


Figure 2-9: Resistor bridge harmonic distortion (h_2 and h_3) response for bridge TEST circuit (line) and DIGITAL QUADRATURE bridge (circles) as a function of input voltage.

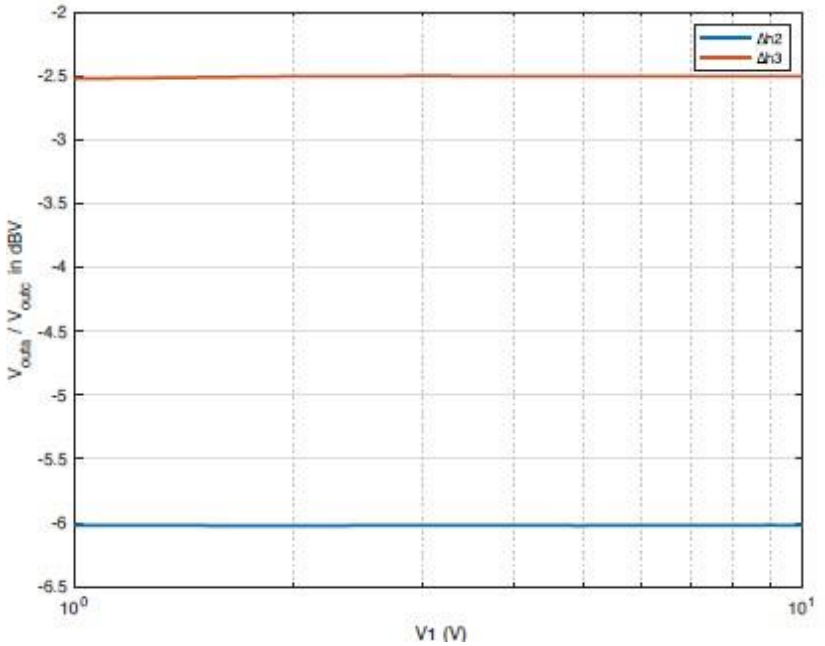


Figure 2-10: Resistor bridge h_2 and h_3 response ratio between TEST circuit and REFERENCE circuit as a function of input voltage.

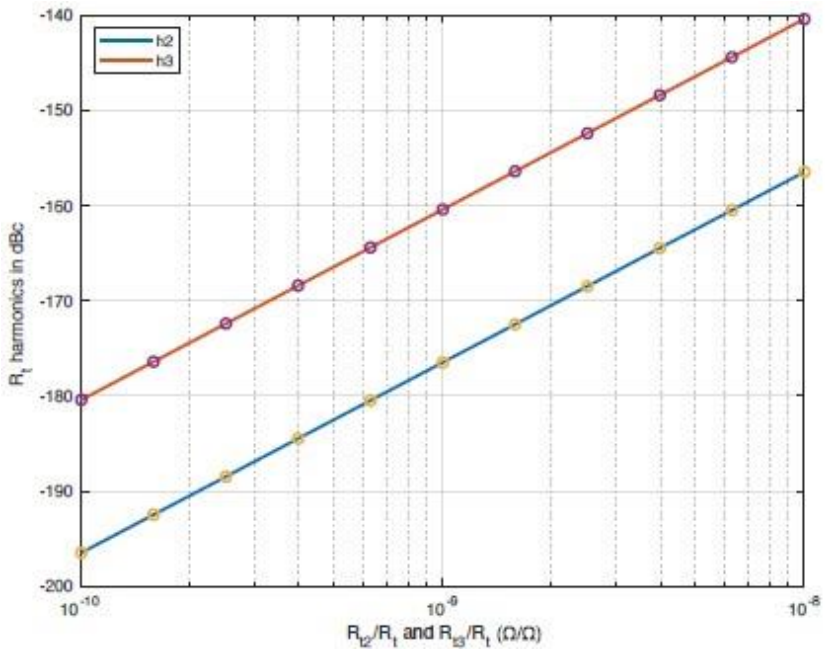


Figure 2-11: Resistor bridge response to varying resistor nonlinearity and keeping the bridge slightly out of balance (V_{res} = −29 dBV).

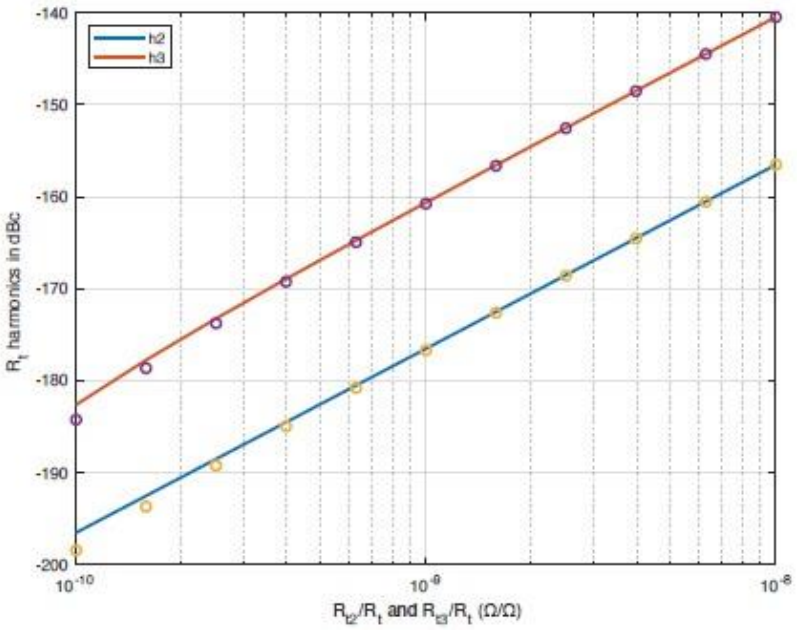


Figure 2-12: Resistor bridge response to varying resistor nonlinearity and keeping the bridge strongly out of balance (V_{res} = 12.5 dBV). The difference between the TEST circuit (line) and the DIGITAL QUADRATURE bridge (circles) starts to appear and it increases by decreasing harmonic levels.

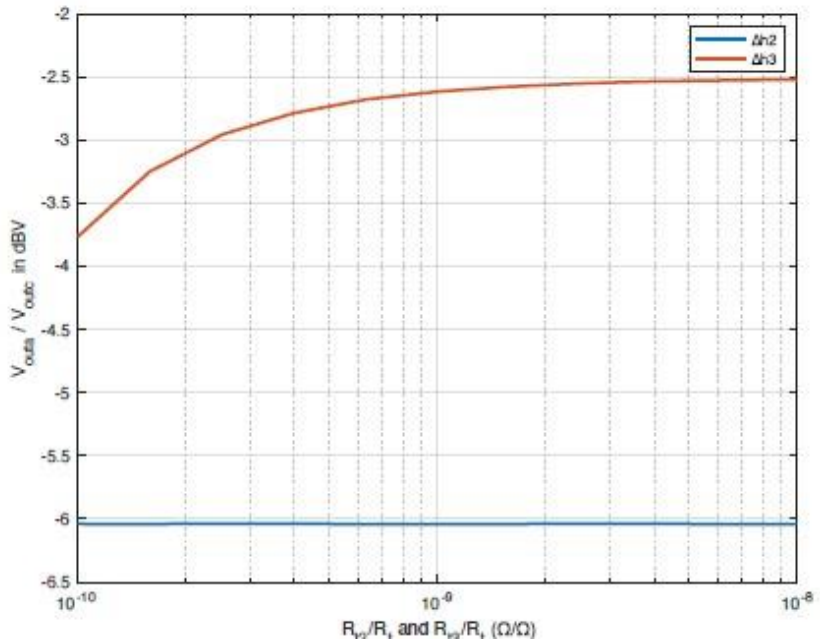


Figure 2-13: Resistor bridge response to varying resistor nonlinearity and keeping the bridge strongly out of balance.

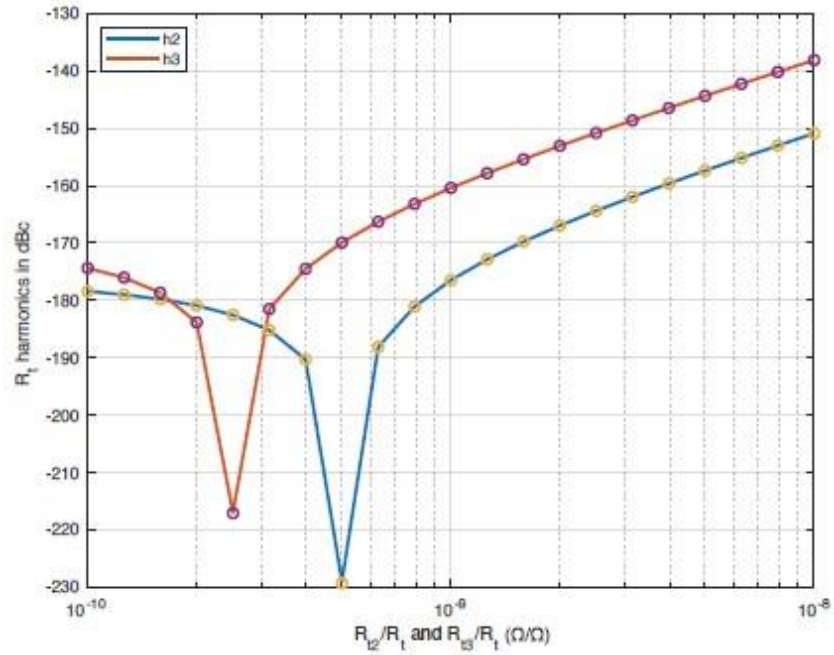


Figure 2-14: Resistor bridge response to varying test resistor nonlinearity and keeping the reference resistor nonlinearity components at $R_{r2}/R_r = R_{r3}/R_r = 10^{-9}$. The bridge was slightly out of balance.

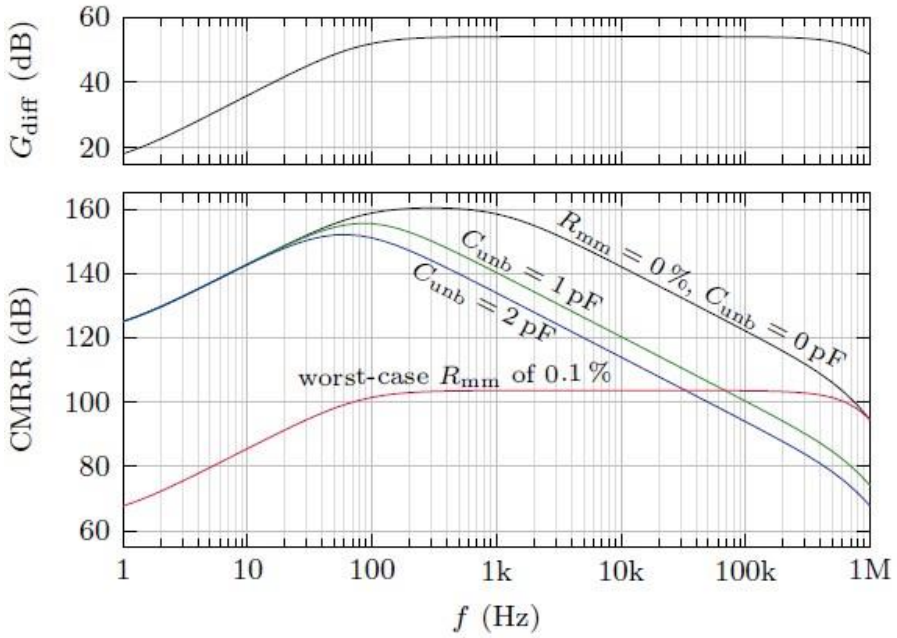


Figure 2-15: Common mode rejection ratio (CMRR) for simulated instrumentation amplifier with gain G_{diff} = 500 and using full models for OPA1656. Rmm stands for instrumentation amplifier gain resistors mismatch and C_{unb} stands for C_{s1} and C_{s2} circuit board stray capacitance mismatch (see Figure 2-16).

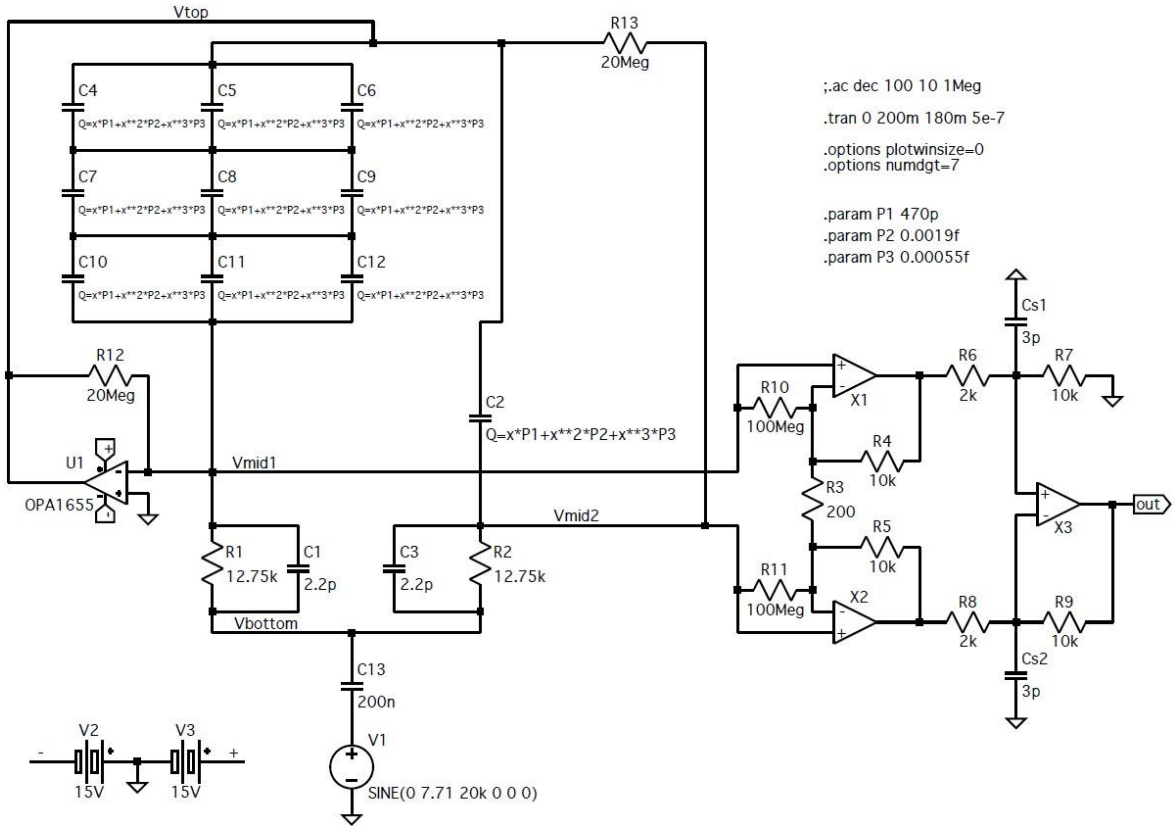


Figure 2-16: LTSpice simulation circuit used to identify capacitor polynomial voltage dependence model. C_{s1} and C_{s2} are stray PCB capacitances, whose mismatch degrades the instrumentation amplifier CMRR (see Figure 2-15), while their actual value at the pF level does not impair the circuit behaviour.

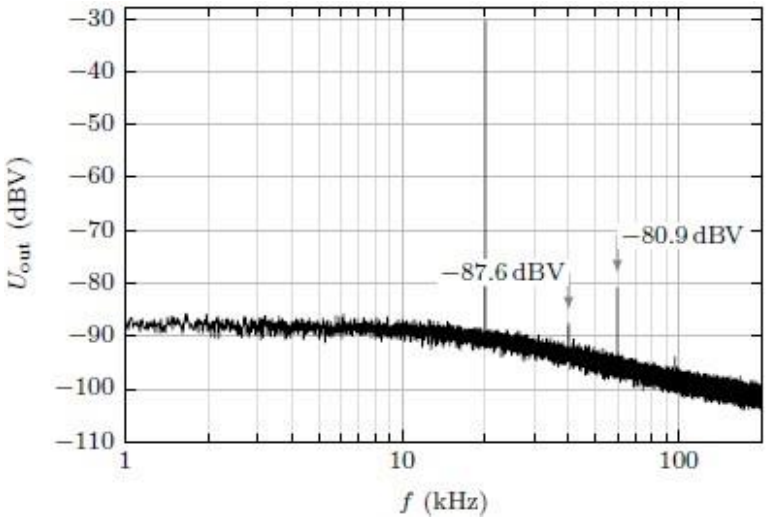


Figure 2-17: U_{out} spectrum obtained for the balanced bridge at U_{exc} = 7.07 V at the frequency of 20 kHz. The second and third harmonics are indicated by their measured values.

2.4 Measurement methodology

Different resistors and capacitors were measured for their distortion and some results were already published in [8]. Bridge circuits were realised on a common PCB design. For the capacitance bridge, the PCB was populated with test and reference capacitors, as shown on Figure 2-5. For the resistance bridge, the PCB was populated with test and reference resistors, as shown in Figure 2-6. Both bridges have the lover legs populated with metal film resistors, connected in series to reduce their overall distortion and average their response to be as similar as possible between these two legs. Two measurement setups were used:

- Of-the-shelf signal generator for bridge excitation and 10-bit oscilloscope for output spectral analysis. The measured spectrum is shown on Figure 2-17.
- ApX555 audio spectrum analyser, which provided excellent performance both on the generator and analyser side, with harmonic distortions below −120 dBc and low noise levels. The measured spectrum is shown on Figure 2-18. While a dynamic range is clearly better, it was later further improved by optimising the ApX555 FFT analyser settings, allowing for reliable readings of U_{out} down to −122 dBV.

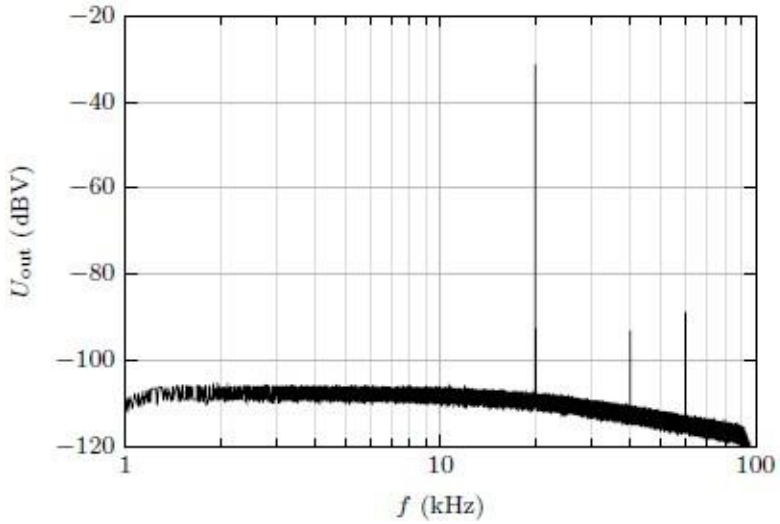


Figure 2-18: U_{exc} = 7.071 V, 54 averages

2.5 Results and analysis

A series of measurements were performed, looking for the effects of various bridge components on the actual test resistor distortion result. To better understand these effects, theoretical calculations and circuit simulations were performed as detailed in Chapters 2.2 and 2.3. In summary, the following conclusions were drawn:

- The modified bridge is simple to operate, as it only requires a single signal source and a spectral analyser.
- The instrumentation used can have harmonic distortion up to −80 dBc to measure component distortions down to −160 dBc.
- Using better instrumentation (ApX555 in our case), even better performance can be achieved. The input signal low distortion (<110 dBc) will not affect resulting performance even for larger bridge unbalance. The low noise and low distortion (<110 dBc) digitizer with records up to 1.2 MS allows for distortion components measurements down to −170 dBc.
- The bridge performance is limited by the components used in the bridge arms and by the instrumentation used. The amplifiers within the bridge were not identified as a limiting factor at frequencies tested (e.g. from 5 Hz to 20 kHz fundamental frequency).
- The reference component should have smaller non-linearities than the measured component, as the bridge cannot differentiate the source of nonlinearity. For the best components available, this can be achieved using a series-parallel configuration with the same components as the one under the test. The measurement can then give the upper bound distortion for the test component when correction due to reference is used (see Chapter 2.2.3.1 and 2.2.4).
- The bridge lower legs need to have the same distortion (amplitude and phase). Any difference would show as a signal in the output spectrum and would add to the measured test component nonlinearity signal in a complex way, depending on the phase of the distortion. That can be achieved using a number of metal film resistors in series. This was actually implemented and there were no issues identified with this configuration. For the ultimate implementation and to remove any doubt, the highest linearity resistors identified could be used also in lower legs using a parallel-serial configuration.

Results obtained on 470pF 630 V 1206-size NP0 capacitors are summarised in Table 2-3.

Measurement results for 10 kΩ 1/4 W through hole metal film resistor are given in Table 2-4. Measurement results for Susumu SMD 10 kΩ resistor are given in Table 2-5.

f (kHz)	U_{exc} (V)	U_{in} (V)	2^{nd} harm. (dBc)	3^{rd} harm. (dBc)
5	7.07	1.37	−164.1	−159.5
10	7.07	2.73	−163.5	−158.7
20	7.07	5.46	−159.9	−158.1
20	3.54	2.73	−166.4	−170.6
20	2.35	1.81	<−167.5*	−170.3

Table 2-3: Measured harmonics amplitude for 470 pF NP0 capacitor relative to generated U_{exc} and recalculated for capacitor bridge harmonic attenuation using a low distortion audio test system. * marks the noise level at the frequency of expected harmonic. These results are compensated for reference capacitor distortion (3 x 3 NP0 capacitors) using values from Table 2-2.

f (kHz)	U_{exc} (V)	U_{in} (V)	2^{nd} harm. (dBc)	3^{rd} harm. (dBc)
5	7.07	7.07	−161.3	−162.0
10	7.07	7.07	−154.4	−163.6
20	7.07	7.07	−145.3	−161.8
20	3.54	3.54	−150.9	<−166.9*
20	2.35	2.35	−154.0	<−163.3*

Table 2-4: Measured harmonics amplitude for 10 kΩ 1/4 W through hole metal film resistor, relative to generated U_{exc}. * marks the noise level at the frequency of the expected harmonic. These results are not compensated for reference resistor distortions.

f (kHz)	U_{exc} (V)	U_{in} (V)	2^{nd} harm. (dBc)	3^{rd} harm. (dBc)
1	7.10	7.07	−170.5	−155.2
2	7.10	7.07	−167.4	−156.3
5	7.10	7.07	−162.1	−158.0
10	7.10	7.07	−153.8	−156.9
20	7.10	7.07	−145.7	−160.1

Table 2-5: Measured harmonics amplitude for 10 kΩ Susumu SMD resistor, relative to generated U_{exc}. * marks the noise level at the frequency of expected harmonic. These results are not compensated for reference resistor distortions.

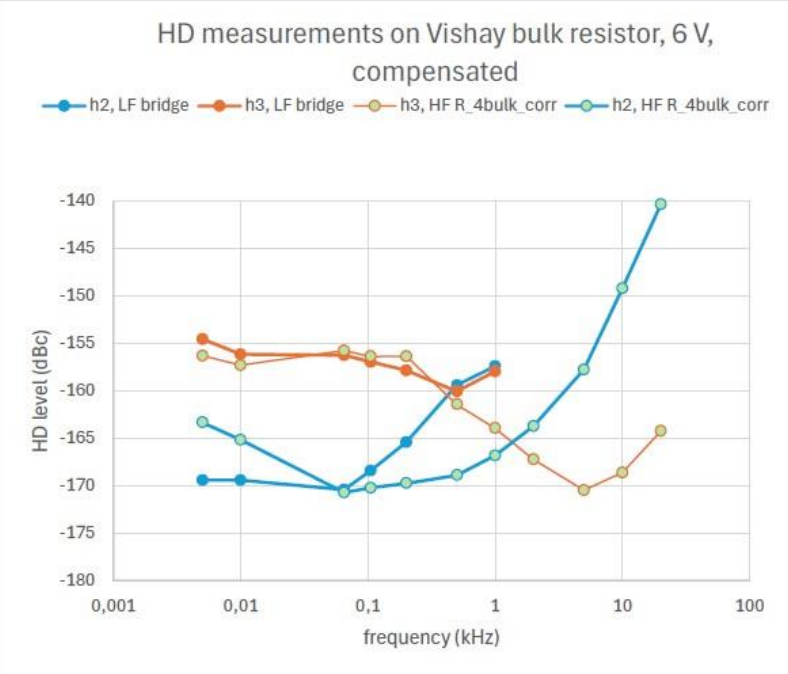


Figure 2-19: Measured harmonics amplitude for 10 kΩ Vishay Bulk metal foil resistor, relative to generated U_{exc}. These results are compensated for reference resistor distortion (2 x 2 10 kΩ Vishay Bulk metal foil resistors) using values from Table 2-2.

Final measurements were performed on Vishay 10 kΩ bulk metal foil resistors, which were also used as a reference resistor in 2 x 2 series-parallel configuration. Results are compensated for reference resistor distortion using values from Table 2-2 for m = 2 and are presented on Figure 2-19. Measurements using the LF bridge were made to confirm the operation of the HF bridge. For h_3, results agree very well, except at 1 kHz, where the LF bridge started to deviate from the expected performance. For h_2 results deviate more, which is not completely understood. However, the smooth frequency response using HF bridge is believed to present the actual performance of the measured resistors on the higher frequency end. On the lower frequency end, the HF bridge is close to its detection limit its results were corrected for its high pass filter with a corner frequency at 200 Hz. Therefore, these measurements were not reliable as they were pushed into the noise due to this filter, hence the noise level was measured instead of actual harmonics. This explains the elevated HF bridge h_2 results at 5 Hz (filter correction is 18.1 dB) and 10 Hz (filter correction is 12.3 dB)). Taking these comments into account, the final results for Vishay Bulk metal foil resistor are presented in Figure 2-20, showing the best performance down to −170 dBc for both the second and third harmonic component.

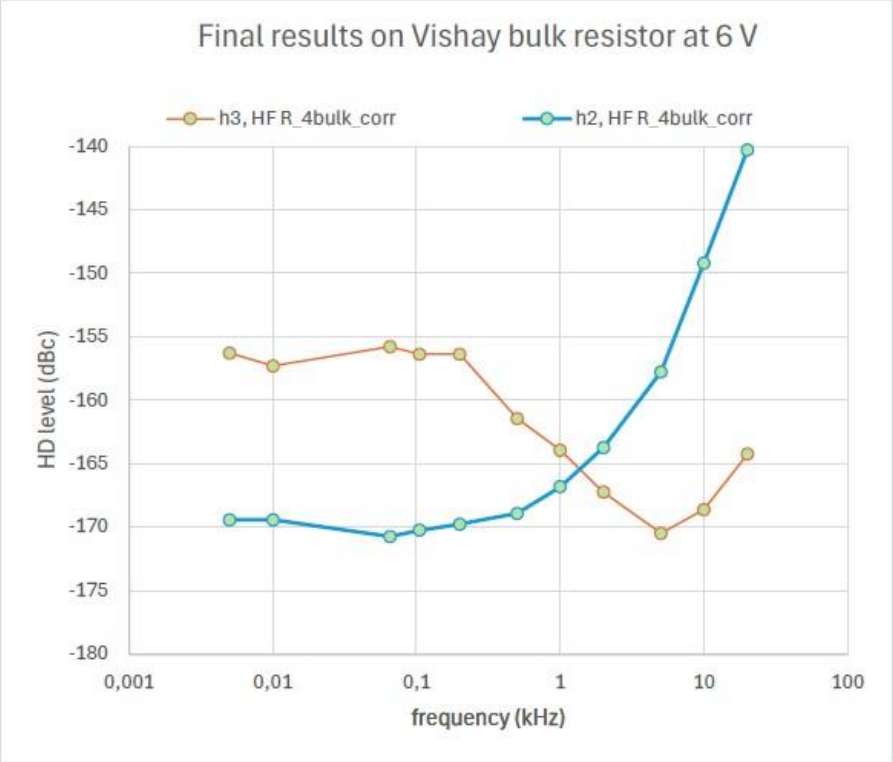


Figure 2-20: Final harmonics amplitude for 10 kΩ Vishay Bulk metal foil resistor, relative to generated U_{exc}.

2.6 Detailed bridge analysis

2.6.1 Analysis of imperfections of the quadrature bridge

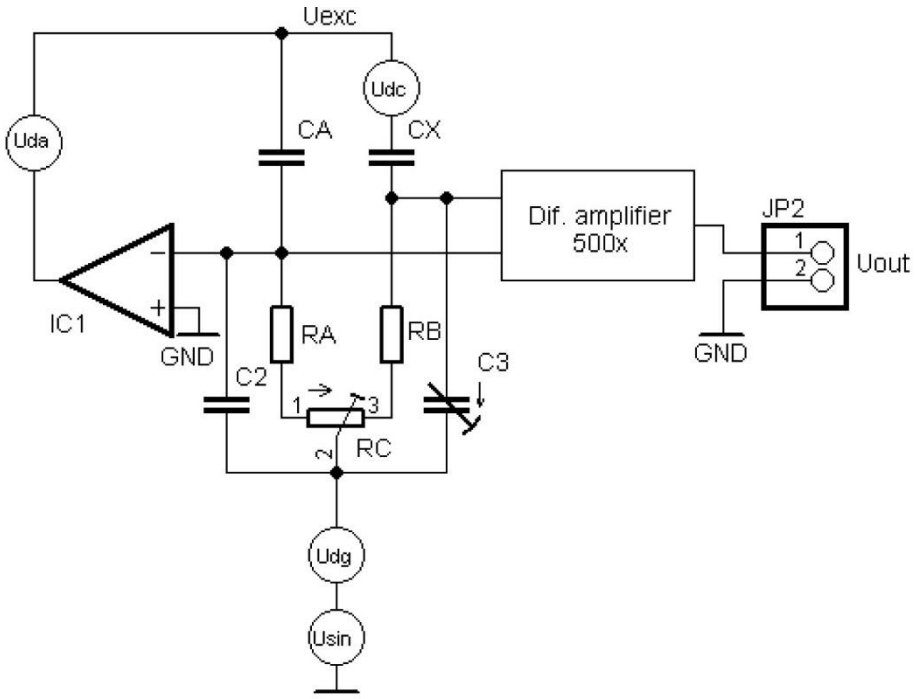


Figure 2-21: Block diagram of the bridge

A perfectly balanced bridge with an ideal amplifier IC_1 and a differential amplifier eliminates any distortion coming from the generator, only distortion from C_X appears at the output of the bridge and is amplified by the differential amplifier. A real bridge with a real amplifier isn't perfectly balanced and the amplifier has finite gain and some distortion, so the impact of those imperfections was evaluated. Distortion coming from the generator, IC_1 and measured capacitor C_X is modelled as corresponding voltage sources U_{dg}, U_{da} and U_{dc}, see Figure 2-21 and their influence was computed and simulated. Requirements for a digitizer sampling the output of the differential amplifier are also evaluated.

The whole circuit simulated in LTSpice is shown in Figure 2-22. Modifications of Figure 2-21 that better reflect a real circuit were made.

1. C_A and C_X differ by 1%, R_B was changed accordingly to keep the bridge close to the balance.

2. R_{12} was added to close DC feedback around IC_1 and R_{13} was added for symmetry.

3. OPA1556 were used instead of ideal operational amplifiers.

4. R_B and C_3 were slightly changed to get a small unbalance of the bridge with a similar value as was measured on the real bridge – see Chapter 2.5.

5. R_6 - R_9 were changed to reflect the worst-case error 0.1%.

6. C_5 was added to simulate the influence of unequal parasitic capacitances in the differential amplifier. Those modifications will be evaluated in the next paragraphs.

Bridge unbalancing

The bridge was slightly unbalanced to better reflect real achievable balancing. Simulated transfer function from U_{dg} to the output shows that the unbalancing isn't frequency independent - see Figure 2-23.

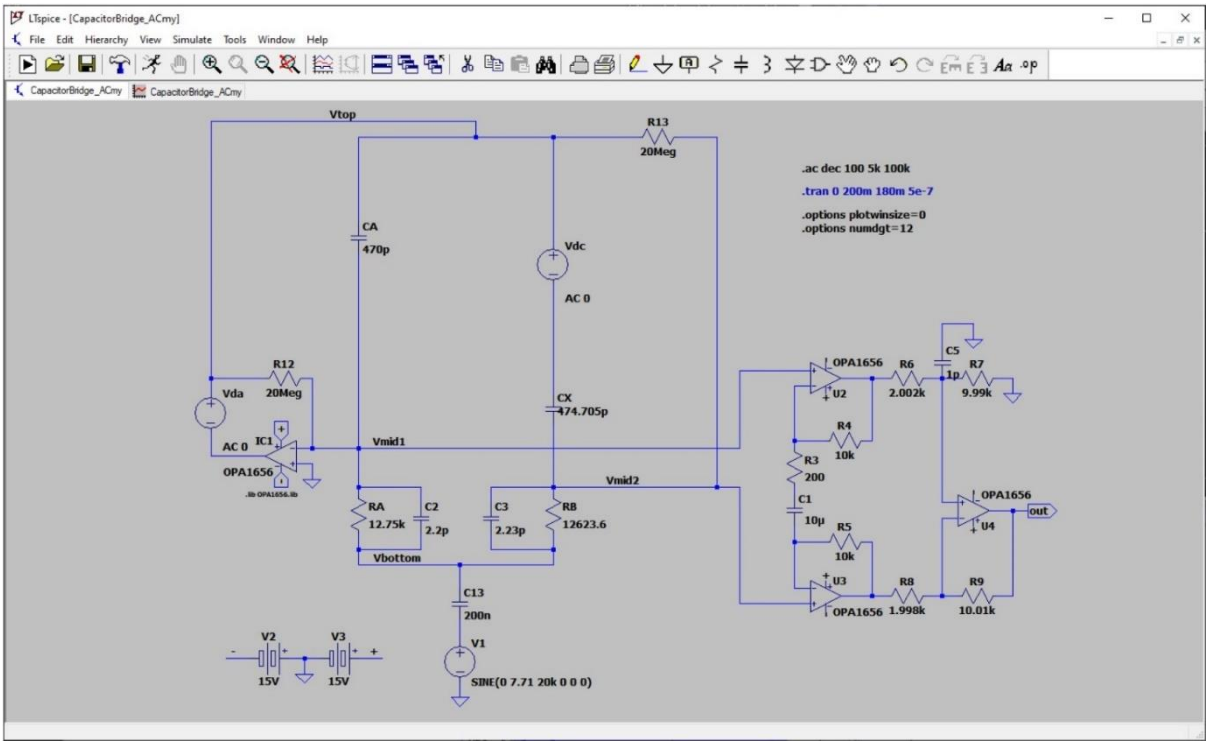


Figure 2-22: LTSpice schematic

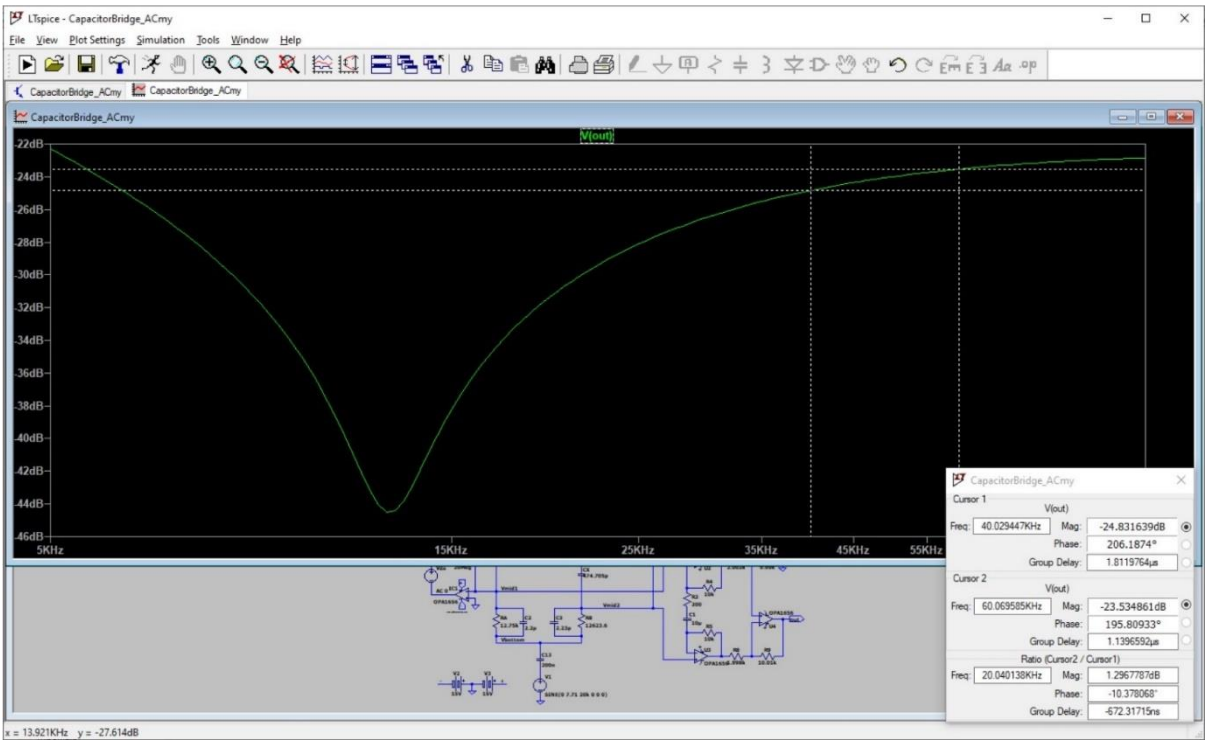


Figure 2-23: Bridge balancing

Excitation voltage with amplitude 7.71 V_P = 5.45 V_{RMS} = 14.7 dBV was used for simulation, this voltage generates 20 V_{PP} on the tested capacitor. The fundamental has amplitude -31 dBV on the output, 2nd harmonic is -25 dBV, 3rd harmonic is -24 dBV, the differential amplifier has a gain of 54 dB, so the attenuation of the bridge is 100 dB for the fundamental, and 94 dB for 2nd harmonic and 93 dB for 3rd harmonic. We assume to use a generator with THD better than -70 dB (DG992 fulfil this), so we got 2nd harmonic < -95dBV and 3rd harmonic < -94 dBV on the amplifier's output coming from the generator's THD.

C_X distortion transfer to the output with high-pass filter see Table 2-1 in our article, simulation – Figure 2-24 confirms the computed results in our article.

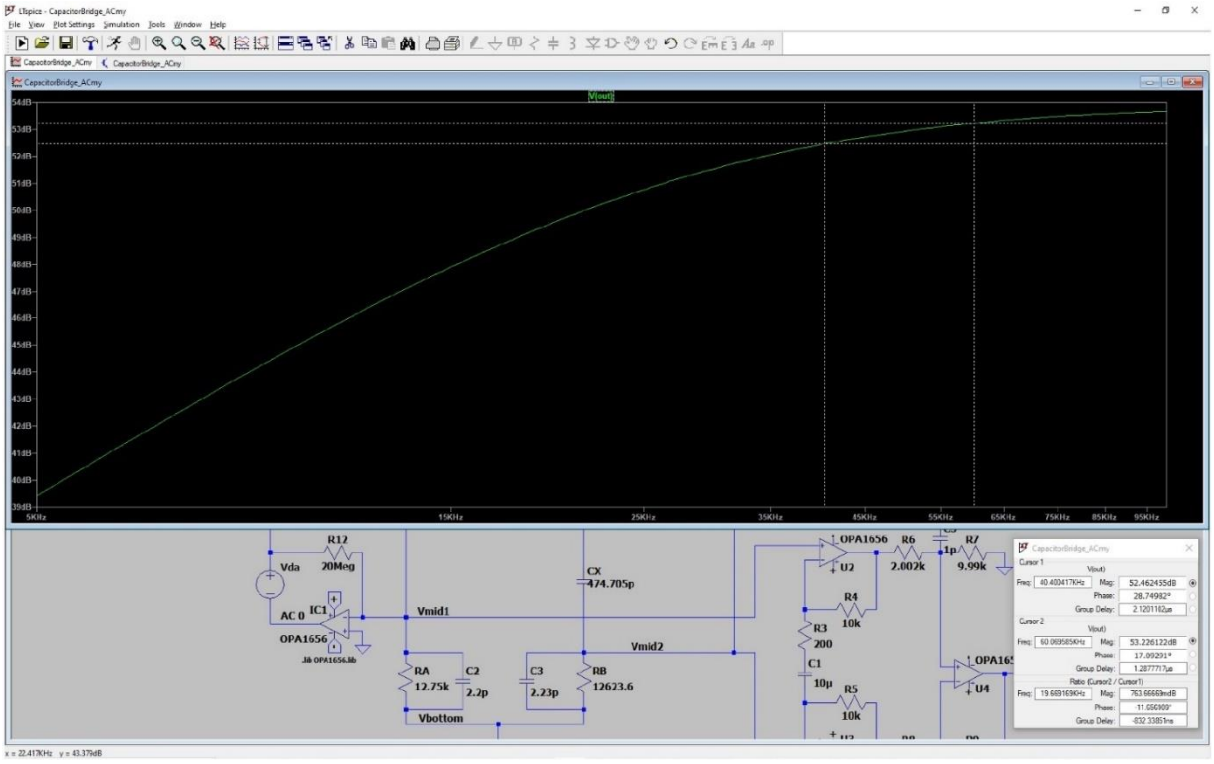


Figure 2-24: Capacitor C_X distortion transfer

The gain of the amplifier is 54 dB, attenuation for 2nd harmonic is 1.6 dB, for 3rd harmonic 0.8 dB, so the resulting gain is 52.4 dB for 2nd harmonic and 53.2 dB for 3rd harmonic matches the simulated results.

We require a distortion measurement range up to -160 dB, with applied voltage 20 V_{PP} = 7.071 V_{RMS} = 17 dBV on the tested capacitor, which presents 2nd harmonic on the output of the amplifier higher than 17 – 160 + 52.4 = -90.6 dBV and 3rd harmonic > -89.8 dBV.

Influence of *IC₁*

IC_1 suffers from two main non-idealities – finite gain and distortion. Finite gain manifests as a non-zero voltage U_{mid} at the middle point and appears as a common mode voltage on the input of the differential amplifier.

Eq. 2-49: $$U_{mid} = \frac{U_{exc}}{A_{ol}}$$

In Eq. 2-49 U_{exc} is the voltage on the amplifier's output, A_{ol} is open loop gain $A_{ol} = \frac{GBW}{f}$, where GBW is the gain bandwidth product of the amplifier – 53 MHz for OPA1656 and f is frequency. It is also true that

Eq. 2-50: $$U_{exc} = \frac{U_{sin} \cdot |Z_{CA}|}{R_A} = \frac{U_{sin}}{2} \cdot \pi \cdot f \cdot R_A \cdot C_A.$$

From those equations we get

Eq. 2-51: $$U_{mid} = \frac{U_{sin}}{2} \cdot \pi \cdot R_A \cdot C_A \cdot GBW = \frac{U_{sin}}{1996}$$

so U_{sin} is attenuated by 66 dB.

Simulation in Figure 2-25 confirms this computation. The fundamental is attenuated by 100 dB by the bridge itself, so keeping attenuation of this voltage >120 dB requires a differential amplifier with CMRR > 54 dB. Such requirements can be fulfilled easily, and our amplifier is significantly better as will be shown later.

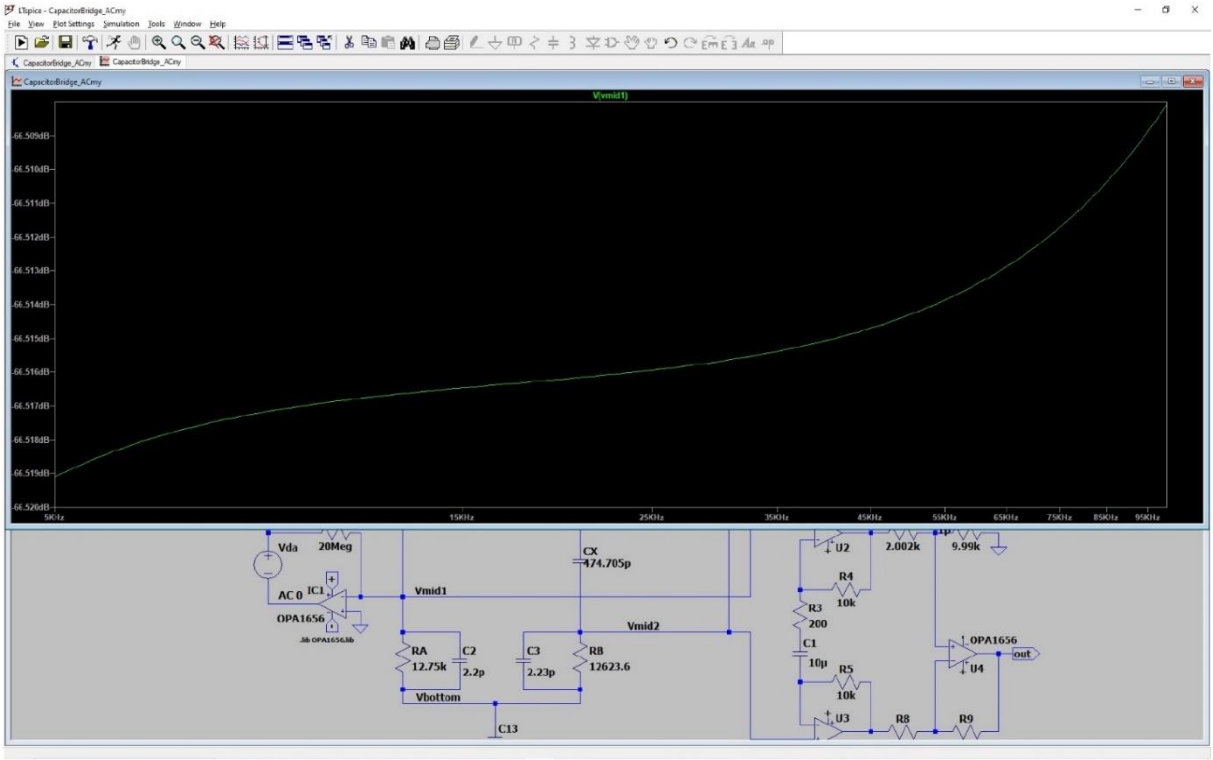


Figure 2-25: V_{mid1} voltage

Distortion of IC_1 is high-pass filtered by C_AR_A and C_XR_B R_C filters and appears on the output of the bridge again as a common mode signal, which is attenuated by the differential amplifier. A simulated transfer from the IC_1's output (V_{da} = 7.071 V_{RMS} was used for simulation) to the differential amplifier's output is shown in Figure 2-26. Simulation shows -26 dBV for 2nd harmonic and -22 dBV for 3rd harmonic, but IC_1 has THD < -120 dB at 20 kHz [from datasheet], so 2nd harmonic and 3rd harmonic from IC_1 appears with amplitude -146 dBV and -142 dBV on the amplifier's output, well below the -90 dBV limit given by C_X's distortion.

Simulation of IC_1 distortion includes the effect of the differential amplifier, specifically its finite CMRR, but the simulation of the effect of finite gain doesn't, so the CMRR of the differential amplifier was evaluated separately.

CMRR of a simple difference amplifier (U4) coming from [9] is approximately CMRR = (A_D+1) / 4t, where A_D is the gain of the amplifier, t is resistor tolerance, here A_D = 5, t = 0.001, CMRR = 63.5 dB. The input stage (U_2, U_3) with a gain of 40 dB adds another 40 dB, so the total CMRR of the complete differential amplifier is about 103.5 dB at low frequencies. The simulation shown in Figure 2-27: CMRR simulation confirms this computation, decrease of CMRR at higher frequencies is caused by C_5 modelling unbalancing from parasitic capacitances on the PCB.

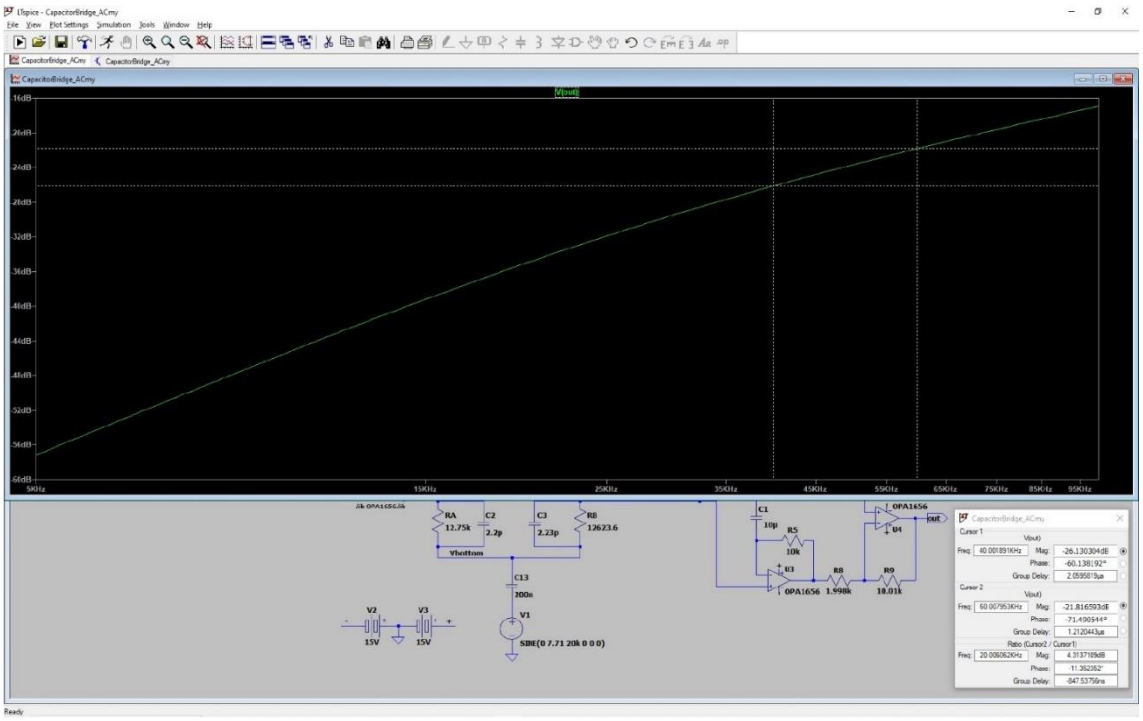


Figure 2-26: Transfer from V_{da} to V_{out}

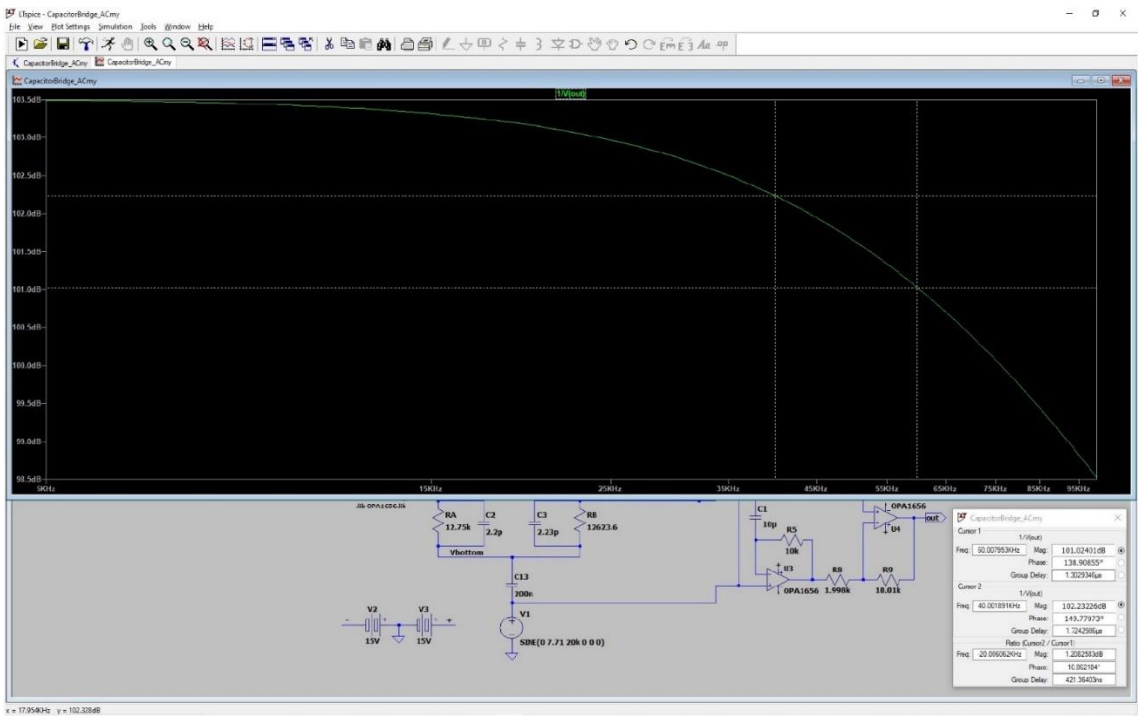


Figure 2-27: CMRR simulation

Digitizer requirements

Amplitude of the fundamental coming from an imperfect balancing of the bridge on the output is about -30 dBV, for -160 dB THD of measured capacitor it is necessary to resolve higher harmonics with an amplitude of about -90 dBV, so the used digitizer has to have SFDR better than 60 dB.

3. CHARACTERIZATION OF RESISTORS

3.1 Introduction

This report focuses on the characterization of resistor elements, specifically the stability and tracking of the resistance value (or ratio of two resistor elements) with temperature and humidity.

A set of resistor components to be tested with different nominal values and types was established and supplied by the partner CERN.

The characterization presented in this report is related to the variation of the ratio between paired resistors elements of resistor networks with the temperature and humidity variation. The preliminary interval of temperature and humidity values were defined with the following sequences:

- Temperature values at fixed humidity:

  (15, 25, 35, 45, 35, 25, 15) °C at a fixed RH = 50 %

- Humidity values at fixed temperature:

  (20, 40, 60, 80, 60, 40, 20) % RH at a fixed temperature = 25 °C

The time at each temperature/humidity value was defined as a minimum of 12 hours.

The measurement method and system used were based on the ratio measurement capability of the multimeter Fluke 8508A and are presented and analysed in Chapter 3.2.

The measurement results for 4 different types of resistors are presented in Chapter 3.3.

3.2 Measurement method

The measurement method was based on the direct resistance measurements with the “ohm ratio function” of the multimeter Fluke 8508A. This measurement function allows the sequential measurement of the two inputs available in the multimeter and gives directly the ratio of the two measured resistances. The advantage compared to more accurate (and stable) instruments like resistance bridges is the relatively reduced time needed to perform the measurements being this relevant when it is desired to make a large number of measurements.

When the selected measurement range of the two inputs is the same, the measurement uncertainty specification of the multimeter Fluke 8508A is dominated by the short-term noise and linearity.

As the main goal of our characterization is focused on the variability of the ratio with temperature and humidity and not on the absolute value of the ratio, the short-term noise and eventual thermal errors will be the main components of the measurement uncertainty.

A test of the system was made measuring the ratio of standard resistors in temperature-controlled conditions (air bath). The system includes a scanner and is shown in Chapter 0.

The results are presented in the Figure 3-1 and Table 3-1. The “true ohm” function was used for the ratios 100 Ω/100 Ω and 10 kΩ/10 kΩ and the “normal ohm” function for the 10 kΩ/100 kΩ and 100 kΩ/100 kΩ.

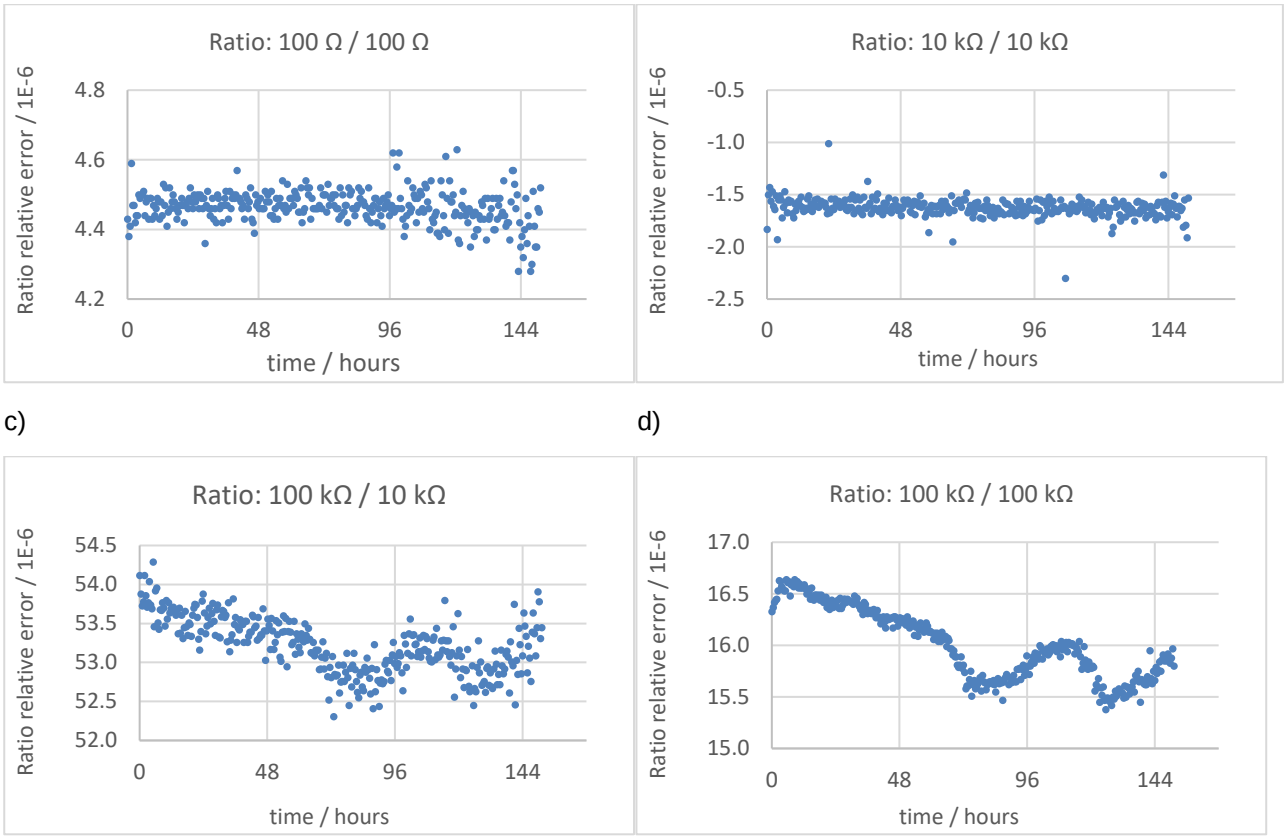
The measurements of Figure 3-1 c and d show an identical drift over the first half of the measurement period. This could be related to the common standard resistor of 100 kΩ used in both measurements (Guildline, model 9330).

The consecutive measurements lasted 6 days and produced 337 values for each ratio. The variability of the results evaluated by the standard deviation of each set of values is lower than $1x10^{-6}$. This variability decreases

by an order of magnitude (to 10^{-8} and 10^{-9}) considering the standard deviation of the mean and gives the expected magnitude to the measurement uncertainty of the method based on this measurement system.

The better values for measurements stability were obtained for the multimeter lower ranges (200 Ω and 20 kΩ) used for the ratio 100 Ω/100 Ω and 10 kΩ/10 kΩ and where it was also available the “true ohm” function.

a) b)



c) d)

Figure 3-1: Relative error of the resistance ratio measured with the multimeter Fluke 8508A. a) and b) used the “true ohm” function; c) and d) used the “normal ohm” function.

Table 3-1: Mean value and standard deviation of the relative error of 337 consecutive values of the ratio measured for different pairs of resistors identified in Figure 3-1.

Ratio	Mean value	Std	Std (mean)
	$1x10^{-6}$		
100 kΩ / 100 kΩ	4.47	0.05	0.003
10 kΩ / 10 kΩ	-1.62	0.09	0.005
100 kΩ / 10 kΩ	53.22	0.36	0.020
100 kΩ / 100 kΩ	16.01	0.34	0.019

3.2.1 Measuring setup

The measurement setup is presented in the following photos.

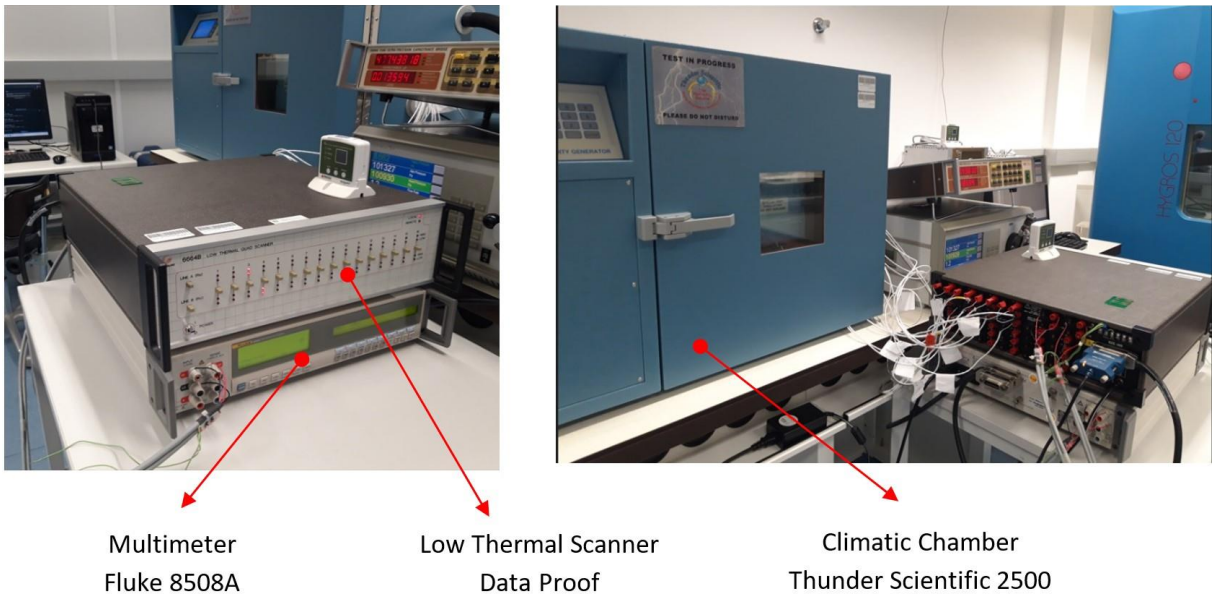


Figure 3-2: Measurement setup

The resistors tested under the temperature and humidity conditions generated by the climatic chamber were connected to the low Thermal Scanner with 16 4-wire input channels. The 2 selectable outputs of the scanner were connected to the front and rear inputs of the multimeter.

A script in python was developed to control the scanner and the multimeter. The measurements of the ratio between the front and rear input of the multimeter were done sequentially and continuously for the tested resistors.

The multimeter was configured to its highest resolution (8 bits) and at 4-wires ohms measurement function. Depending on the ohm range needed for measurements, the “true-ohm” function was selected. With this function, each measurement is repeated with reversed polarity to reduce the thermal effects.

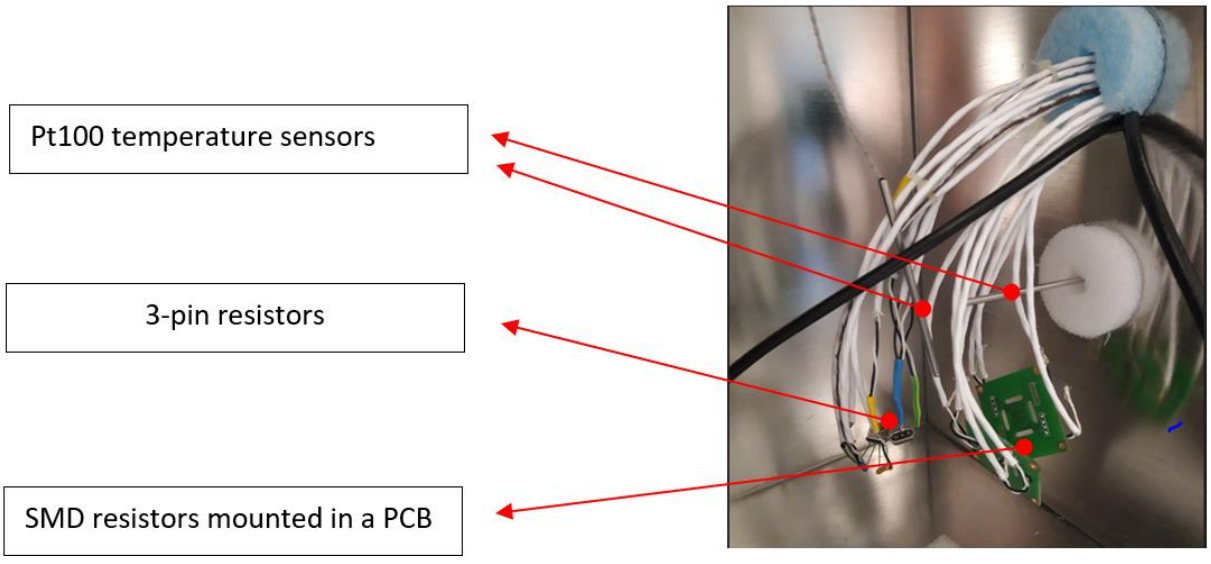


Figure 3-3: Resistors mounted inside the climatic chamber

3.3 Results

The results presented below are related to the resistor networks shown in Table 3-2.

Table 3-2: Resistors used

Identification	Reference	Parameters	Notes
Resistor_1	Y0000321866	10 K / 10 K	Hermetic 3-pin THD package, matched pair
Resistor_2		10 K / 35 K	
Resistor_3	Y1365V0008QT0U	10K / 10K / 10K / 10K	Plastic SO-8 SMD package
Resistor_4	Y1485V0001BA0L	10K / 10K	Plastic 3-pin SMD package

For Resistor_3, the tested elements were the 2nd and 3rd. Resistor_3 and Resistor_4 were mounted in a PCB.

The results presented in the following section are based on the relative error (reference to the nominal value) of the measured ratio.

3.3.1 Temperature test

Figure 3-4 to Figure 3-7 present the results obtained for the tested resistors at 4 steps of temperature and the fixed relative humidity of 50 %. The measurements were made consecutively for the 4 resistors and in a continuous way for the entire period of the measurements (4 days).

The initial step at 15 °C had a duration of 12 hours and all the other steps of temperature lasted 14 hours each. The temperature curve in all figures is the same, covering the identical period. Before the beginning of the testes, the resistors were for approximately 2.5 days under the initial conditions of 15 °C and 50 %RH.

Table 3-3 presents the mean value and its standard deviation of the relative error of the ratio for each step of temperature. The mean value was calculated for 40 consecutive measurements approximately distributed around the middle of the step. In this way, it was intended to avoid spikes and the transition values at the limits of the temperature steps.

All resistors tested show a ratio dependence on the temperature.

Resistor_1 and Resistor_4 show a well-defined and fast response to the temperature change. It is also noticed hysteresis (difference of the ratio relative error for the same temperature step) when returned from the maximum temperature: 0.68 ppm (at 25 ºC) and 0.57 ppm (at 35 ºC), respectively.

Resistor_2 seems to react significantly only to the higher temperature step (45 ºC), followed by high inertia to recover the ratio values in the temperature decrease cycle. The maximum value for hysteresis is found at 35 ºC and equal to 3.3 ppm.

Resistor_3 only reacts to the temperature change step of 35 ºC. The maximum value for hysteresis is found at 35 ºC and equal to 0.57 ppm.

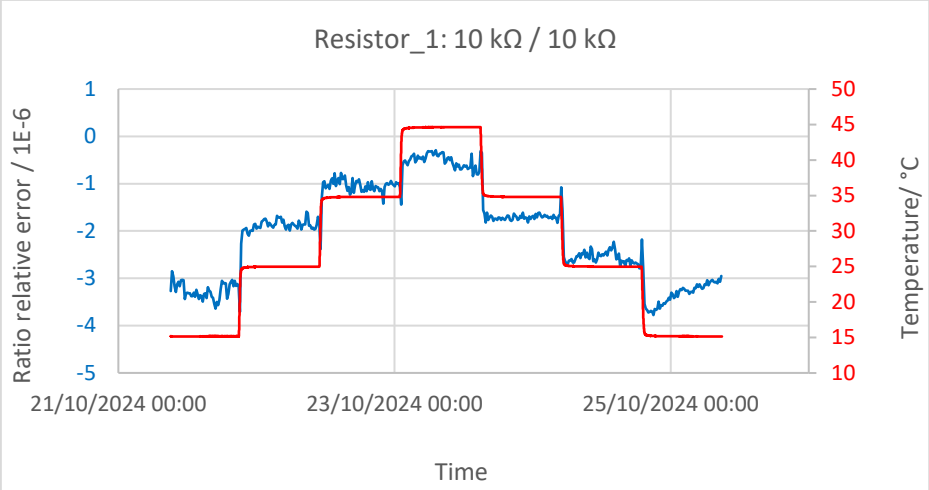


Figure 3-4: Results for Resistor_1

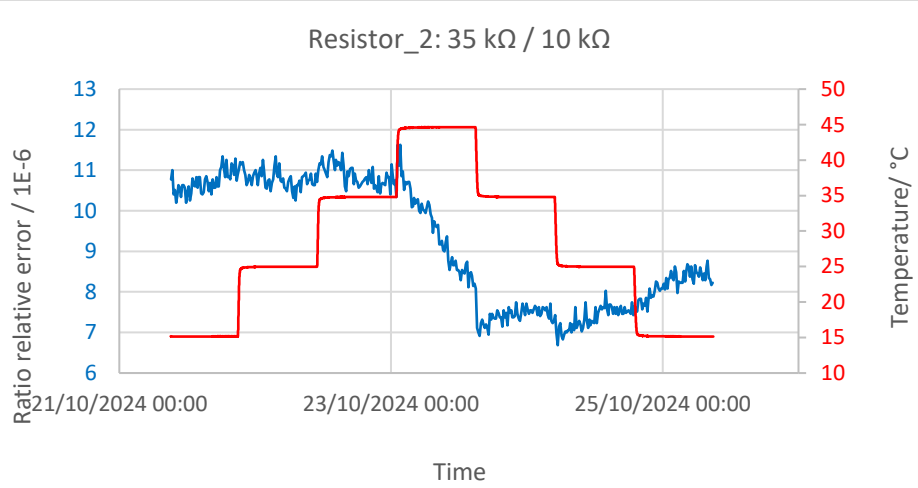


Figure 3-5: Results for Resistor_2

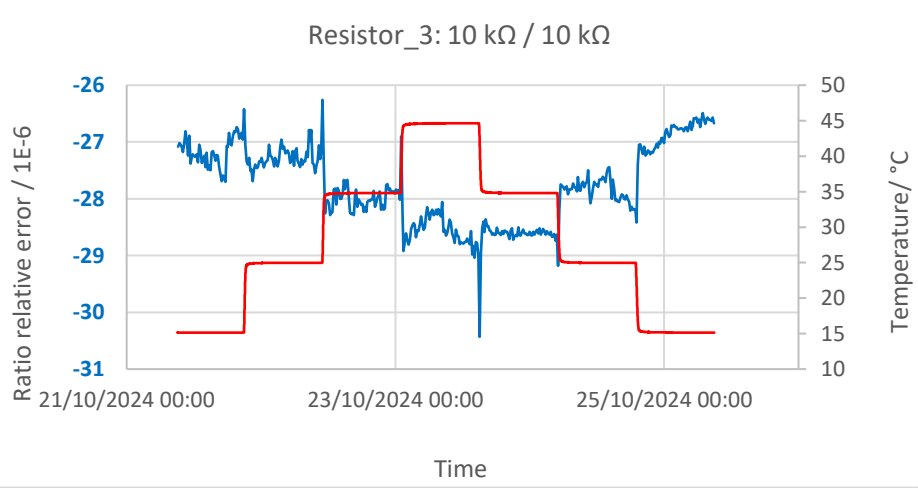


Figure 3-6: Results for Resistor_3

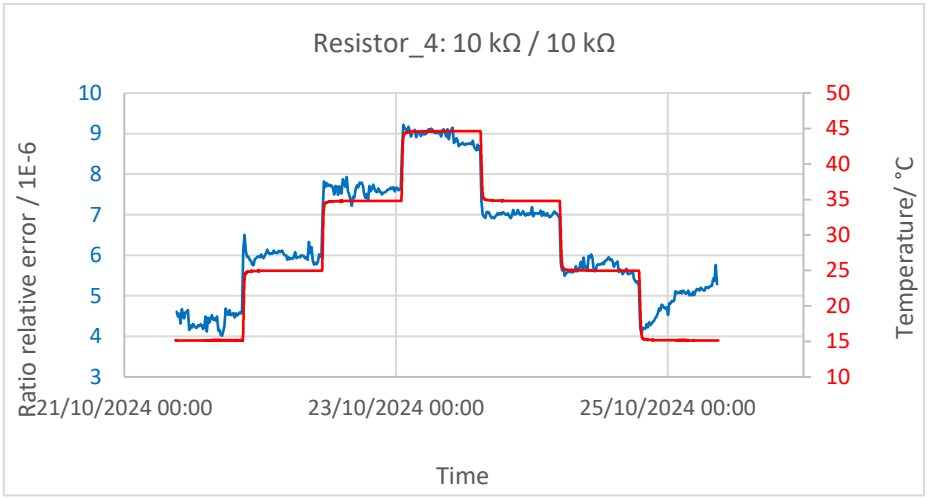


Figure 3-7: Results for Resistor_4

Table 3-3: Mean value and standard deviation of the mean for the relative error of the measured ratio

Temperature Step	Resistor_1		Resistor_2		Resistor_3		Resistor_4	
	Mean	Std (mean)	Mean	Std (mean)	Mean	Std (mean)	Mean	Std (mean)
°C	$1x10^{-6}$							
15	-3.31	0.02	10.72	0.04	-27.22	0.04	4.36	0.03
25	-1.85	0.02	10.73	0.03	-27.25	0.03	5.99	0.02
35	-1.06	0.02	10.79	0.03	-28.01	0.03	7.59	0.02
45	-0.48	0.02	9.43	0.10	-28.47	0.03	8.95	0.02
35	-1.71	0.01	7.47	0.02	-28.60	0.01	7.02	0.01
25	-2.53	0.02	7.45	0.03	-27.80	0.03	5.75	0.02
15	-3.30	0.02	8.29	0.04	-26.81	0.03	4.96	0.03

3.3.2 Humidity test

Figure 3-8 to Figure 3-11 present the results obtained for tested resistors at 4 steps of Humidity and the fixed temperature of 25 °C. The measurements were made consecutively for the 4 resistors and continuously for the entire period of the measurements (4 days).

The previous temperature test ran at 50 %. Therefore, an initial step at 10 % was done to ensure a starting point at a low value of humidity.

All steps of humidity lasted 14 hours. The humidity curve in all figures is the same, covering the identical period.

The results show that the ratio is less dependent on the humidity change than the temperature.

Table 3-4 presents the mean value and its standard deviation of the relative error of the ratio for each step of humidity. The mean value was calculated for 40 consecutive measurements approximately distributed around the middle of each step.

Resistor_1 and Resistor_2 show to be low sensitivity to humidity variation. The difference between the maximum and minimum values for the ratio error over all the humidity interval variations is 0.2 ppm and 0.9 ppm, respectively.

For Resistor_3 and Resistor_4, this difference increases to 2.9 ppm and 1.9 ppm, respectively, and show clearly a linear dependence on the humidity. The variation of the ratio error from the step 20 % to 80 % is -2.7 ppm and 1.9 ppm, respectively.

The repeatability (standard deviation of the mean) of the ratio values obtained has the same order of magnitude of 10^{-8} for all steps of humidity tested.

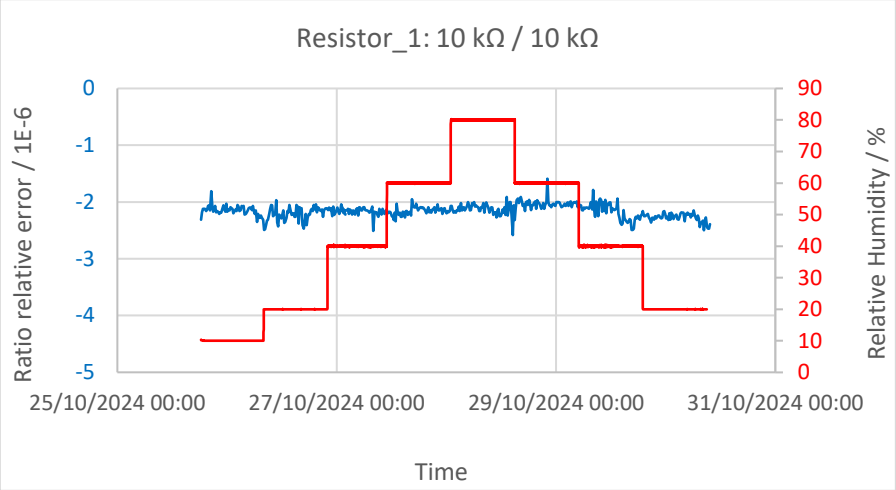


Figure 3-8: Results for Resistor_1

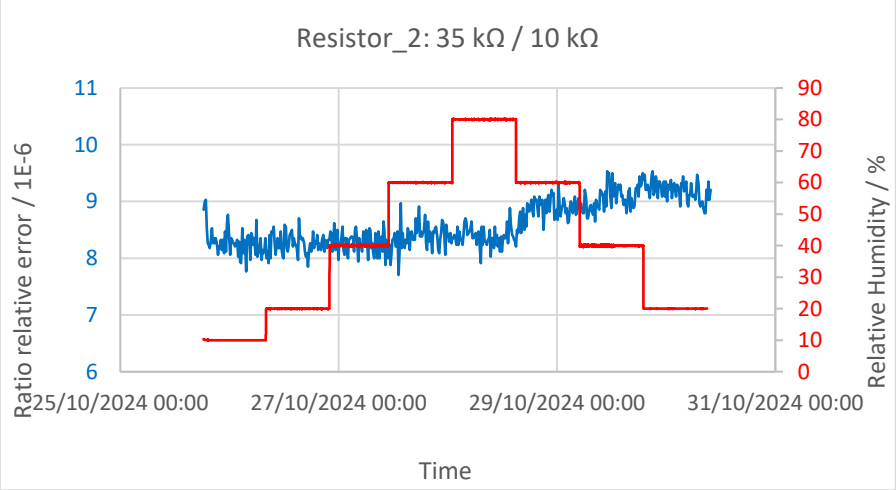


Figure 3-9: Results for Resistor_2

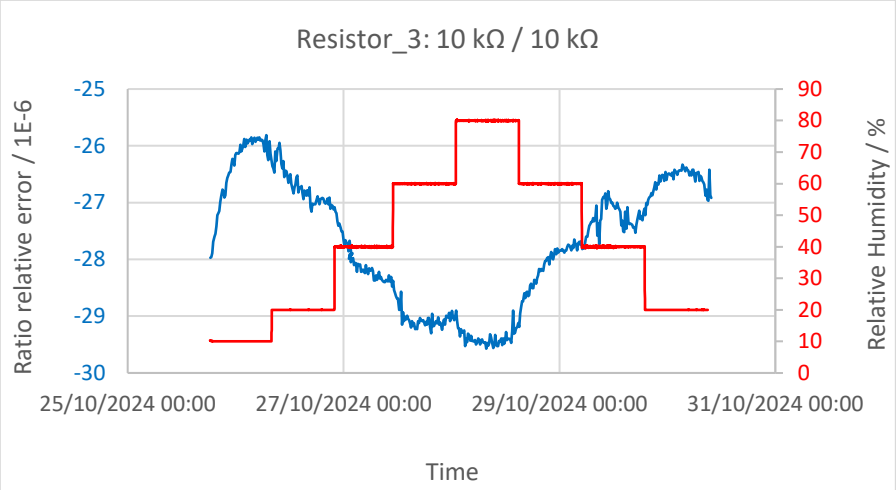


Figure 3-10: Results for Resistor_3

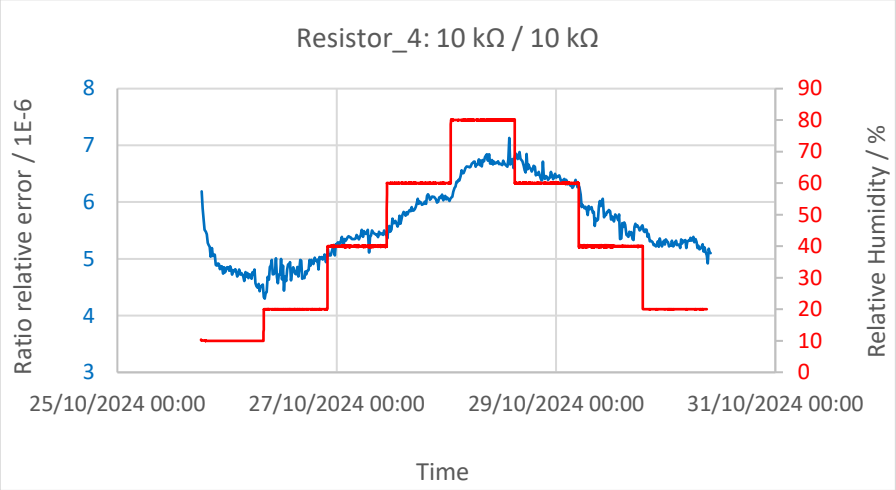


Figure 3-11: Results for Resistor_4

Table 3-4: Mean value and standard deviation of the mean for the relative error of the measured ratio

Humidity Step	**Resistor_1**		**Resistor_2**		**Resistor_3**		**Resistor_4**	
	Mean	Std (mean)	Mean	Std (mean)	Mean	Std (mean)	Mean	Std (mean)
%	$1x10^{-6}$							
20	-2.22	0.02	8.26	0.03	-26.68	0.05	4.78	0.02
40	-2.17	0.01	8.27	0.03	-28.25	0.02	5.41	0.01
60	-2.14	0.01	8.39	0.03	-29.12	0.01	5.95	0.02
80	-2.12	0.01	8.36	0.03	-29.43	0.02	6.71	0.01
60	-2.03	0.01	8.92	0.03	-27.96	0.03	6.44	0.01
40	-2.20	0.03	9.14	0.03	-27.19	0.03	5.65	0.03
20	-2.24	0.01	9.20	0.02	-26.48	0.01	5.29	0.01

3.4 Conclusions

A measurement methodology to characterize the variation of the resistance ratio of a pair of resistors (also applicable for the variation of single resistance values) was demonstrated with the capability to achieve relative uncertainties (type A) of the order of some parts in 10^8 and 10^9.

The resistor networks tested show a higher sensitivity to temperature variation than humidity, with the exception for Resistor_3. For the temperature variation tested (15 °C to 45 °C) the variation of the ratio was between $1.8 \cdot 10^{-6}$ and $4.6 \cdot 10^{-6}$. For humidity interval variation (20 % to 80 %) was $0.2 \cdot 10^{-6}$ and $2.9 \cdot 10^{-6}$.

The rate of the ratio variation depends on the type of the resistor. Resistor_1 and Resistor_2 (hermetically encapsulated type) were demonstrated to be more insensitive to the humidity than the plastic SMD type Resistor_3 and Resistor_4.

4. CHARACTERIZATION OF CAPACITORS

4.1 Introduction

Metrologically sound methods were developed to measure the following characteristics of capacitors:

- temperature coefficient of capacitance,
- temperature coefficient of loss component,
- sensitivity of capacitance to changes in relative humidity,
- sensitivity of loss component to changes in relative humidity,
- dielectric absorption of capacitors.

During the development of the measurement set-ups, capacitors with various values and dielectrics were used as test pieces. In the case of the dissipation factor measurement set-up larger value capacitors (> 100 nF) were used initially to minimize the effect of offset and leakage currents.

Once the measuring set-ups were operating satisfactorily, they were used to measure high quality surface mount capacitors intended for use as critical elements in the digitizer. Capacitors from two different manufacturers were tested:

- TDK 470 pF, 650 V, 5%, C0G/NP0 1206, Part No. C3216C0G2J471J085AA,
- MURATA 470 pF, 650 V, 5%, C0G/NP0,1206, Part No. GRM31A5C2J471JW01D.

In the following sections, these will be referred to as TDK and MURATA respectively.

This report describes the measurement set-ups and their development. The results of measuring the characteristics of the TDK and MURATA capacitors are presented.

4.2 Measurement of temperature coefficient of capacitance and D factor

4.2.1 Overview of method

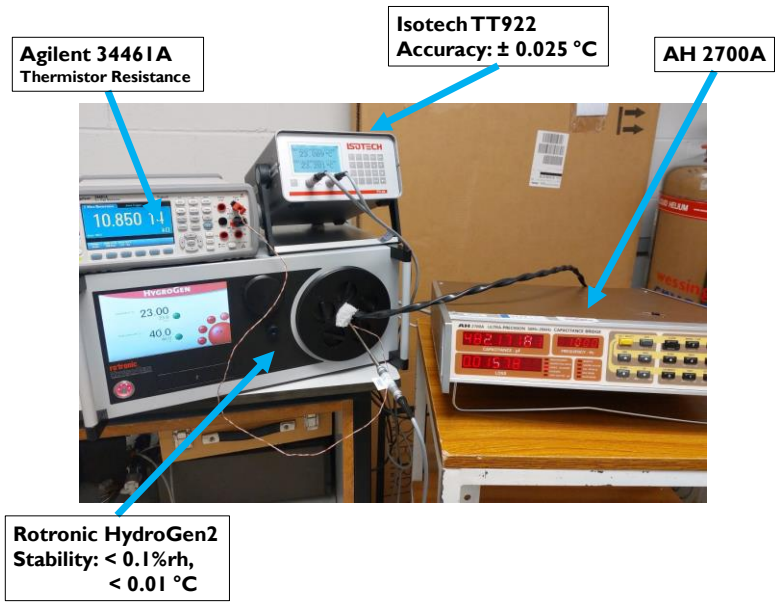


Figure 4-1: Set-up for characterizing temperature sensitivity of capacitors

The capacitor under test is placed in a fixture which allows a three-terminal measurement of its capacitance. The fixture is placed in a temperature-controlled enclosure whose temperature can be varied. The capacitance at each temperature setting is measured using an accurate, high resolution, digital bridge. The measurements were made over the range 18 to 43 °C. Figure 4-1 shows a photograph of the test set-up with the main components labelled.

4.2.1.1 Technical Details

Capacitance Measurement

An Andeen Hagerling AH2700A Capacitance Meter was used to measure the capacitance and loss component of the test capacitor. This instrument measures capacitance over the frequency range 50 Hz to 20 kHz with a display resolution and stability below 1 µF/F. It also measures the loss which can be displayed as dissipation factor (D), conductance (parallel representation), or equivalent series resistance (series representation).

Temperature Control

A Rotronic HYDROGEN HG2-S is used to vary the temperature of the test capacitor in a controlled fashion. This is an instrument for generating stable conditions of temperature and humidity in a small chamber with a working volume of 1.5 litres. Its main intended use is the calibration of temperature and humidity sensors.

The temperature can be set in the range 0 to 60 °C. Once it has stabilised the stability of the temperature is of the order of ±0.01 °C with temperature gradient of less than ±0.05 °C (in range 5 – 50 °C). The typical time to set point is 5 minutes.

The thermoregulated chamber can be programmed to generate a timed sequence of temperatures.

Temperature Measurement

The air temperature in the chamber can be monitored with a digital thermometer using an Pt-100 probe (IsoTech TTI-22). The expanded uncertainty of the measured temperature is ±0.025 °C. In addition, a thermistor is mounted in the test fixture, adjacent to the test capacitor and terminals are provided for connection to an external ohmmeter (Agilent 34461A).

Test Fixture

The purpose of the test fixture is to allow test capacitors of various shapes and sizes to be connected to the capacitance bridge. A 3-terminal configuration is required to minimize the effect of stray capacitance. The bridge input terminals are two BNC connectors. A photograph of one of the test fixtures with the top cover removed is shown in Figure 4-2. This fixture is intended to accommodate SMD components. Spring loaded pogo pins are used to hold the component in place. The picture shows the fixture with a component of size 1608 (metric) installed. Similar text fixtures to accommodate other component shapes were constructed as required.

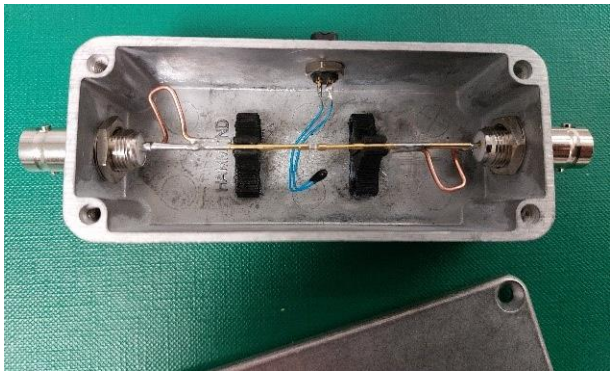


Figure 4-2: SMD Test Fixture

4.2.2 Measurement of temperature response of capacitance value

4.2.2.1 Preliminary results

A typical data set for measurements over the range 23 to 43 °C, taken during the initial testing of the measurement set-up, is shown in Figure 4-3. The test capacitor was a TDK CGA3E3NP02E102J080AA 1 nF C0G\NP0 multilayer ceramic capacitor (size 1608 metric). The temperature was varied from 23 to 43°C in steps of 5°C. The stabilisation time at each set temperature was 1 hour. The test frequency was 1 kHz.

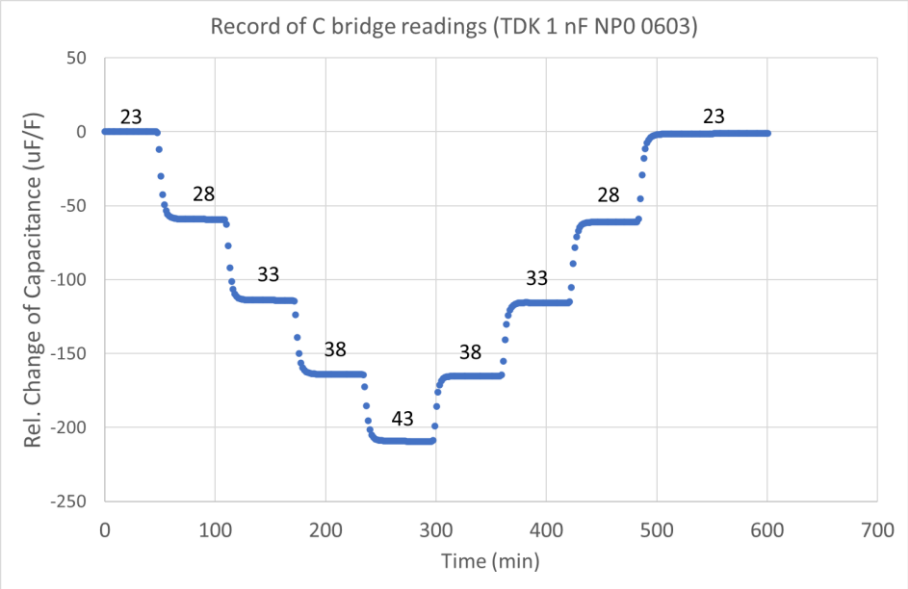


Figure 4-3: Uniformity measurement setup (not shown x-axis)

A small amount of hysteresis was observed. It's possible that pre-conditioning the test capacitor may remove this effect, but this was not investigated. A much larger hysteresis effect was observed for 1 nF capacitor with a Teflon dielectric as shown in Figure 4-4.

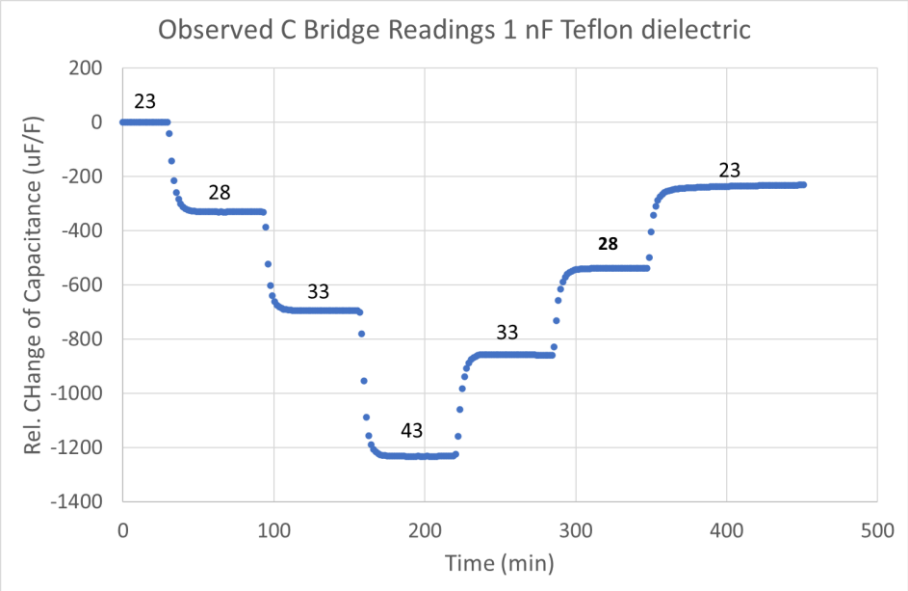


Figure 4-4: Observed capacitance variation of Teflon 1nF over 23 to 43 °C

Figure 4-5 shows the measured capacitance of the C0G/NP0 1 nF capacitor as a function of temperature based on the data shown in Figure 4-3. A linear fit line is shown, although the distribution of the data points about the line suggests that the capacitance does not vary linearly with temperature. Nonetheless a linear fit is sufficient to provide a usable temperature coefficient.

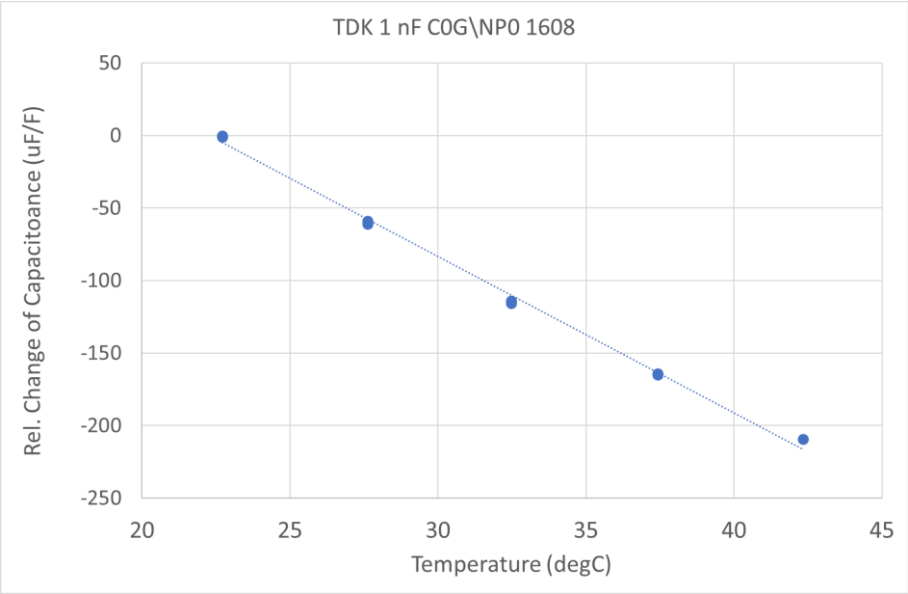


Figure 4-5: Mean measured capacitance vs temperature for G0G/NP0 1nF

Table 4-1 shows the temperature coefficients of a number of types of capacitors that were tested as part of the validation of the test set-up. Since the uncertainties of the capacitance and temperature measurements are small the standard uncertainty of the measured temperature coefficient is dominated by the uncertainty in the slope of the least squares fitted line. The scatter of data about the line and hence the uncertainty of the fit is increased by hysteresis effects and the possible non-linear relationship between capacitance and temperature.

Table 4-1: Measured temperature co-efficient of several capacitors

Nominal Value	Manufact.	Part No.	Dielectric	Measured Temperature Coefficient	Standard Uncertainty
				(µF/F per °C)	(µF/F per °C)
1 nF (#1)	Not known	Not known	Mica	+37.1	0.2
1 nF (#2)	Not known	Not known	Mica	+34.8	0.3
1 nF	Not known	Not known	Teflon	-60	7
1 nF (#1)	TDK	CGA3E3NP02E102J080AA	Ceramic	-11.0	0.4
1 nF (#2)	TDK	CGA3E3NP02E102J080AA	Ceramic	-10.8	0.2
1 nF	Vishay	VISHAY MKP1839210631	Polypropylene	-220	2

4.2.2.2 Temperature Coefficient of Selected Capacitors

A 470 pF SMD capacitor manufactured by TDK (Part Number Part No. C3216C0G2J471J085AA) is a candidate for use in the novel integrating ADC. The temperature sensitivities of ten of these components taken from the same batch were measured. The response to changes in temperature of one capacitor is shown in the graph in Figure 4-6. The response to changes in temperature is substantially linear although a better fit can be obtained by using a quadratic model.

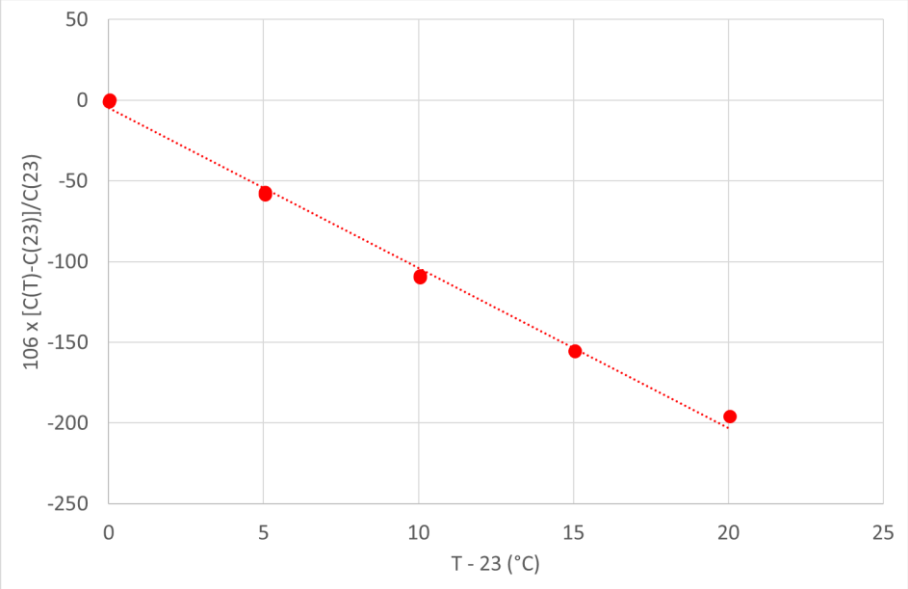


Figure 4-6: Typical temperature response of TDK capacitor

The measured temperature coefficients of the capacitors were remarkably consistent as shown in Table 4-2. All capacitors showed the same slight deviation from linear dependence of temperature as well as a slight hysteretic effect. The associated standard uncertainty of 0.25 ppm/K is dominated by the (systematic) deviation of the data about the LS fitted line. The repeatability of the measurement is less than 0.05 ppm/K.

Table 4-2: Measured Temperature Coefficients of TDK 470 pF NP0 capacitors

Capacitor Number	Temperature Coefficient
	(ppm per K)
TDK #1	-10.17
TDK #2	-10.29
TDK #3	-10.25
TDK #4	-9.93
TDK #5	-10.28
TDK #6	-10.14
TDK #7	-9.91
TDK #8	10.11
TDK #9	-10.17
TDK #10	-10.17

A sample of three capacitors from a second batch with the same part number were also measured. The results, which are shown in Table 4-3, show a temperature coefficient which is marginally higher than the first batch.

Table 4-3: Measured Temperature Coefficients of TDK 470 pF NP0 capacitors (Batch 2)

Capacitor Number	Temperature Coefficient of Capacitance
	(ppm per K)
TDK #1A	-10.55
TDK #2A	-10.63
TDK #3A	-10.33

A capacitor of similar design and construction from a different manufacturer (MURATA 470 pF, 650 V, 5%, C0G/NP0,1206, Part No. GRM31A5C2J471JW01D) was also tested. The temperature sensitivities of five samples from the same batch were tested and the results are shown in Figure 4-7.

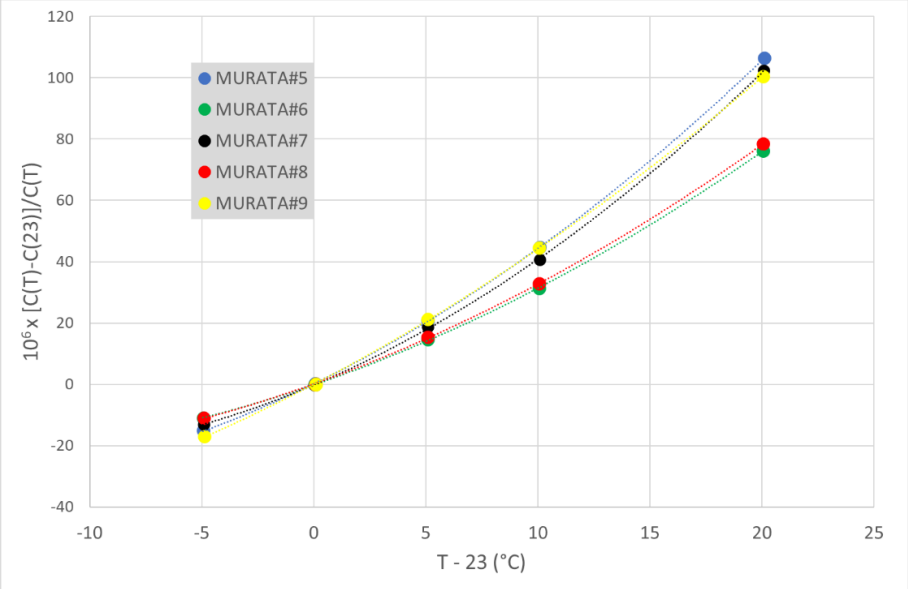


Figure 4-7: Temperature response of MURATA capacitors

For these capacitors the non-linearity of the response was more pronounced, and the responses were not as consistent as for the TDK capacitors. The parameters of a LS quadratic fit to the data for a reference temperature of 23 °C are given in Table 4-4 and are calculated as shown in Eq. 4-1.

Table 4-4: Temperature coefficients of MURATA capacitors

Capacitor	α x 10^6	β x 10^6
MURATA #5	3.56	0.086
MURATA #6	2.50	0.065
MURATA #7	3.10	0.100
MURATA #8	2.61	0.064
MURATA #9	3.82	0.059

Eq. 4-1: $$C(T) = C(23) \cdot (1 + \alpha \cdot (T - 23) + \beta \cdot (t - 23)^2)$$

The typical temperature sensitivities of the two types of capacitors are compared in Figure 4-8.

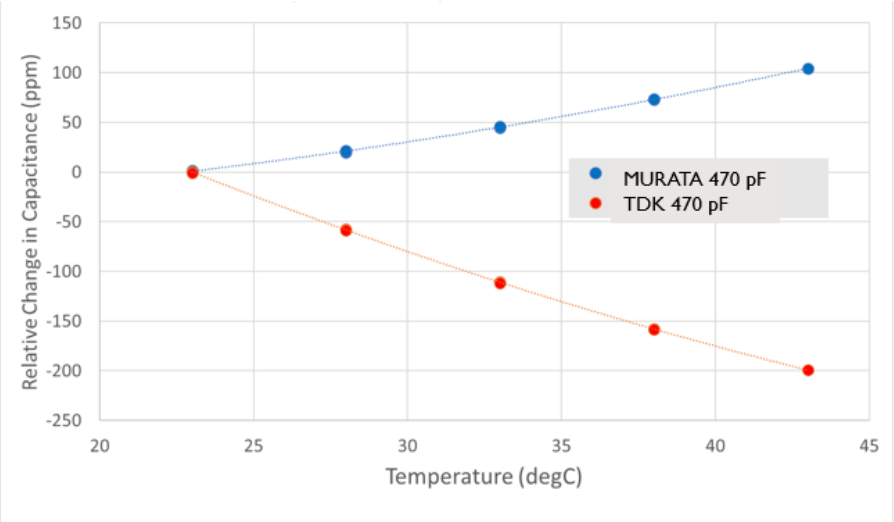


Figure 4-8: Comparison of temperature sensitivities of TDK and MURATA capacitors

4.2.3 Measurement of the temperature response of loss component of capacitors

The loss components of the capacitors were recorded during all of the temperature tests. The AH2700A bridge can display several versions of the loss component, namely conductance (nS), dissipation factor (dimensionless), equivalent series resistance (kΩ), equivalent parallel resistance (GΩ) and loss factor (pF). Dissipation factor is used throughout the following results. The other representations of the loss component may be evaluated from the dissipation factor and the capacitance.

The measured values of the loss components exhibited considerable temporal drift, as shown in Figure 4-9 which shows the measured dissipation factor as a function of time while the temperature is varied in steps of 5°C over the range 23 to 43°C.

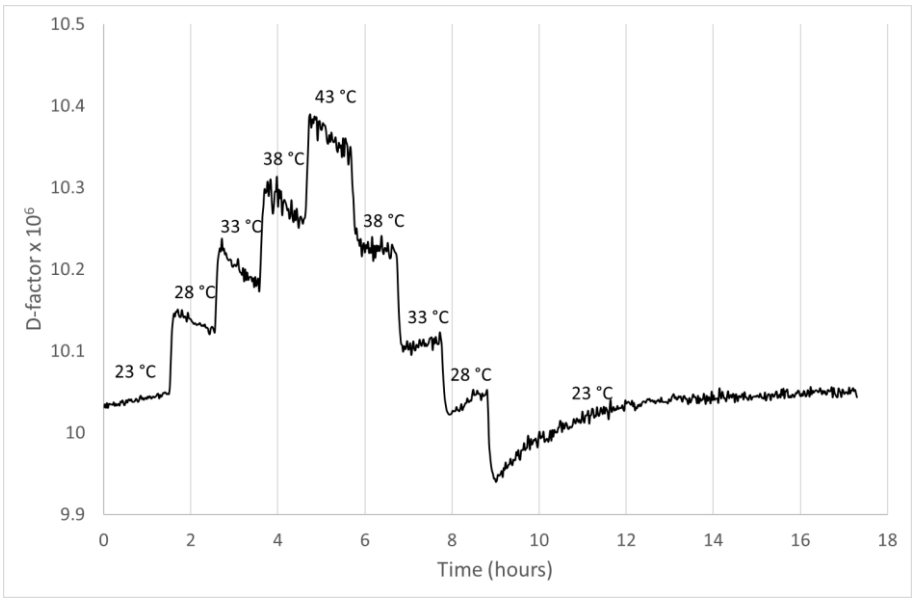


Figure 4-9: Measured Dissipation factor of TDK #10 during temperature cycle

This behaviour was further examined by performing three consecutive temperature cycles over a four-day period. The results are shown in Figure 4-10.

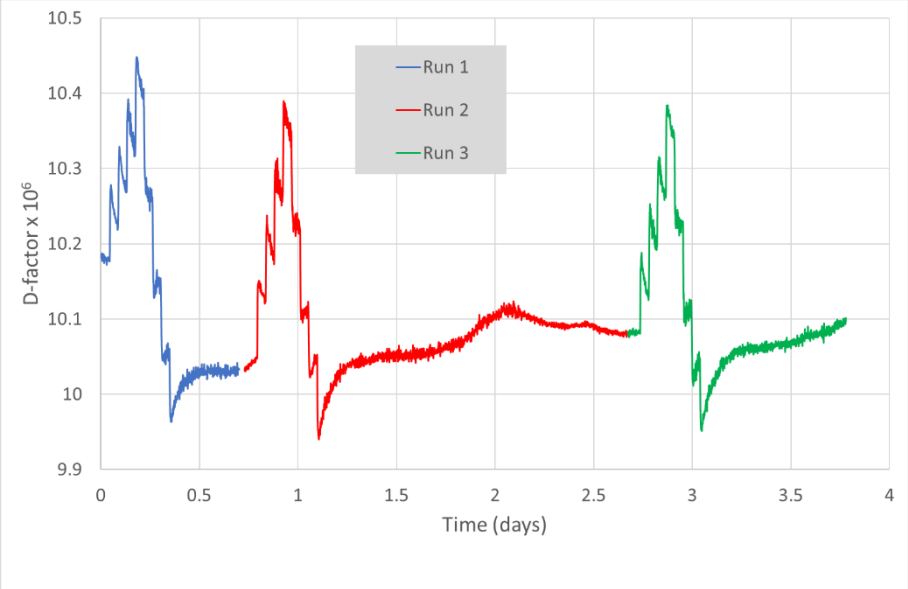


Figure 4-10: Measured dissipation factor for three consecutive temperature cycles

The drift appears to be instigated by the temperature changes, but its origin is unknown and needs further investigation. It was found that the effect was far smaller for the TDK capacitors from the second lot, as can be seen in Figure 4-11.

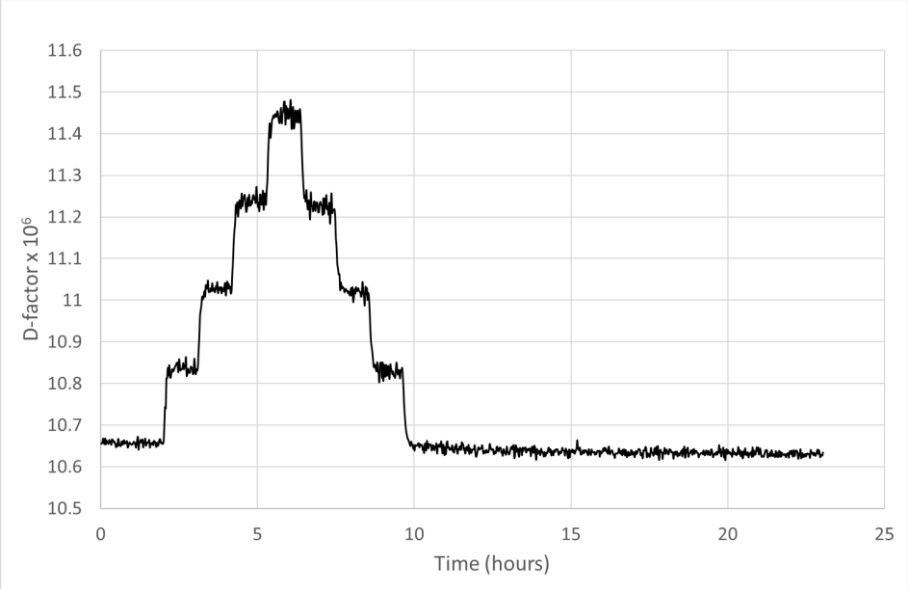


Figure 4-11: Measured Dissipation factor of TDK #1A during temperature cycle

The effect of the drift behaviour is to cause the plots of dissipation factor versus temperature to show considerable hysteresis. This can be seen in Figure 4-12 which shows the measured temperature response of the dissipation factor for one capacitor taken from each of the two batches.

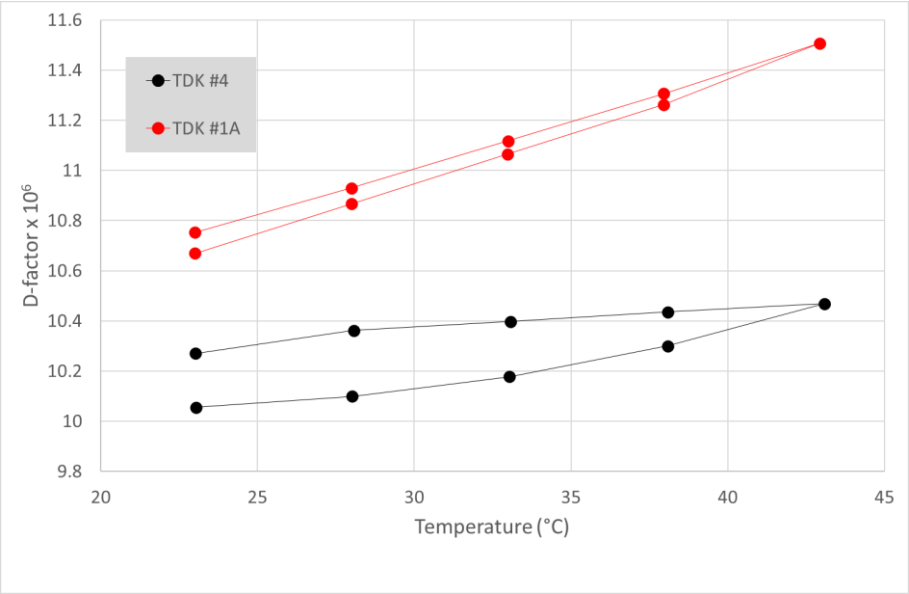


Figure 4-12: Measured response of the dissipation factor to temperature cycling for capacitor TDK#4 and TDK#1A

If the drift is assumed to be linear, the temperature coefficient of the dissipation factor can be determined by plotting the average measured value at each temperature versus temperature.

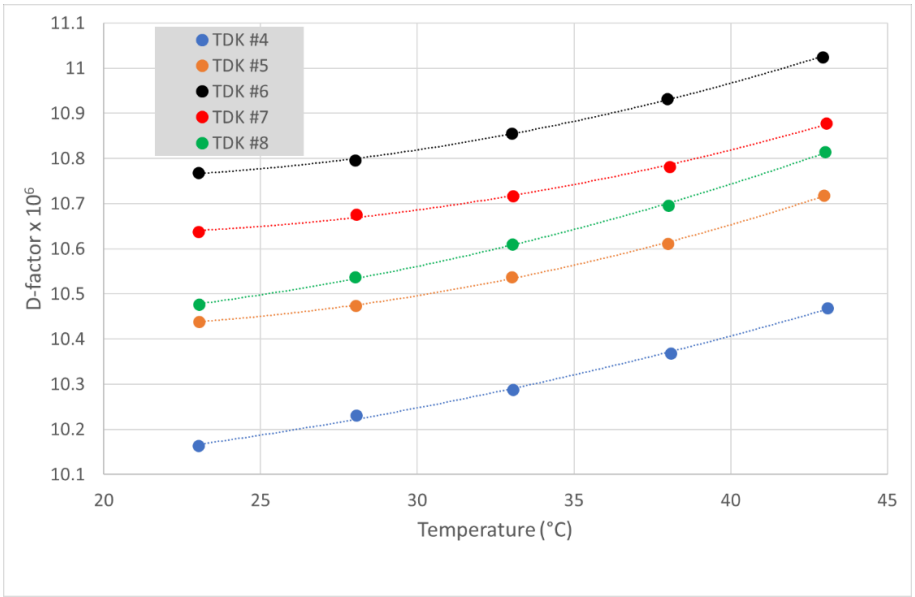


Figure 4-13: Observed temperature response of dissipation factor for capacitors TDK #4 – 8

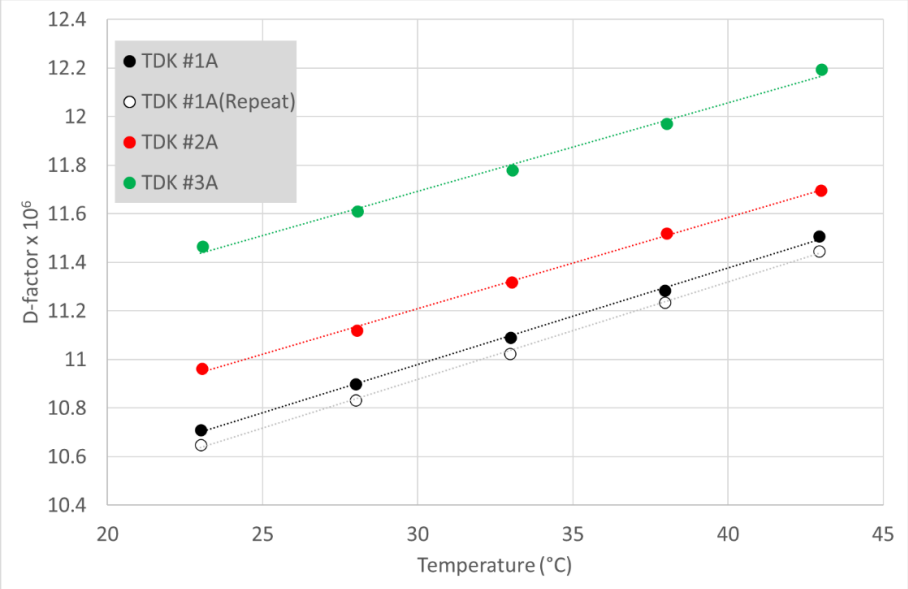


Figure 4-14: Observed temperature response of dissipation factor for capacitors TDK #1A – 3A

The temperature response of the dissipation factor of the MURATA capacitors is shown in Figure 4-15.

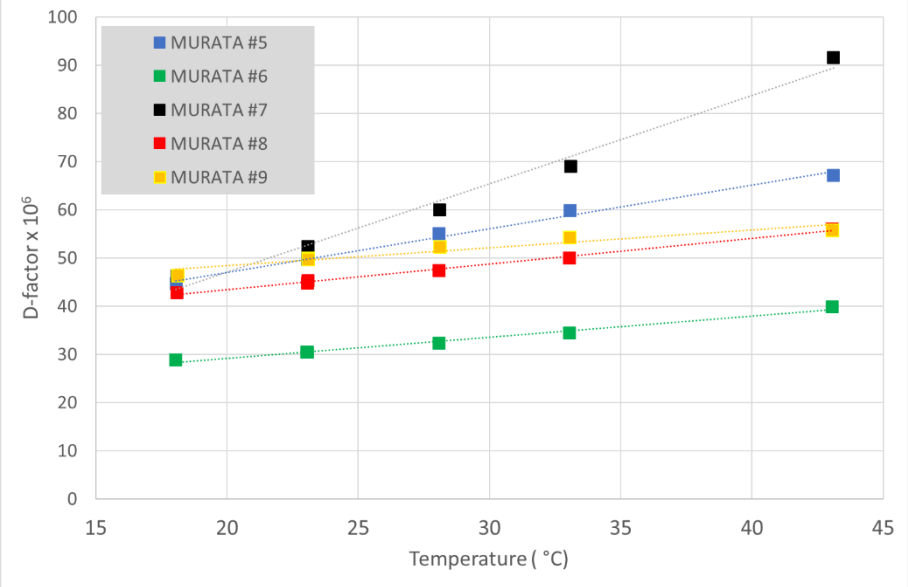


Figure 4-15: Observed temperature response of dissipation factor for capacitors MURATA #5-9

The results of the temperature sensitivity measurements of the dissipation factor of the 470 pF SMD ceramic NP0 capacitors are summarised in Table 4-5.

Table 4-5: Measured values of dissipation factors and their temperature coefficients

Capacitor	Range of D-factor @ 23°C ($x10^6$)	Range of Temperature Co-efficient ($x\ 10^6\ °C^{-1}$)
TDK (batch 1)	10.2 – 10.8	0.036 – 0.040
TDK (batch 2)	10.7 – 11.5	0.011 – 0.017

4.3 Measurement of the effect of humidity changes on capacitors

Using the same set-up as used for the temperature measurements, the effect of changes in humidity on the capacitance and loss component of the TDK and MURATA capacitors was measured. As usual with humidity effects the measurements are complicated by long time constants and different behaviours for the absorption and desorption of water vapour.

4.3.1 Sensitivity of the component's capacitance to humidity changes

The observed change in the capacitance of capacitor TDK #1 (batch 1) is shown in Figure 4-16. The humidity was varied in steps of 20%rh over the range 20%rh to 80%rh with a stabilization time of 12 hours at each humidity level apart from the 80%rh level which has a longer stabilization time of 18 hours. Only the steady state humidity level was recorded.

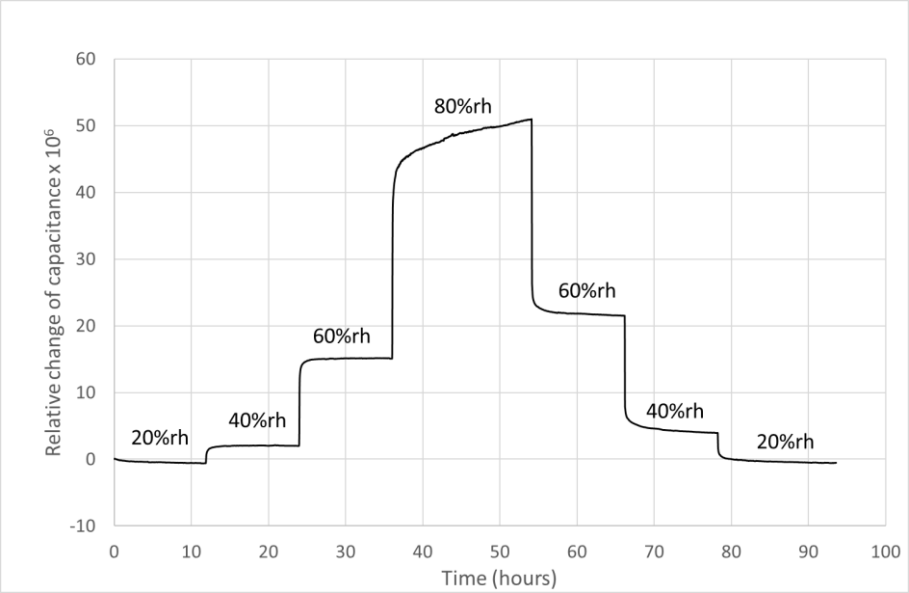


Figure 4-16: Measured capacitance of TDK #1 for humidity cycle

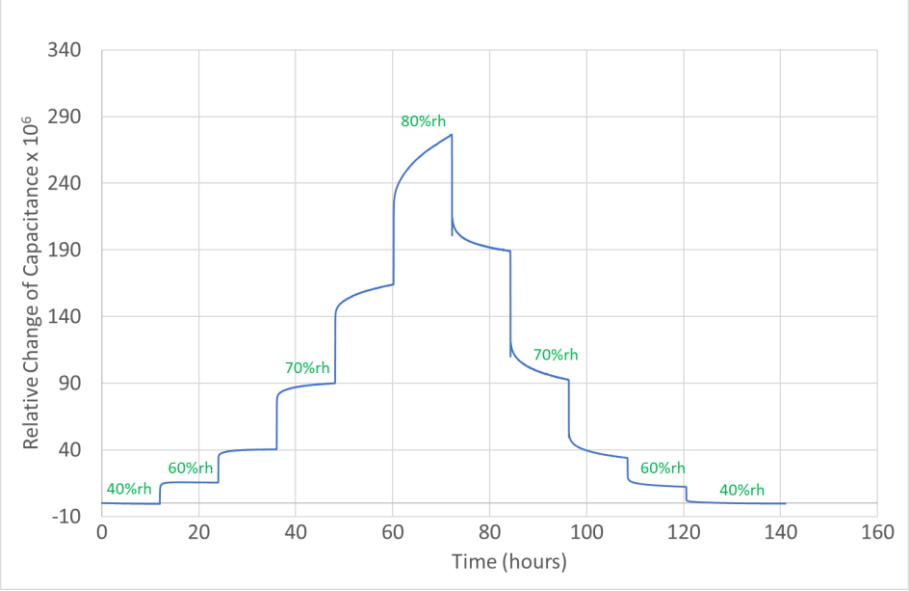


Figure 4-17: Measured capacitance of MURATA #5 for humidity cycle

A similar plot is shown in Figure 4-17 for a MURATA capacitor with a different humidity cycle of 40%-60%-65%-70%-75%-80% with a stabilization time of 12 hours for each humidity setting.

Both responses show similar behaviour although the MURATA component shows a significantly higher sensitivity. The capacitance initially responds rapidly to the change in humidity and thereafter appears to slowly approaches a constant value. The overall response is non-linear with the sensitivity increasing dramatically as the humidity increases. Another feature is the large hysteresis, possibly caused by the desorption mechanism having a very long time constant.

The mean measured capacitance at each step is plotted against temperature in Figure 4-18 and Figure 4-19 for the same data.

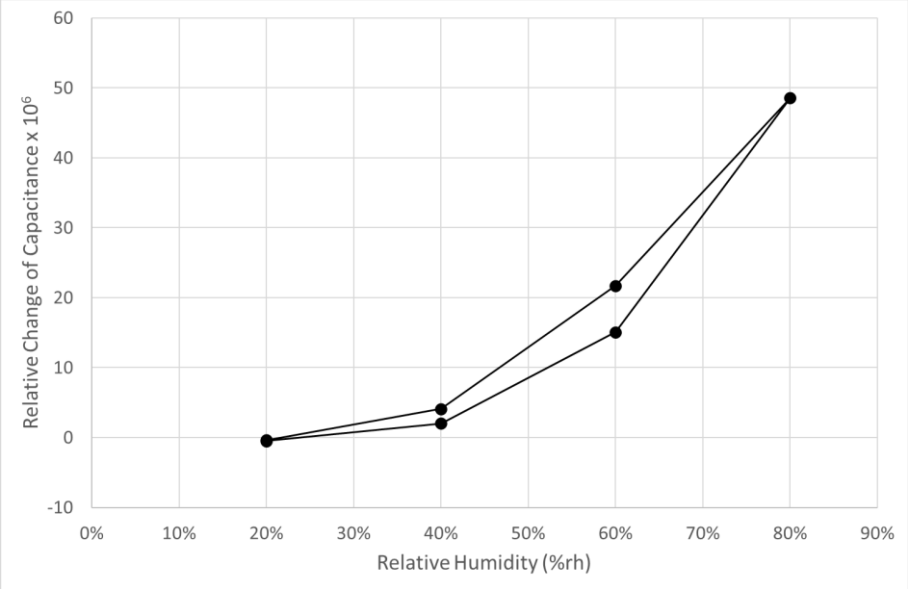


Figure 4-18: Measured humidity response of TDK #1

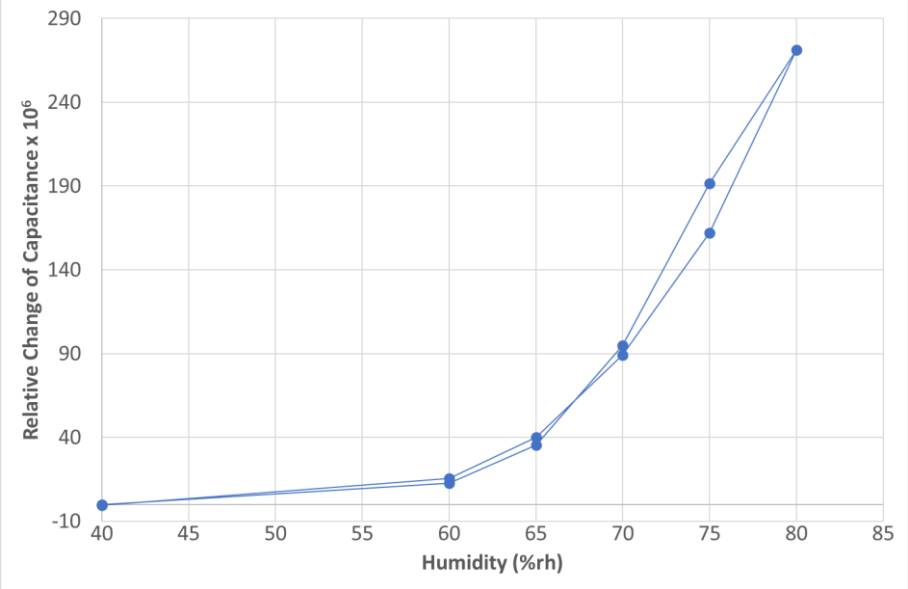


Figure 4-19: Measured humidity response of MURATA #5

An abbreviated humidity test was performed on five samples of TDK (batch 2) and MURATA capacitors whereby the humidity was held constant at 40%rh for 8 hours, raised to 80%rh for 8 hours and then returned to 40%rh for 8 hours. The results are shown in Figure 4-20 and Figure 4-21 for the TDK and MURATA components respectively.

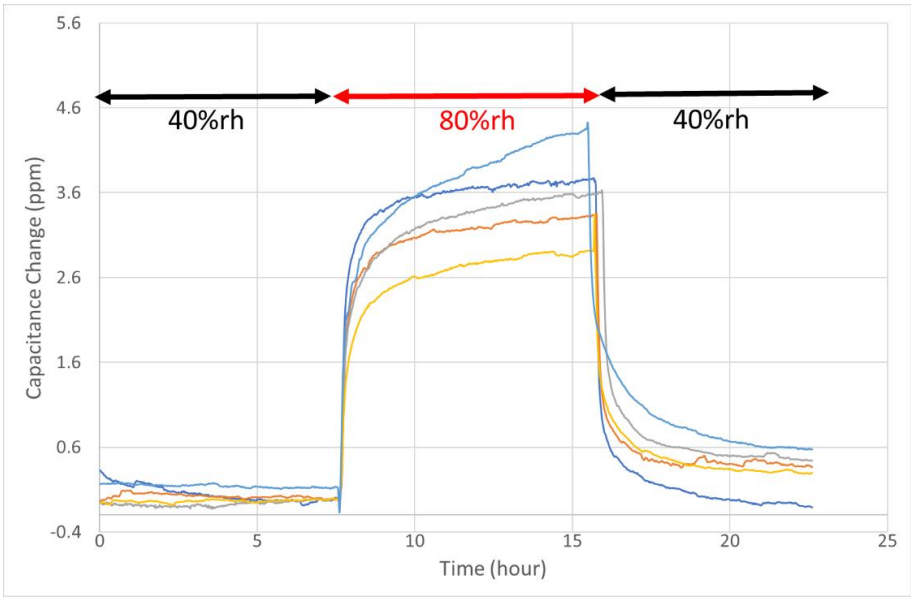


Figure 4-20: Response of 5 x TDK (batch 2) capacitors to humidity change of 40%rh

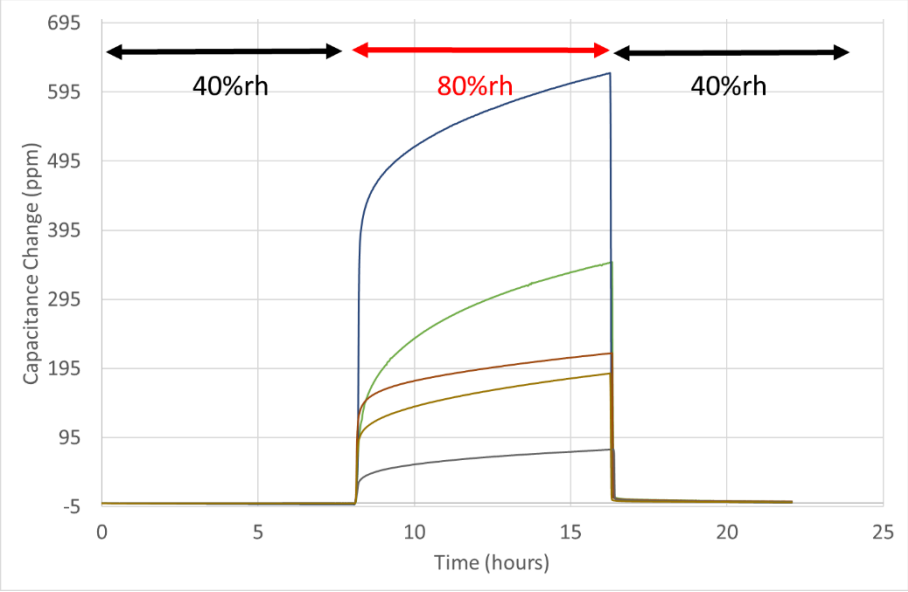


Figure 4-21: Response of 5 x MURATA capacitors to humidity change of 40%rh

The humidity sensitivity of the TDK capacitors from batch 2 was found to be significantly lower than that of capacitors from batch 1. The humidity response was consistent among all five capacitors. This contrasts with the results for the MURATA components which showed a much greater and a much more variable response to the humidity step. This may be due to different protective coatings on the capacitors.

4.3.2 Sensitivity of the component's loss component to humidity changes

The effect of humidity changes on the loss component of the capacitors was found to be quite dramatic. The changes in the dissipation factor of the TDK#1 and the MURATA capacitors due to a changes in the relative humidity are shown in Figure 4-22 and Figure 4-23 respectively. Data for both increasing and decreasing humidity are shown, and the hysteresis effect, probably due to inadequate stabilization times can be seen.

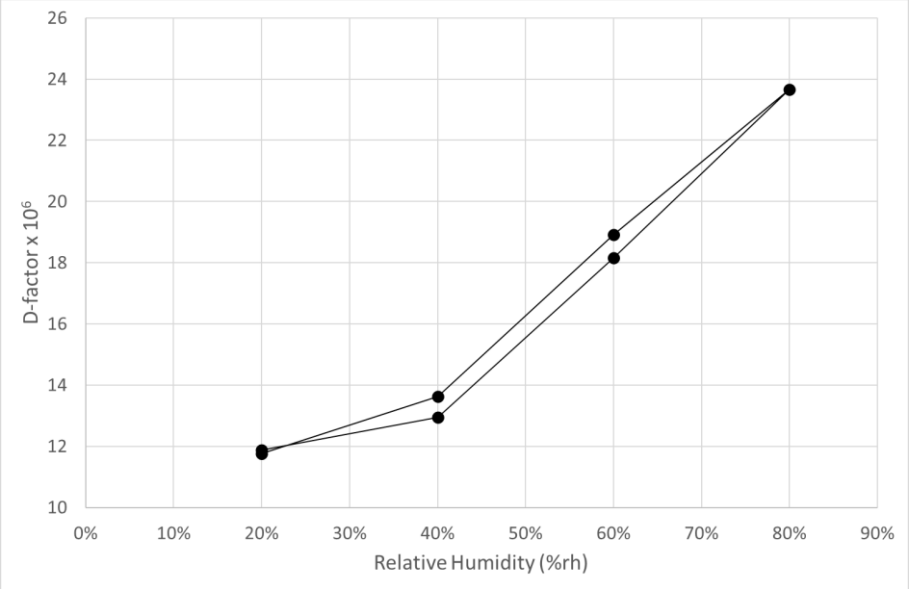


Figure 4-22: Effect of humidity changes on dissipation factor of TDK#1

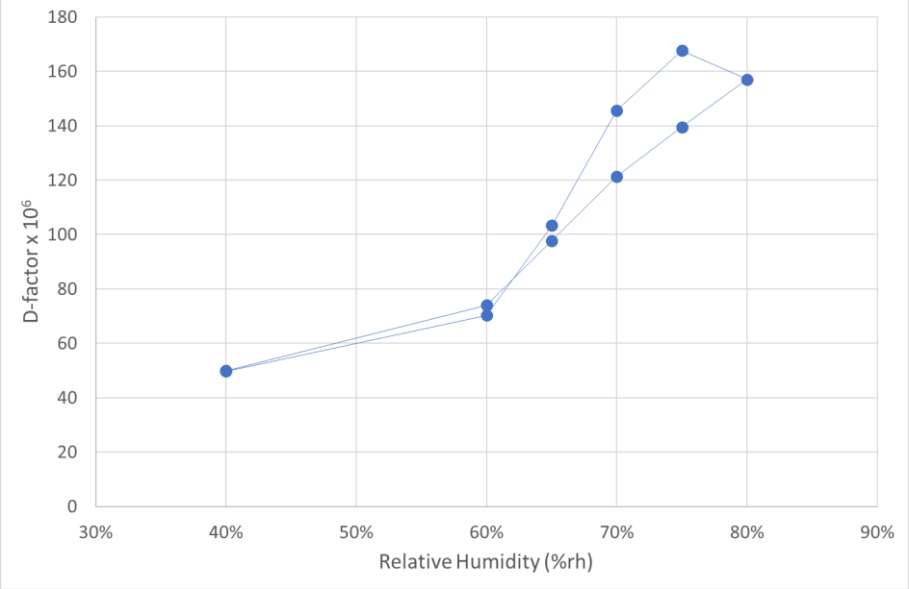


Figure 4-23: Effect of humidity changes on dissipation factor of MURATA #5

The dissipation factor changes by more than a factor of 2 for the TDK component and by a factor of nearly 4 for the MURATA component when the relative humidity is increased from 40%rh to 80%rh. Other capacitors of these types showed similar behaviour.

4.4 Measurement of the dielectric absorption of a capacitor

4.4.1 Overview of Method

The so-called “classical” method of measuring the dielectric absorption of a capacitor as per IEC 60384-1 was used. This is most suitable for charge/discharge times of more than a second.

A schematic of the test set-up is shown in Figure 4-24.

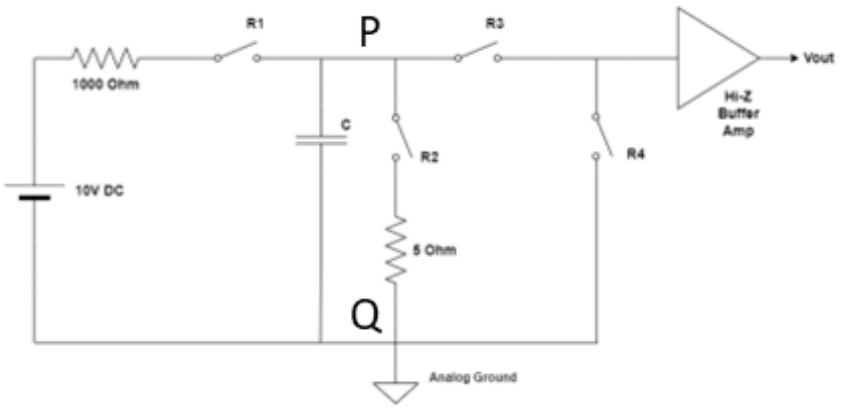


Figure 4-24: Schematic of test set-up for measurement of dielectric absorption

An important requirement of the set-up is to minimize the effects of leakage across the test capacitor and of bias current generated by the buffer amplifier. Low leakage, glass encapsulated relays mounted on a PTFE base were used. The resistance between points P and Q of the measuring circuit when all relays are set to open was measured to be 5 x 1013 Ω at a test voltage of 100 V.

A high impedance, low bias current buffer amplifier using a ADA4530-1 electrometer op amp was constructed. The PCB has the same layout as the evaluation board supplied by Analog Devices but uses IS400 as PCB material rather than the more expensive Rodgers 4350B. Connection to the test fixture is via a triaxial connection. The op-amp’s guard voltage is used to minimize leakage in the input cable and to drive the relay guards. The amplifier is housed in a shielded case to reduce noise. The bias current of the buffer amplifier was measured and found to be less than 10 fA.

An external DC source is used to charge the capacitor. The output of the buffer amplifier (i.e. the recovery voltage), was measured using a Fluke 8588A multimeter.

The relays were controlled by a Raspberry Pi PICO microcontroller and open-source software (CircuitPython).

The overall control of the measuring system (operation of charging source, operation of relays, reading of voltmeter) was via a Python programme.

The relay board (A), buffer amplifier (B) and the relay control board (C) were mounted in an earthed metal enclosure as shown in Figure 4-25 where the top cover of the enclosure has been removed.

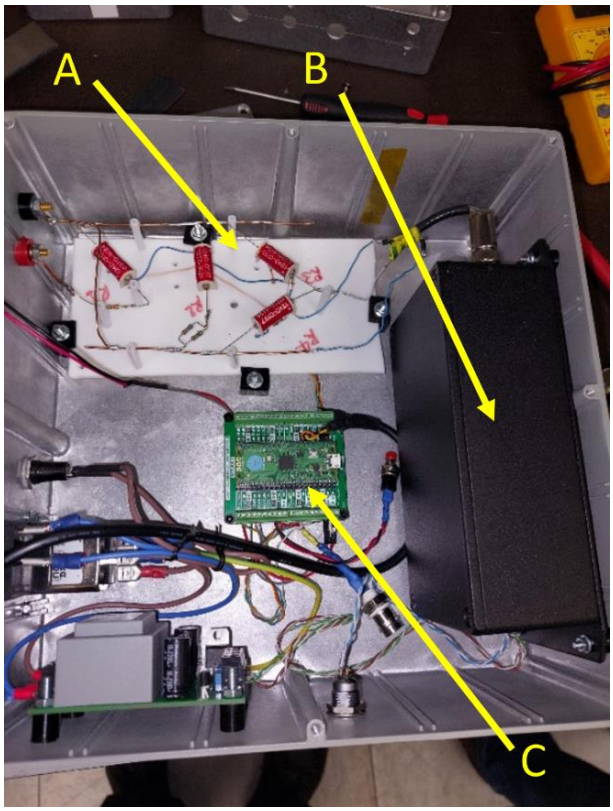


Figure 4-25: DA buffer amplifier, relay board and controller

Table 4-6: Relay Sequence

Switch Settings				Action
R1	**R2**	**R3**	**R4**	
Closed	Open	Open	Open	Capacitor is charged by the stable DCV source through 1 kΩ resistor for time t_1
Open	Closed	Open	Open	Capacitor is discharged through 5 Ω resistor R for time t_2
Open	Open	Closed	Closed	Short circuit applied to buffer amplifier
Open	Open	Closed	Open	Voltage across capacitor is monitored by voltmeter for time t_3

The relay sequence used is shown in Table 4-6. This particular sequence was chosen so that the measurement of the recovery voltage is initiated by the opening rather than the closing of a relay. Closure of a relay was found to cause an injection of charge into the capacitor which disrupted the measurement of the recovery voltage. However, this method has the disadvantage that the capacitor is shorted when R_3 and R_4 are closed so that the discharging time cannot be reduced below the time taken to close and open R_4. In the results given below the discharge times given refer only to the closure time of R_2 and do not include this additional charging time.

4.4.1.1 Results

Initially the measurements were aimed at verifying that the measurement set-up works as expected. Measurements have therefore been confined to capacitors with large capacitances (≥ 33 nF).

Figure 4-26 shows graphs of the recovery voltages of a 33 nF polyethylene capacitor for charging voltages of 5, 10 and 20 V. The charge time was 10 s, the discharge time 5s and each measurement is repeated four times. The variability of the traces is probably due to unreleased charge building up on the capacitor's dielectric. The results confirm that the ratio of the steady state recovery voltage to the charging voltage is constant, as expected.

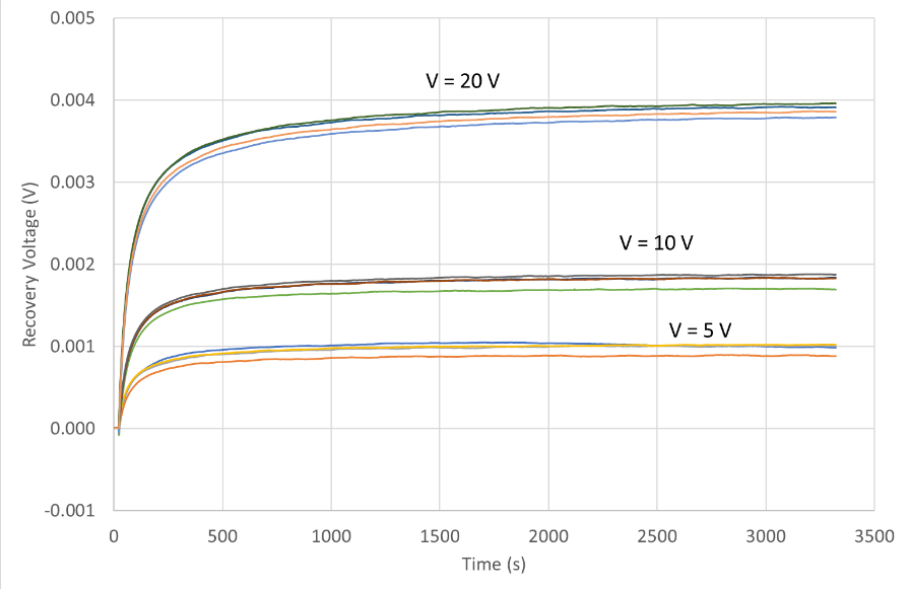


Figure 4-26: Effect of charging voltage on the recovery voltage

Figure 4-27 shows the effect of the charging (soakage) T_S time on the same capacitor. The charging voltage was 10 V and the discharging time was 5 s.

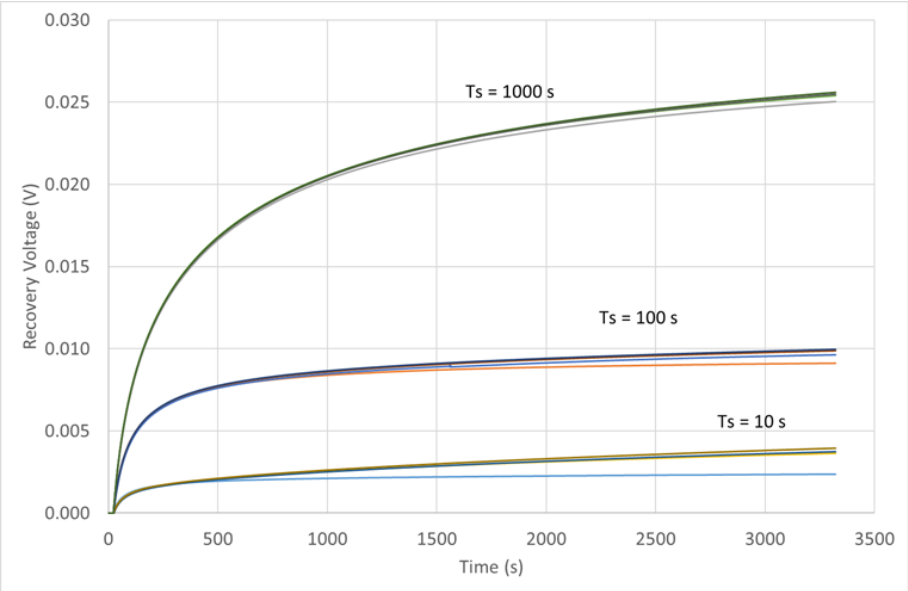


Figure 4-27: Effect of charging time on the recovery voltage

Figure 4-28 shows the effect of the discharge time T_d on the same capacitor. The charging voltage was 10 V and the charging time was 100 s.

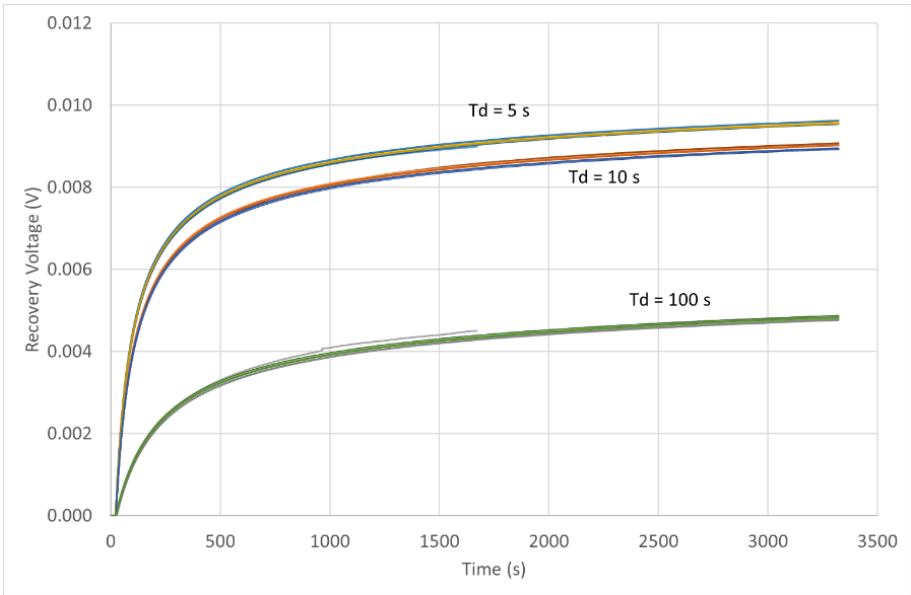


Figure 4-28: Effect of discharging time on the recovery voltage

Figure 4-29 shows the recovery voltages for two 100 nF capacitors with different types of dielectric (charging voltage = 10 V, charging time = 1000 s, discharging time = 5 s)

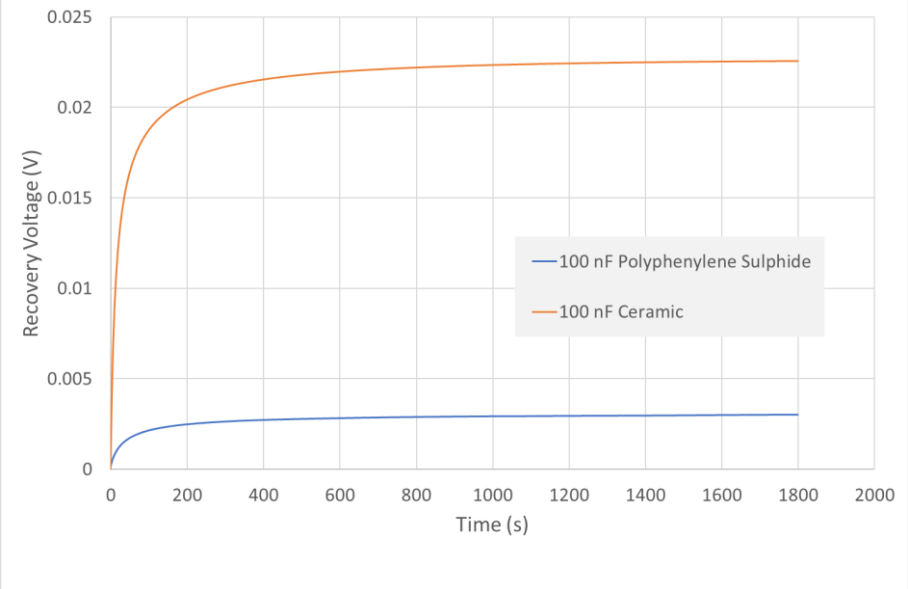


Figure 4-29: Recovery voltages for capacitors with different dielectric materials

Comparison of the measured dielectric factor (V_R/V_C) with those reported in the literature is difficult due to its dependence upon the charging and discharging times.

Figure 4-30 shows a long term (5 hour) record of the recovery voltage of a 100 nF ceramic capacitor with -10 V charging voltage, a 1000 s charging time and a minimum discharging time.

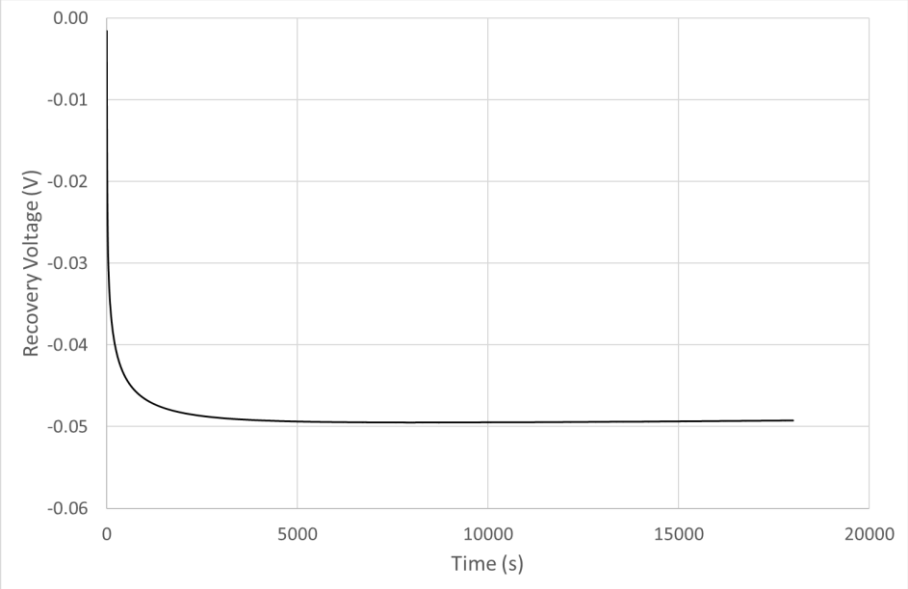


Figure 4-30: Long term record of recovery voltage for 100 nF ceramic capacitor

Figure 4-31 shows the recovery voltage measured over the last 2 hours of the 5-hour observation time. It appears as if the dielectric has fully delivered its charge to the capacitor at this stage and the capacitor is now being charged by the bias current of the amplifier. The slope of the graph is 3 x 10^{-8} V/s which corresponds to a charging current of 3 fA.

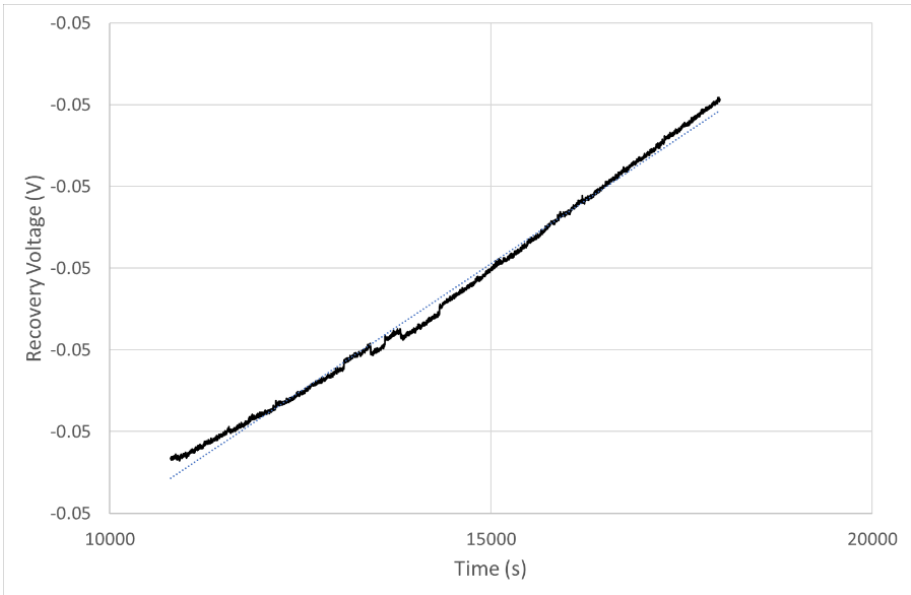


Figure 4-31: Recovery voltage record for 3 to 5 hours after discharge

4.4.2 Measurements of selected components

The dielectric absorption of five TDK capacitors from batch 2 and five MURATA capacitors were measured. The measuring sequence was as follows:

- Capacitor shorted for 1800 s,
- Capacitor charged at 10 V for 900 s,

- Capacitor discharged for 1 s,
- Recovery voltage monitored for 990 s.

The measuring sequence was repeated ten times on the same day to determine the repeatability of the test. The reproducibility of the test was checked for two of the capacitors by repeating the full measurement sequence on three separate days.

Typical results of a measuring sequence for the TDK and MURATA components are shown in Figure 4-32 and Figure 4-33 respectively.

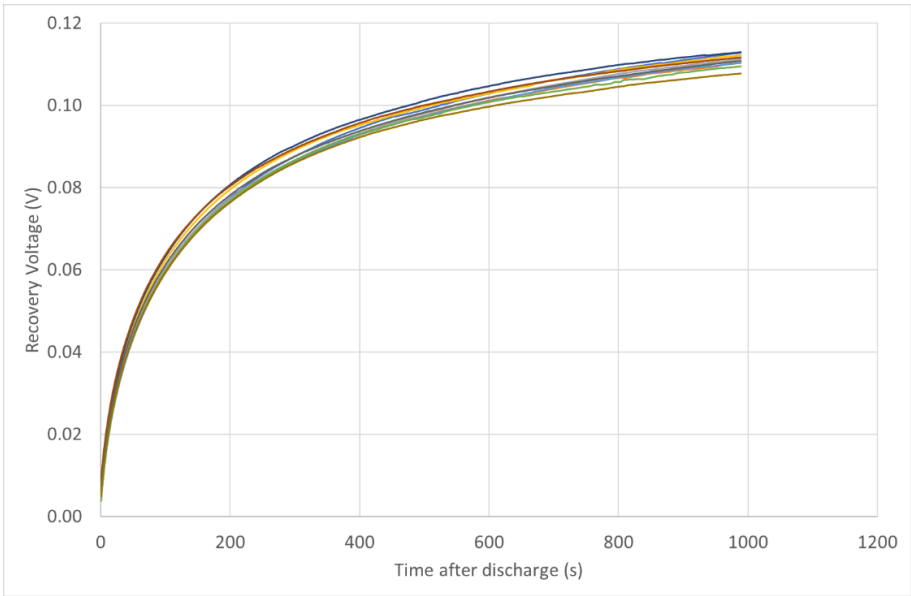


Figure 4-32: Observed recovery voltage for TDK #7A

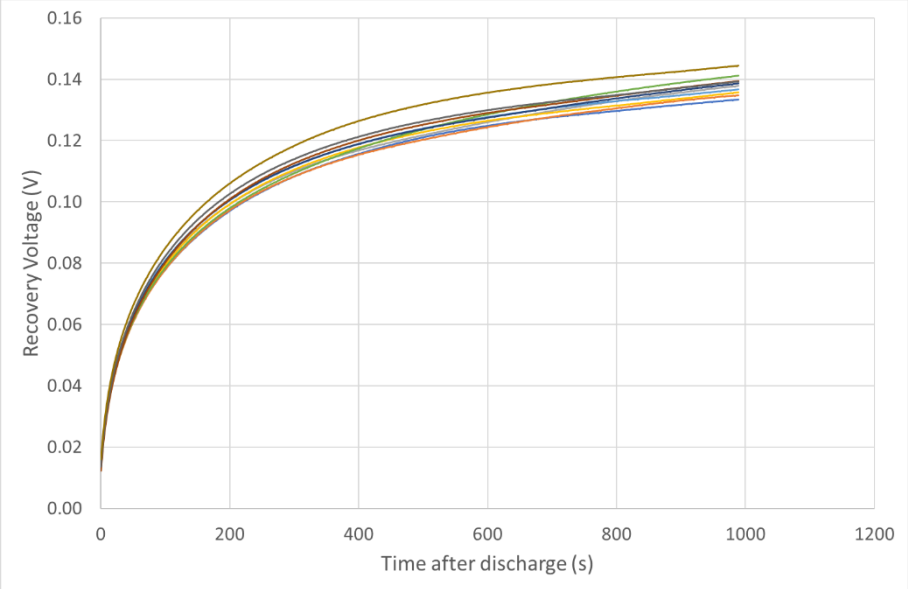


Figure 4-33: Observed recovery voltage for MURATA #13

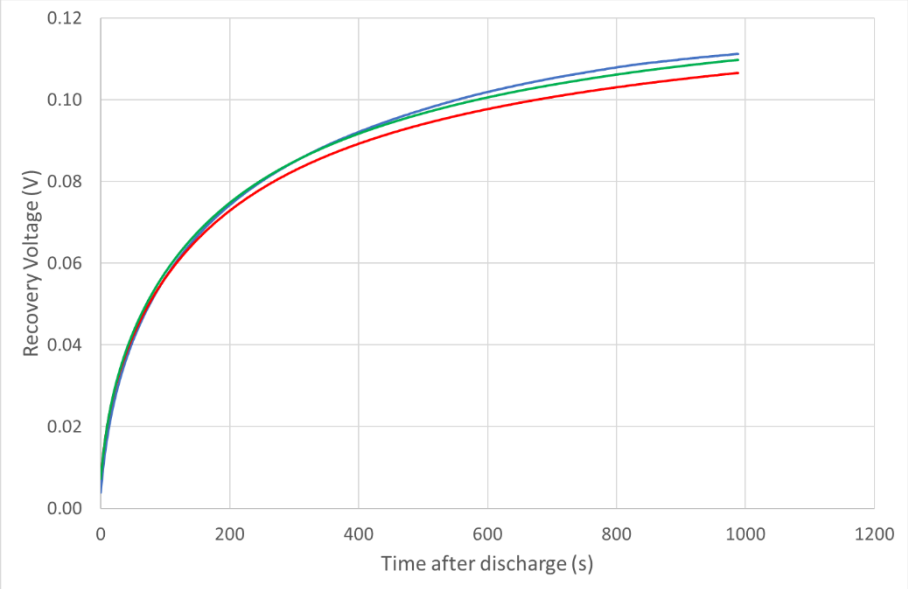


Figure 4-34: Reproducibility of recovery voltage (TDK 10A)

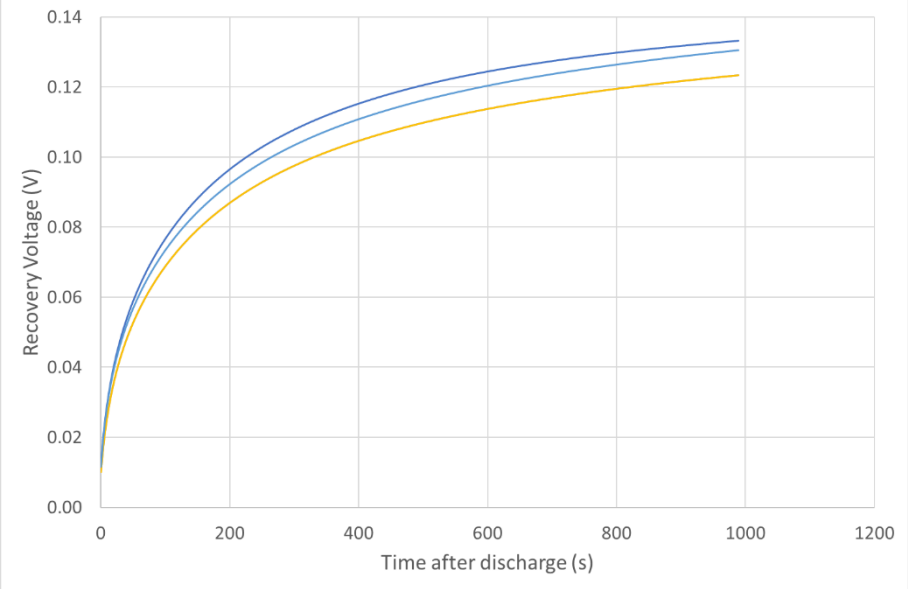


Figure 4-35: Reproducibility of recovery voltage (TDK 10A)

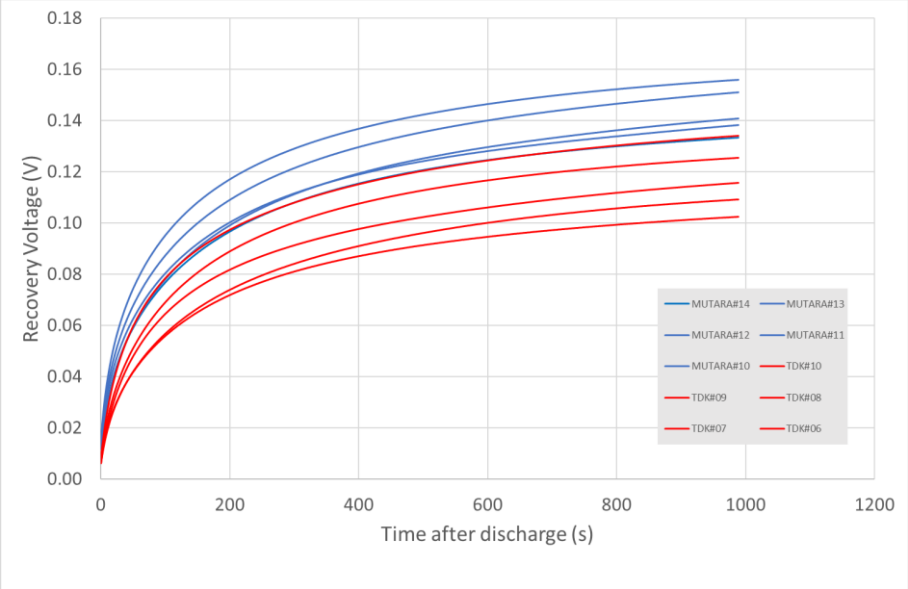


Figure 4-36: Comparison of voltage recovery profiles of TDK and MURATA Capacitors

If we arbitrarily define the dielectric absorption coefficient of the capacitor as the recovery voltage measured 990 s after the capacitor has been discharged divided by the charging voltage the dielectric absorption factors of the TDK and MURATA capacitors are shown in Figure 4-37.

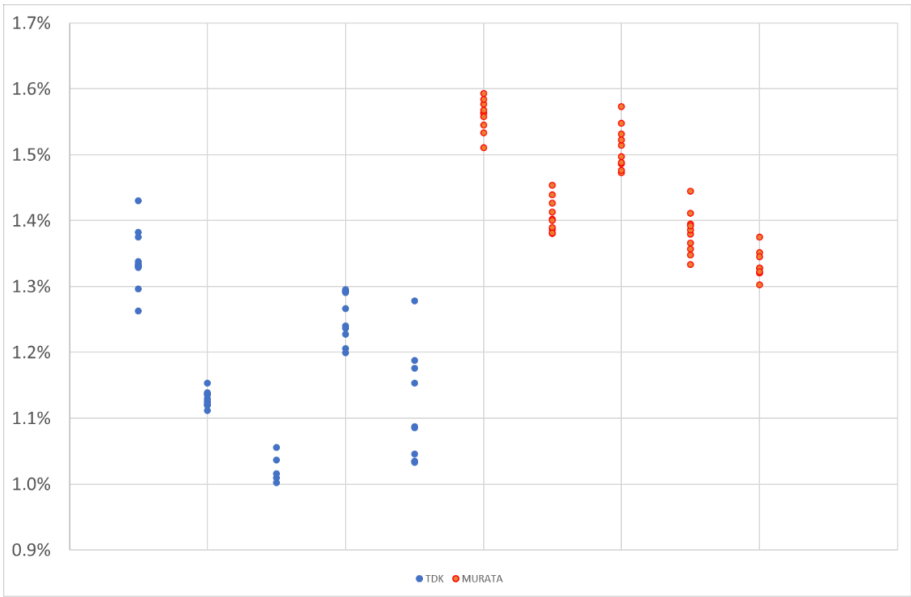


Figure 4-37: Comparison of dielectric absorption factors of TDK and MURATA capacitors

4.4.3 Modelling of dielectric absorption

The effect of dielectric absorption can be modelled by a series of RC circuits in parallel with the capacitor as shown in Figure 4-38.

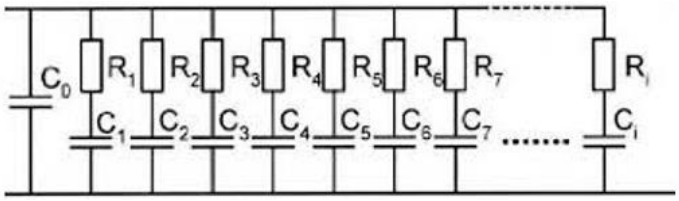


Figure 4-38: Parallel RC model of dielectric absorption

The recovery voltage for a capacitor with capacitance *C* subjected to a charging voltage V_{CH} can be modelled as

Eq. 4-2: $V_{recovery}(t) = \sum_{i=1}^{n} V_i(t) = \sum_{i=1}^{n} a_i \cdot (1 - e^{-b_i \cdot t})$,

where $a_i = V_{CH} \cdot \frac{C_i}{C}$ and $b_i = \frac{1}{R_i \cdot C_i}$ and the time origin is when the shorting relay across the capacitor is opened.

The current delivered by each parallel section during the recovery period is:

Eq. 4-3: $I_i(t) = C_i \cdot \frac{dV_i}{dt} = . C \cdot a_i \cdot b_i e^{-b_i \cdot t}$.

At t =0

Eq. 4-4: $I_i(0) = C \cdot a_i \cdot b_i$.

Assuming that each of the parallel capacitance elements is fully charged we have:

Eq. 4-5: $I_i(0) = \frac{V_{CH}}{R_i}$

we therefore have

Eq. 4-6: $R_i = \frac{V_{CH}}{C \cdot a_i \cdot b_i}$

and

Eq. 4-7: $C_i = \frac{1}{R_i \cdot b_i}$.

Table 4-7 gives the fitted parameters and corresponding *R* and *C* values for the test data for TDK #6A using a model with five parallel RC components.

Table 4-7: Fitted parameters and corresponding RC values for dielectric absorption of TDK #6A

Component	a_i	$\frac{1}{b_i}$	R_i	C_i
	(V)	(s)	(Ω)	(F)
1	0.038 26	147.2	8.25 x 10^{13}	1.78 x 10^{-12}
2	0.051 31	615.2	2.55 x 10^{14}	2.41 x 10^{-12}
3	0.035 40	41.46	2.56 x 10^{13}	1.62 x 10^{-12}
4	0.013 51	10.33	1.81 x 10^{13}	5.71 x 10^{-13}
5	0.005 95	0.50	1.6`1 x 10^{13}	3.10 x 10^{-14}

Figure 4-39 show the original output voltage and the extracted components (V_l(t)). The latter are shown in Figure 4-40.

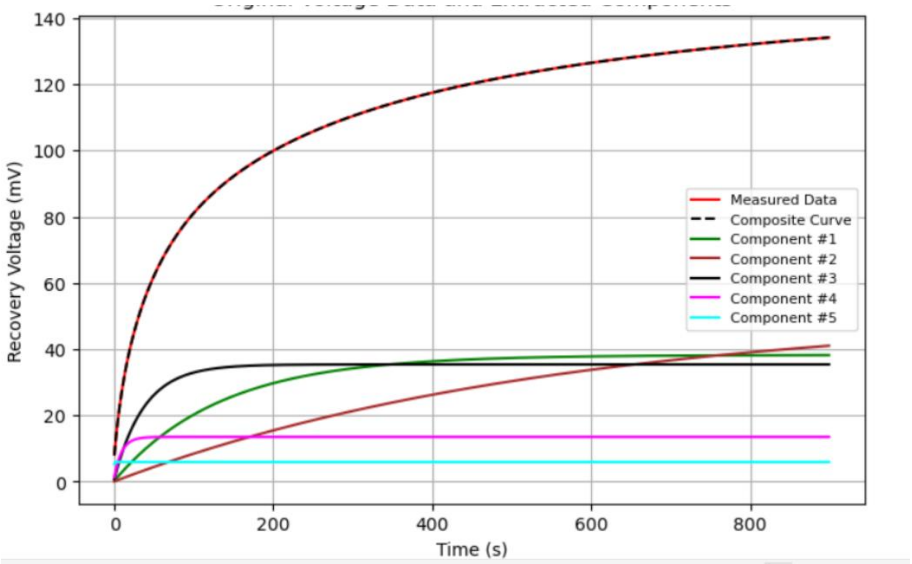


Figure 4-39: Measured data and extracted components for TDK #6A

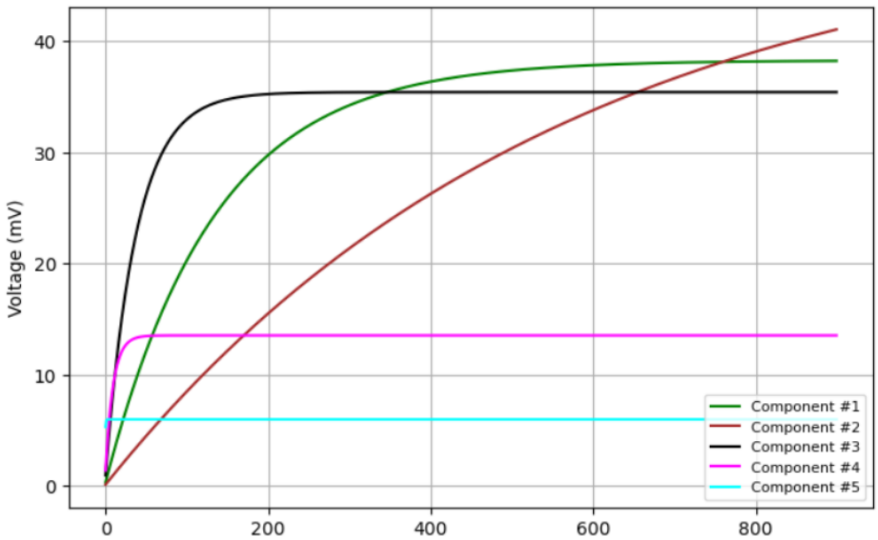


Figure 4-40: Extracted components for TDK #6A

4.4.4 LTSpice Model of dielectric absorption

The LTSpice model show in in Figure 4-41 was used to simulate the test sequence for the measurement of dielectric absorption.

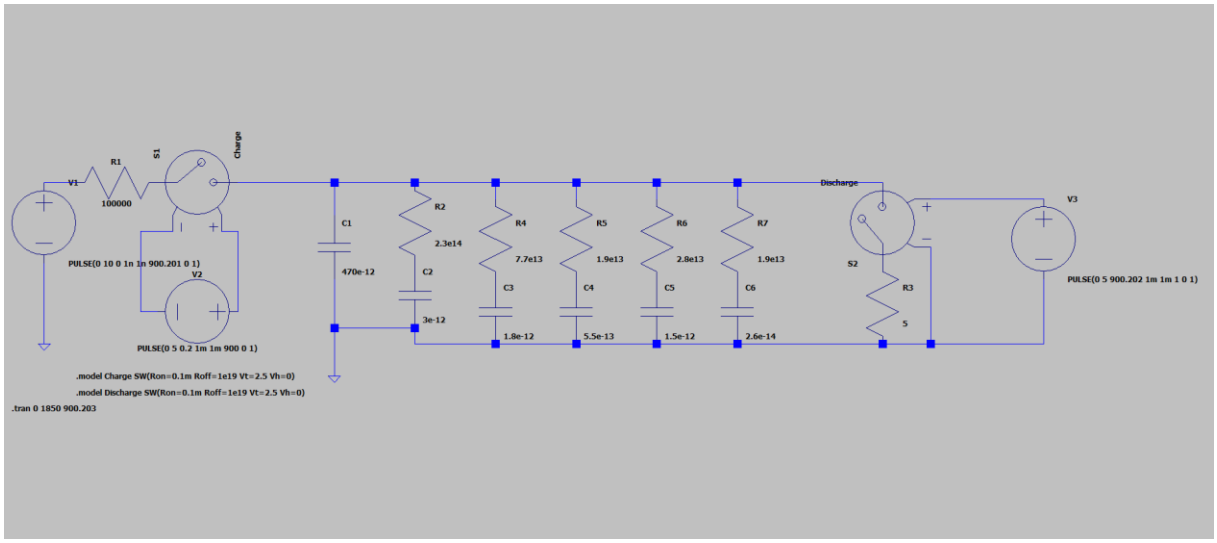


Figure 4-41: LTSpice simulation of dielectric absorption

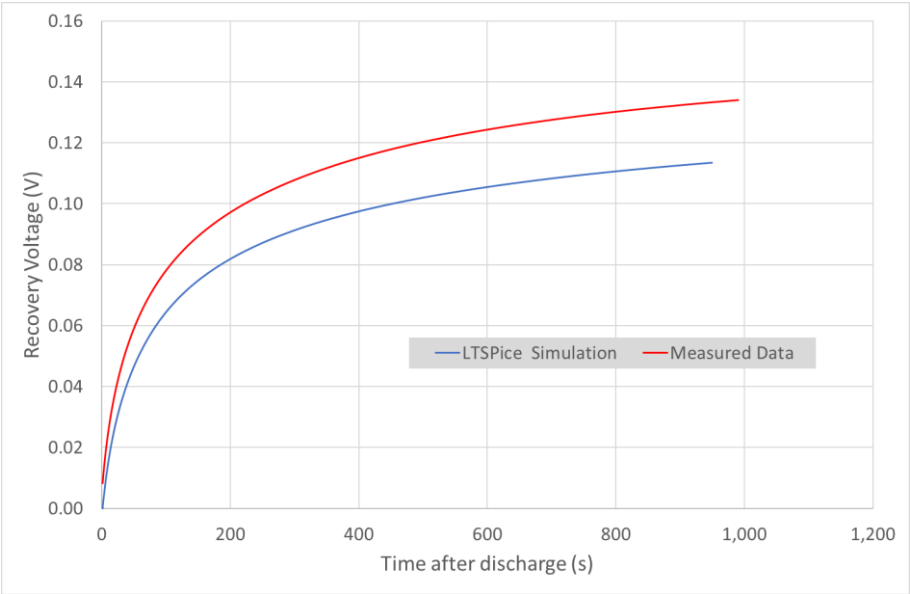


Figure 4-42: Comparison of measured recovery voltage with LTSpice simulation

5. CHARACTERISATION OF ELECTRONIC SWITCHES

5.1 Introduction

The main purpose of this activity is developing a measurement technic for electronic switches. There are several requirements for the switch in order to be used in digitizer application. The electronic switch should have:

- low ON resistance,
- low input and output capacitance,
- fast transients (low rise-times),
- break before make functionality,
- low charge injection,
- high repeatability,
- etc.

There were several candidates for the study:

- 4051, 4052, 4053 family (74HC4051; NXP and Onsemi; MC74LVX4053, SN54LV4053A, SN74LV4053A),
- ADG1411/ADG1412/ADG1413 (Analog Devices, Vishay Siliconix),
- Vishay DG2788A,
- Vishay DG333A, DG333AL,
- PI3A412.

The final switch that has been selected for the study was MC74HC4051A in SOIC−16 package.

5.2 Tested boards

The input and output pins of the MC74HC4051A are shown in Figure 5-1.

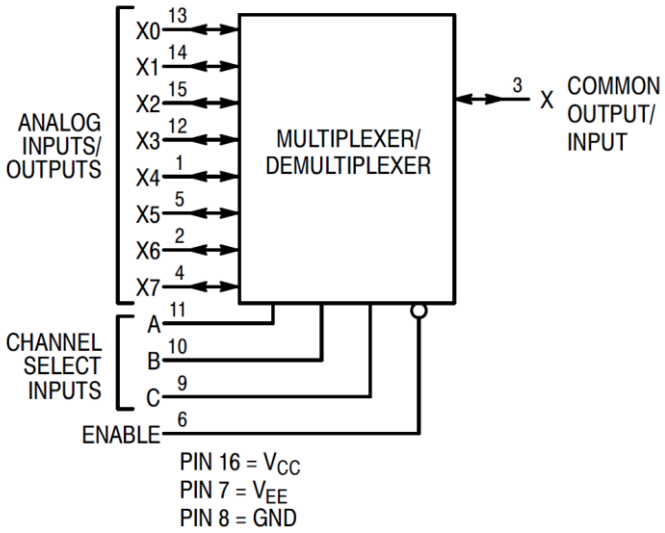


Figure 5-1: Input and outputs pins of selected electronic switch (multiplexer/demultiplexer)

The switch has eight analogue inputs and one common analogue output. There are also three digital channel selects inputs A, B and C, enable input. Other inputs are used for the power supply. The basic test circuit on protoboard is shown in Figure 5-2. It contains five BNC connectors for analogue inputs X_0 and X_1, analogue output X, channel select A and enable input. There are also additional test pins for other inputs if needed, although those inputs were not so thoroughly tested. There is also an option for a battery power supply so the measurement could be performed in a small Faraday cage in order to significantly reduce the noise and other disturbances form the ambient.

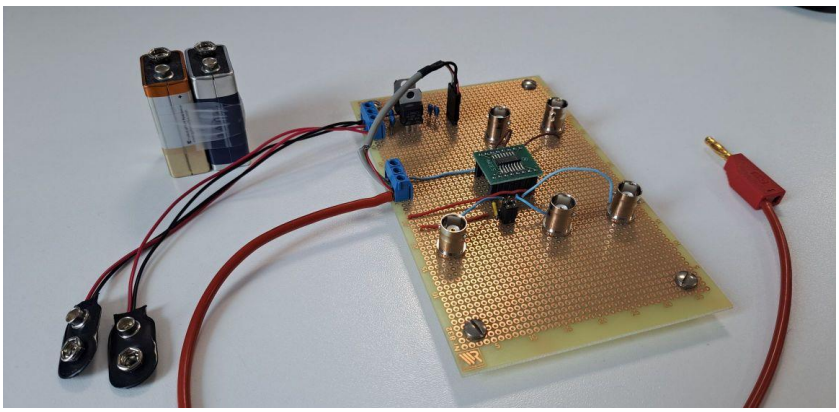


Figure 5-2: Testing board

5.3 Measurements

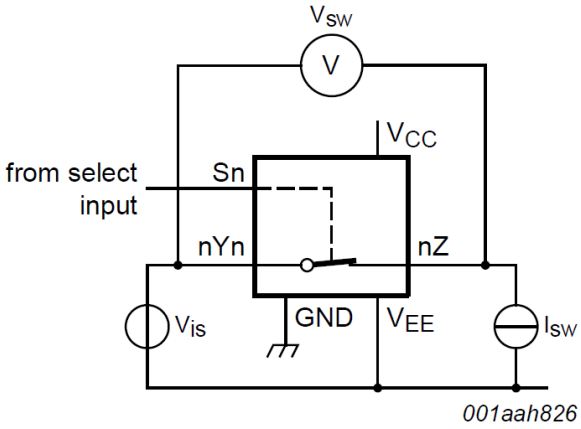
Withing the scope of this activity, several measurements has been performed:

- On-resistance,
- Input/output capacitance,
- Delay time,
- Rise time,
- Charge injection.

ON resistance

The principle for ON-resistance measurement is shown in Figure 5-3. The measurement is quire strait forward. The DC power source is connected to the input pin of the electronic switch and the current is measured at the output pin of the electronic swich. However, three points should be carefully considered here:

- The ON-resistance depends (RON) on input voltage; therefore, the measurements should be performed for different levels, which should be positive and negative. This makes laboratory DC power supply less appropriate since the terminal should be reversed and there might be an issue with the ground. Function generator seems to be more appropriate. The typical ON-resistance is shown in Figure 5-4.
- The combined ON-resistance and resistance of the Ampere meter does not perfectly match with the output impedance of the function generator which is usually 50 Ω based therefore the real output voltage of the function generator (i.e., the real input voltage that is attached to the input X0 pin of the switch) should be measured with the voltmeter.
- The Amper meter has a certain input impedance which should be also considered when calculating the RON resistance.



V_{is} = 0 V to (V_{CC} - V_{EE}).

$$R_{ON} = \frac{V_{sw}}{I_{sw}}$$

Figure 5-3: Principle for ON-resistance measurement

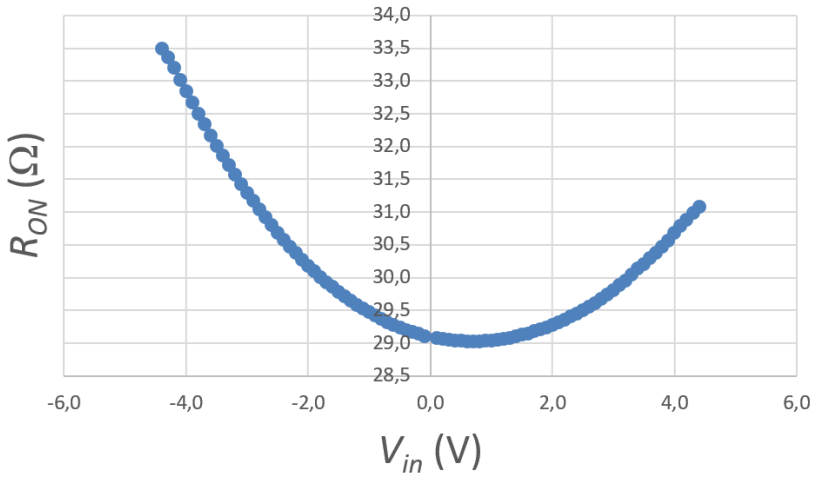


Figure 5-4: Typical R_{ON} resistance measured between input X_0 pin and output X pin for different input voltages.

5.3.1 Input, output capacitance

The input and output capacitance could be measured with LCR meter as shown in Figure 5-5. The measurement is quite strait forward. First the LCR and the cables should be open and short compensated as close to the measuring pin as possible, because any cable movement or changing of the measurement configuration changes the result. The best way is to remove the electronic switch from the base so only inactive connection (wires, BNC connectors) remains and then perform open compensation on BNC connector of interest. The short compensation should be performed similarly except that there should be a short connection between the pin of interest and the ground. Again, the electronic switch should not be connected to the base. After completing the compensation, the electronic switch should be attached to the base again and the capacitance should be measured on the BNC connector where the compensation was previously performed. In capacitance measurements it is also recommended to use a battery power supply since laboratory DC power source introduce distortions which affects the measured capacitance.

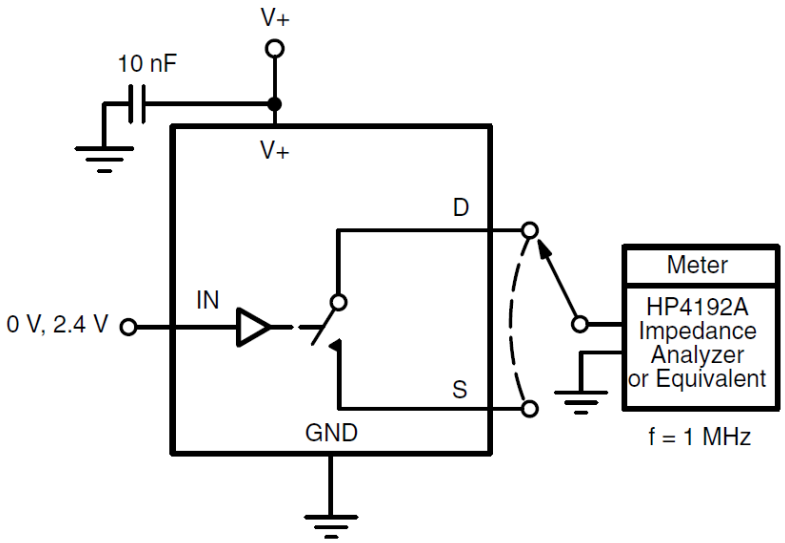


Figure 5-5: Principle for input and output capacitance measurement

There are three different capacitance that could be measured; (1) output capacitance where the IN and OUT pin are connected, this measurement is in principle the same as the input capacitance when the IN and OUT pin are connected, (2) input capacitance where the IN and OUT pin are disconnected and, (3) output capacitance where the IN and OUT pin are disconnected. Typical frequency responses are shown in Figure 5-6, Figure 5-7 and Figure 5-8.

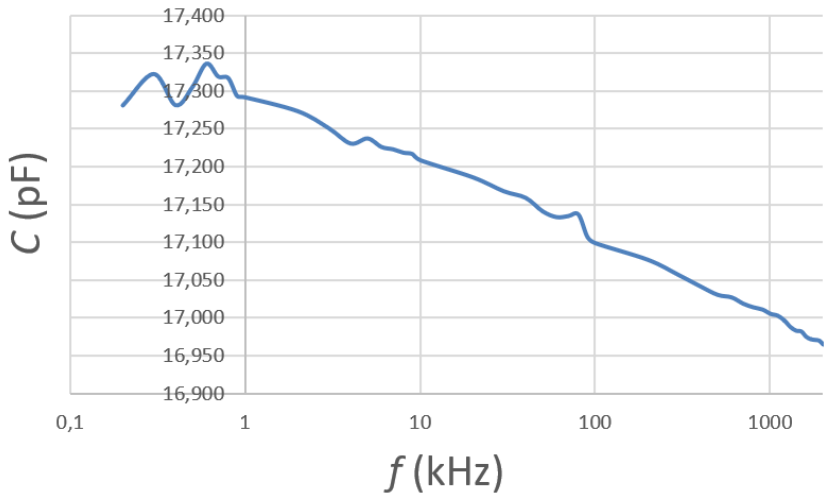


Figure 5-6: Typical frequency response of the output capacitance measured on output X, where IN and OUT are connected

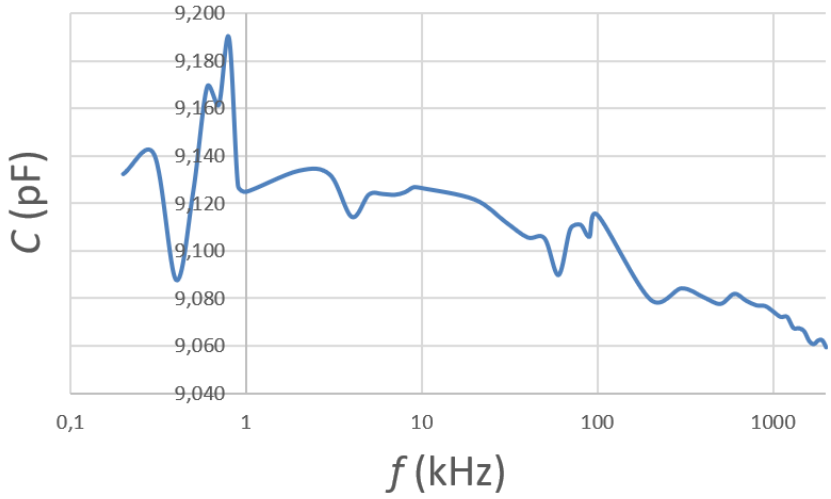


Figure 5-7: Typical frequency response of the output capacitance measured on output X, where IN and OUT are disconnected

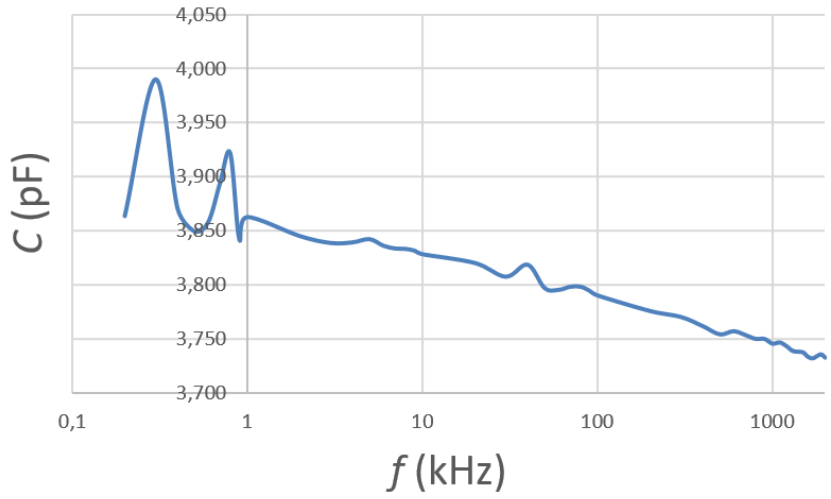


Figure 5-8: Typical frequency response of the input capacitance measured on output X_1, where IN and OUT are disconnected

5.3.2 Delay

For this measurement high bandwidth (500 MHz or more) two channel oscilloscope is required. The input pin (or select A or enable input) is connected to the Channel 1 of the oscilloscope and the output X is connected to the Channel 2 of the oscilloscope. The main parameter of interest is time delay between the input and the output. Three different time delays could be measured:

- E=0, A=B=C=0 and the input X_0 makes transition from 0 to 1 (Figure 5-8),
- X_0=1, E=0, B=C=0 and input A make transition from 0 to 1 (Figure 5-9),
- X_0=1, A=B=C=0 and E makes transition from 0 to 1 (Figure 5-10).

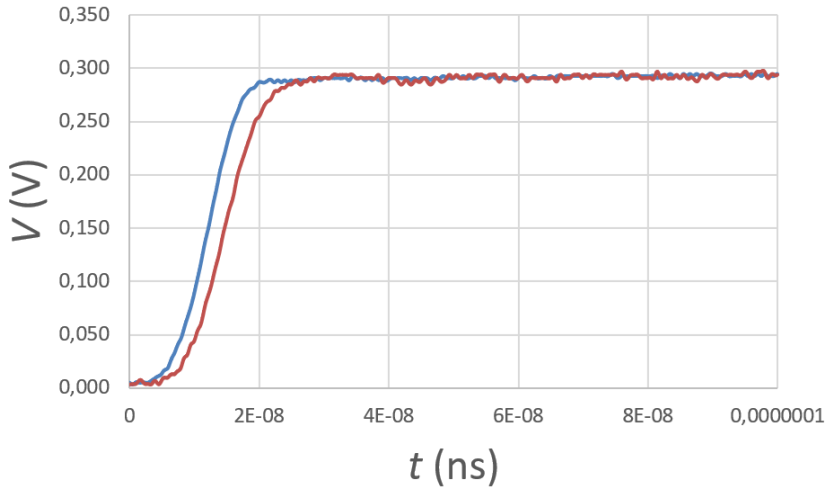


Figure 5-9: Typical time delay where the E=0, A=B=C=0 and the input X_0 makes transition from 0 to 1

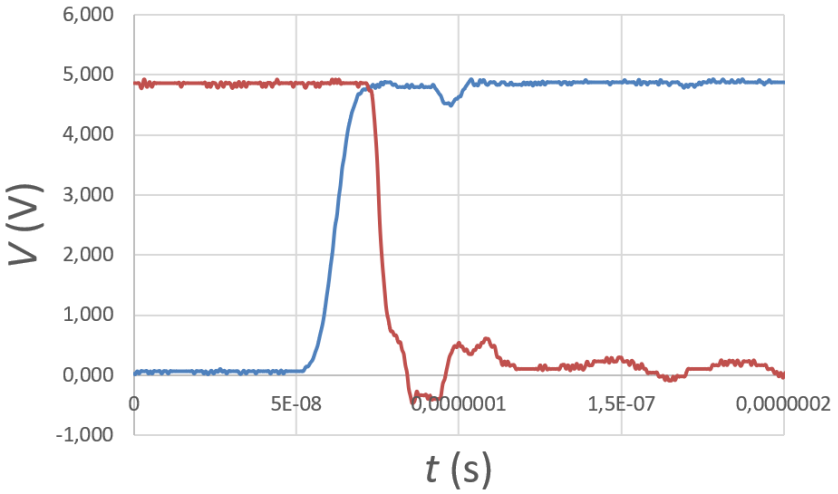


Figure 5-10: Typical time delay where X_0=1, E=0, B=C=0 and input A make transition from 0 to 1

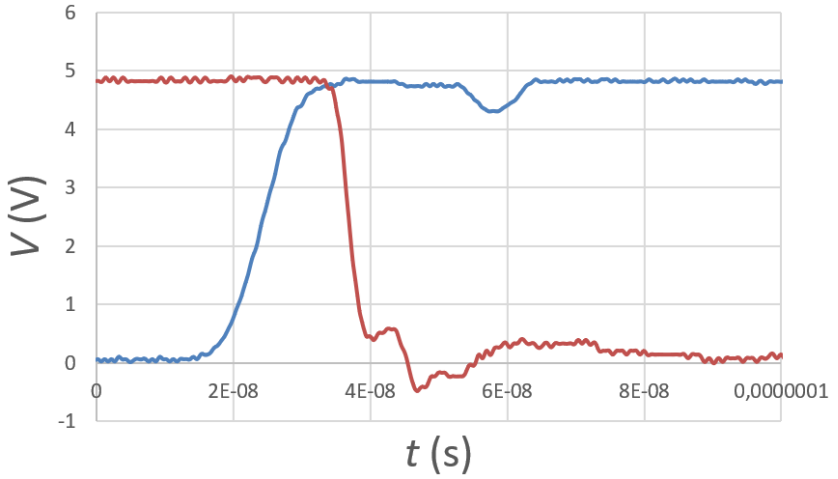


Figure 5-11: Typical time delay where X_0=1, E=0, B=C=0 and input A make transition from 0 to 1

There are a few remarks that should be considered when measuring the time delay:

- Oscilloscope and function generator are typically 50 Ω on-matching. On contrary, the electronic swich has a certain R_{ON} which makes a voltage divider between the input and the output which therefore reduces the output voltage by a certain factor. Therefore, a voltage scaling of the input and output signal is need after the measurements to define the propagation delay.
- Several other delays with inverted inputs and output are also possible to measure.
- The delay should be measured between the 50% point of the input signal and the 50% point of the output signal.
- Measurement in Faraday ‘s cage is recommended to limit noise and disturbances.
- Battery supply is recommended.

5.3.3 Rise-time

The input and output capacitance could be measured with LCR meter as shown in Figure 5-5. The measurement is quite strait forward. First the LCR and the cables should be open and short compensated as close to the measuring pin as possible, because any cable movement or changing of the measurement configuration

5.3.4 Charge injection

The input and output capacitance could be measured with LCR meter as shown in Figure 5-5. The measurement is quite strait forward. First the LCR and the cables should be open and short compensated as close to the measuring pin as possible, because any cable movement or changing of the measurement configuration

5.4 Conclusion and further activities

Several test for electronic switched has been developed and demonstrated. In the further step, the available datasheets should be examined and one or two the most promising candidate for electronic switch should be selected. A more advance test board should be made. There are some considerations that should be taken into account:

- The advance test board should also have test pins where accurate characterisation of the parameters of interest could be performed.
- The test pins should be as close as possible to the IC input/output pins so the resistance and the capacitance of the pins would not significantly affect the measured results.
- There are several other measurements that are characteristics for the electronic switched and they might be interesting for the characterization:
    - Static parameter:
        - R_{ON} match between channels, R_{ON} flatness when supply voltage is varied
        - Insertion loss (given in dB)
    - Dynamic parameters:
        - Break-before-make functionality
    - Other:
        - OFF-state isolation, Crosstalk between switches, Noise, THD, AC Power Supply Rejection Ratio, Frequency response and bandwidth, Maximum OFF channel leakage currents, ON-state and OFF-state current.

6. MEASURING CHARGE INJECTION OF ELECTRONIC SWITCHES

6.1 Why electronic switches

Electronic switches are key components in mixed electronics

- Analog voltage-controlled device and essential for building op-amp circuits, integrators, sample & hold, peak detectors, etc.
- FET & CMOS-most used, JFET - less used

Precise applications require electronic switches

- Zero – ON resistance, without attenuation or nonlinearity
- ∞ – OFF resistance, open circuit
- Low leakage currents, negligible capacitance to GND
- Low capacitance, negligible coupling to the control digital input

Key parameters for switch selections

- Voltage range – ON Resistance –Switching speed/frequency – Capacitance
- Charge injection – Switching time (Rise/Fall time) –Settling time, etc.
- Break-before-make switching (BBM)

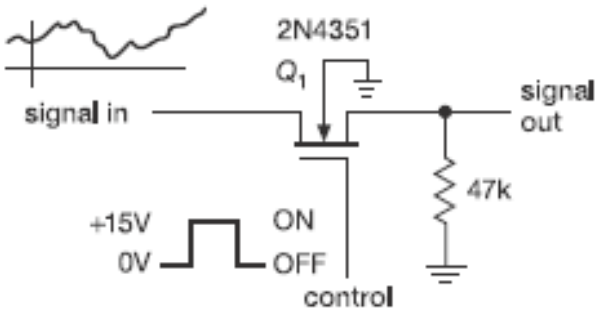


Figure 6-1: Electronic switch schematic

6.2 Selected electronic switches

Those proposed by partners (info from datasheets: difficult comparison, several parameters, sometimes different terminology)

- Texas Instruments CD74HC4053 (either 16 - TSSOP or 16 - SOIC)
    - On resistance 40 -70 Ω
    - Input capacitance 5 pF
    - Switching times up to 18 ns
    - Charge injection?
    - BBM Yes

- Onsemi MC74LVX4053 (either 16 - TSSOP or 16 - SOIC)
    - On resistance 26 -120 Ω
    - Input capacitance 10 pF
    - Switching times up to 50 ns
    - Charge injection 9-12 p
    - Cat 0 V
    - BBM Yes
- Vishay DG333A (either 20-TSSOP or 20-SOIC)
    - On resistance 15 -150 Ω
    - Input capacitance 8-12 pF
    - Switching times up to 175 ns
    - Charge injection -20-30 pC
    - BBM Yes
- Analog Devices ADG1413 (16-TSSOP)
    - On resistance 1.5 -6 Ω
    - Input capacitance 8-12 pF
    - Switching times up to 250 ns
    - Charge injection -20 pC, Vs=0,
    - BBM Yes

6.3 Carrier board selected for switch characterization

- Commerciality available
- Flexibility and scalability
- TSSOP package
- Reconfigurable for single/dual supply

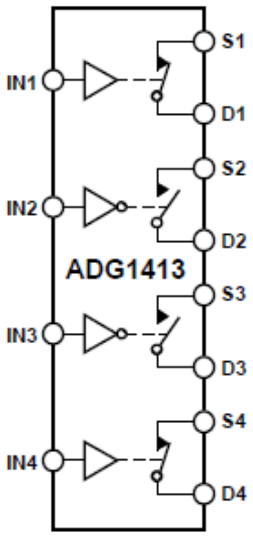


Figure 6-2: ADG1413

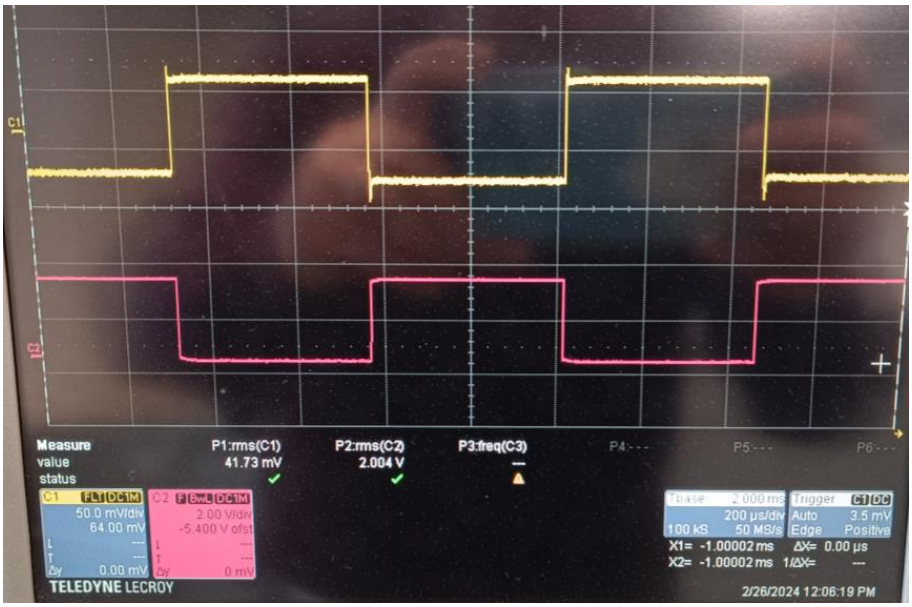


Figure 6-3

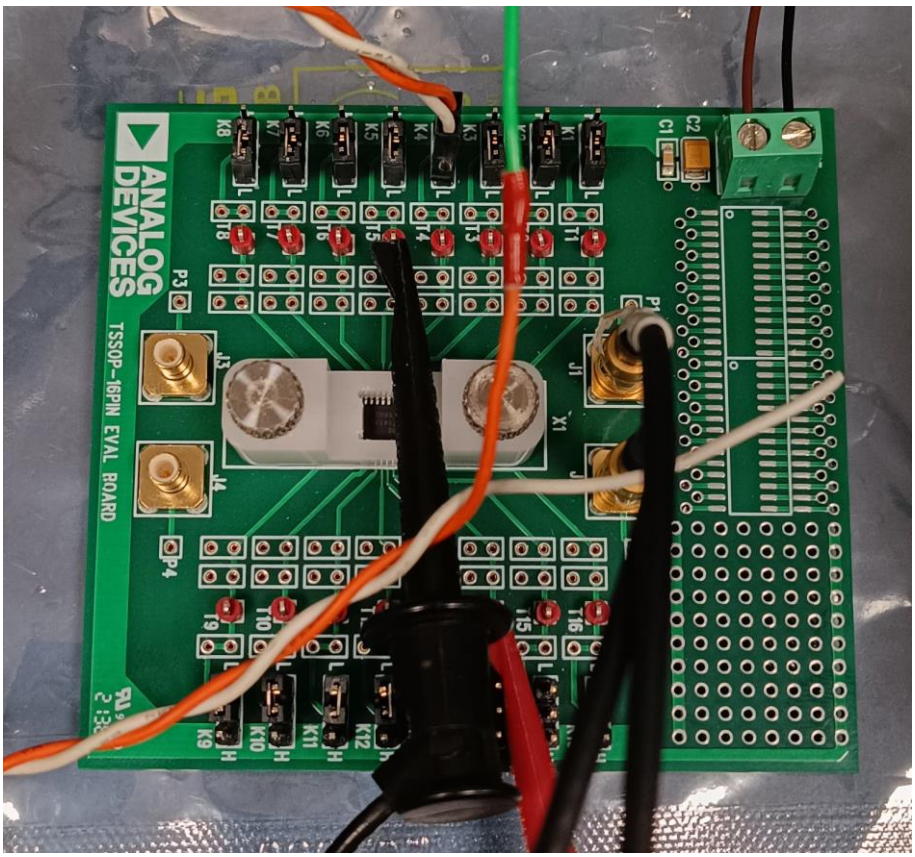


Figure 6-4

6.4 Measurement strategy

Charge injection, during turn-on and turn-off transients. Control signal (gate) can couple capacitively to the drain and source channels. Net amount of charge transfer (injection) to the channel depends only on the total voltage change at the gate, not on its rise time.

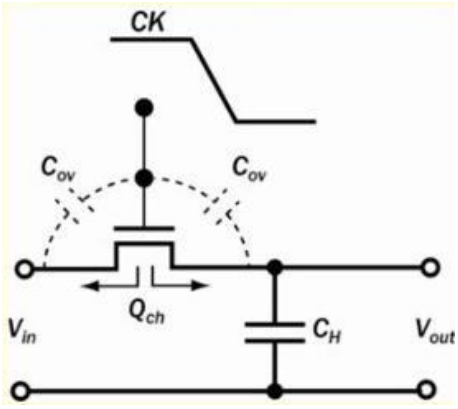


Figure 6-5

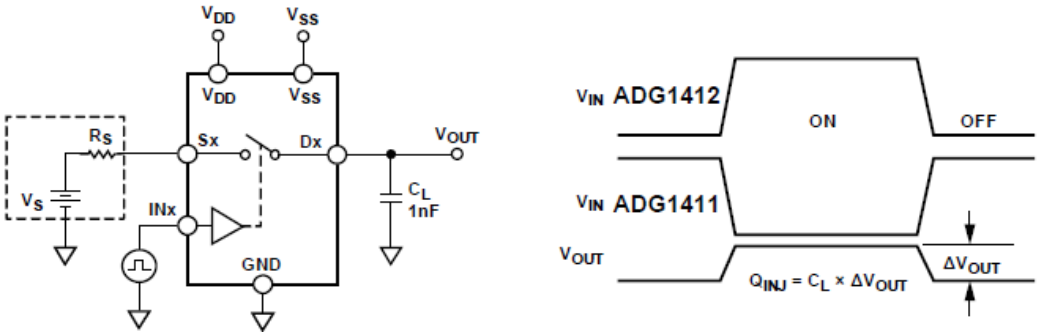


Figure 6-6

6.5 Practical implementation of the measurement method

What on how to measure?

Eq. 6-1: $Q_{INJ} = C_L \cdot \Delta V$

Eq. 6-2: $\Delta V = V_{ON}^{Switch} - V_{IN}$

Increasing the Switch ON-OFF frequency to compensate for time constants of the measurement environment.

Reaching a measurement condition in which the voltage shape at the output of C_{Lis} similar to a rectangular / square waveform (rectangular approximation).

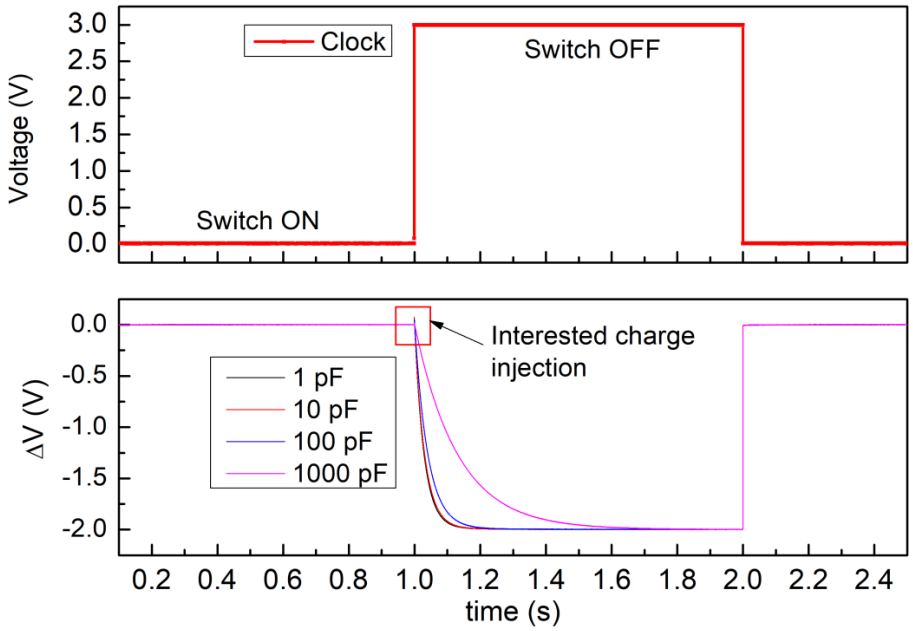


Figure 6-7

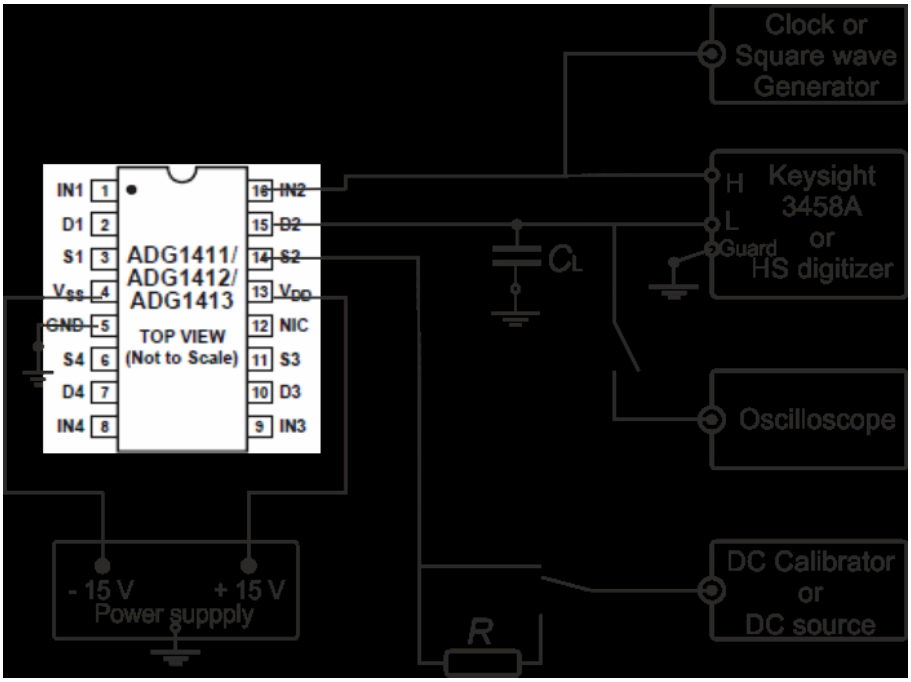


Figure 6-8

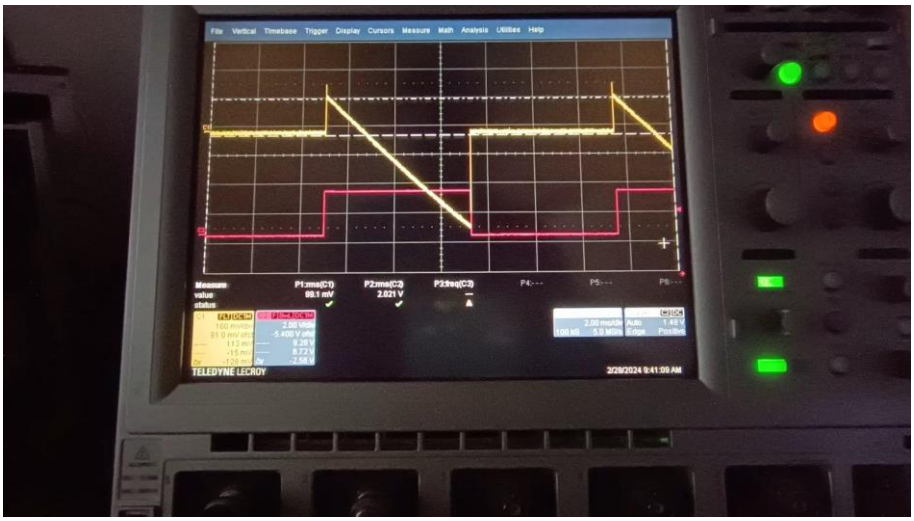


Figure 6-9: Method demonstration

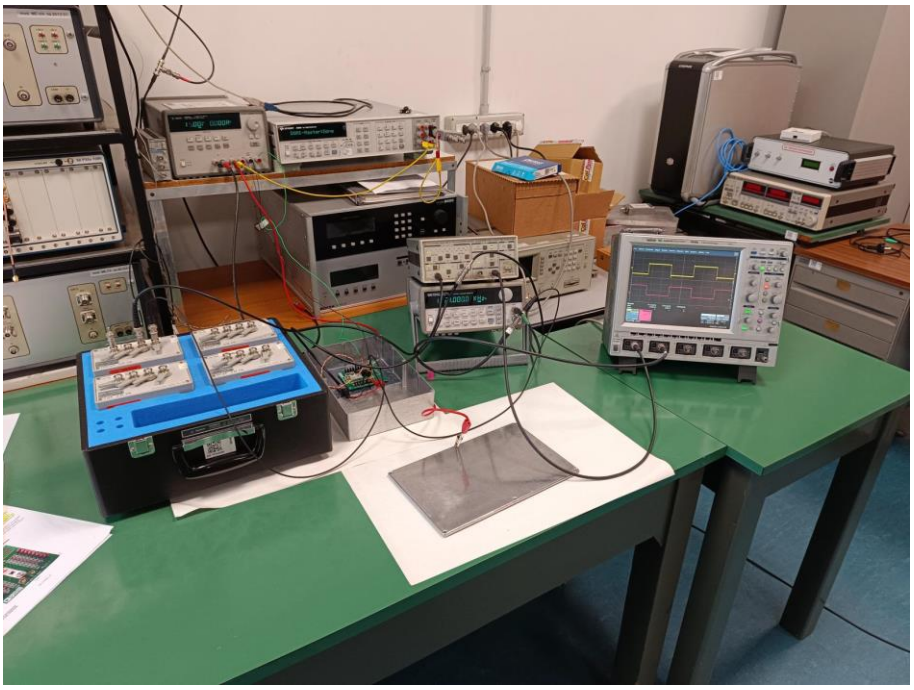


Figure 6-10: Experimental setup for traceable measurement of charge injection

- Gas - dielectric standard capacitor from 1 pF to 1000 pF traceable to national capacitance standard from 50 Hz to 20 kHz.
- DMM 3458 sampling, traceable to DC Josephson voltage standard.
- Fluke 5730A DC calibrator.

6.6 Experimental results

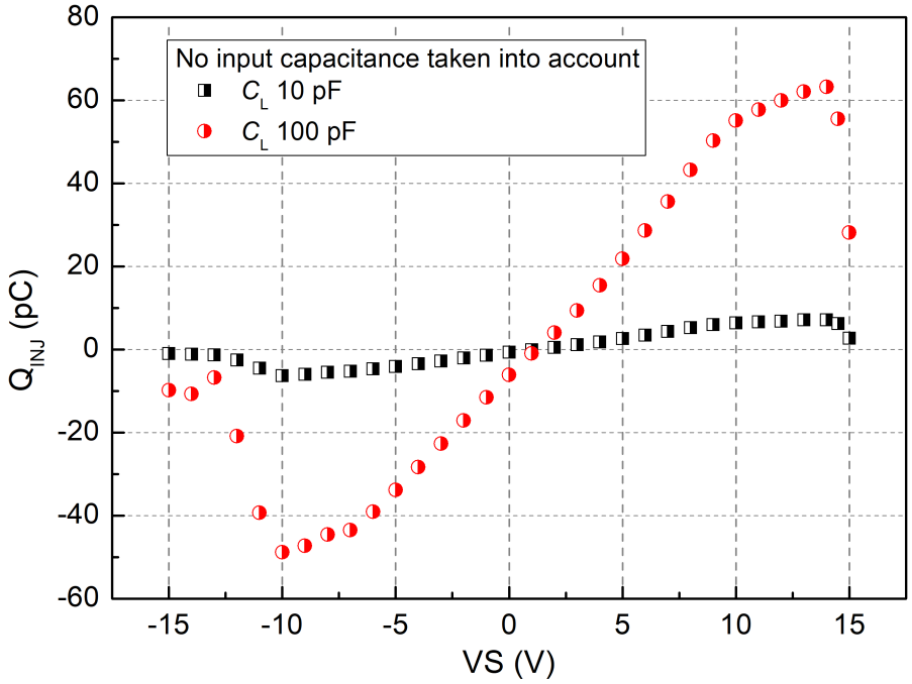


Figure 6-11: Simple voltage configuration ($Q_{INJ} = C_L \cdot \Delta V$)

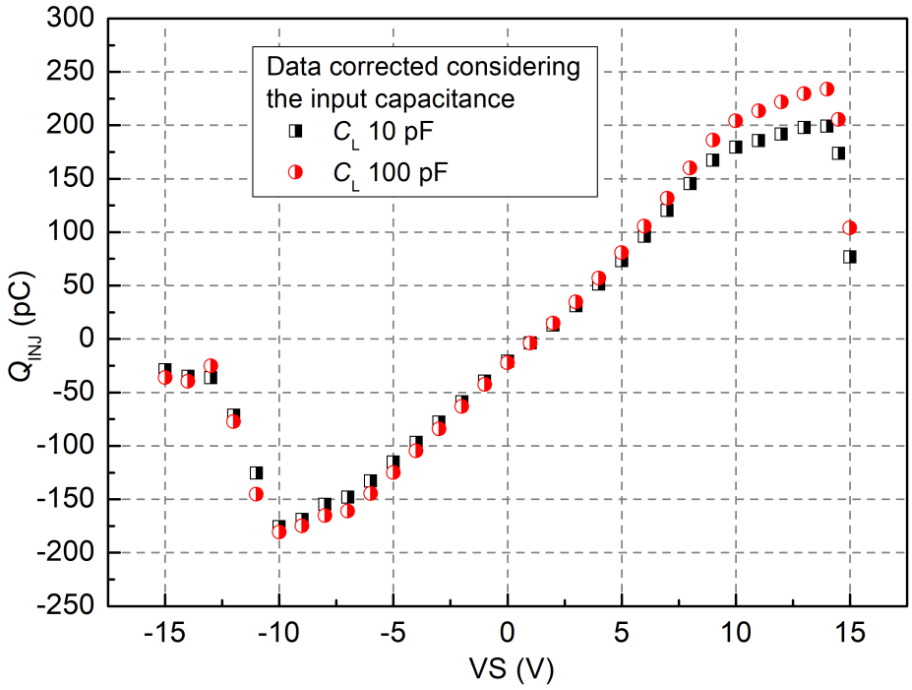


Figure 6-12: Simple voltage configuration ($Q_{INJ} = (C_L+C_{IN}) \cdot \Delta V$)

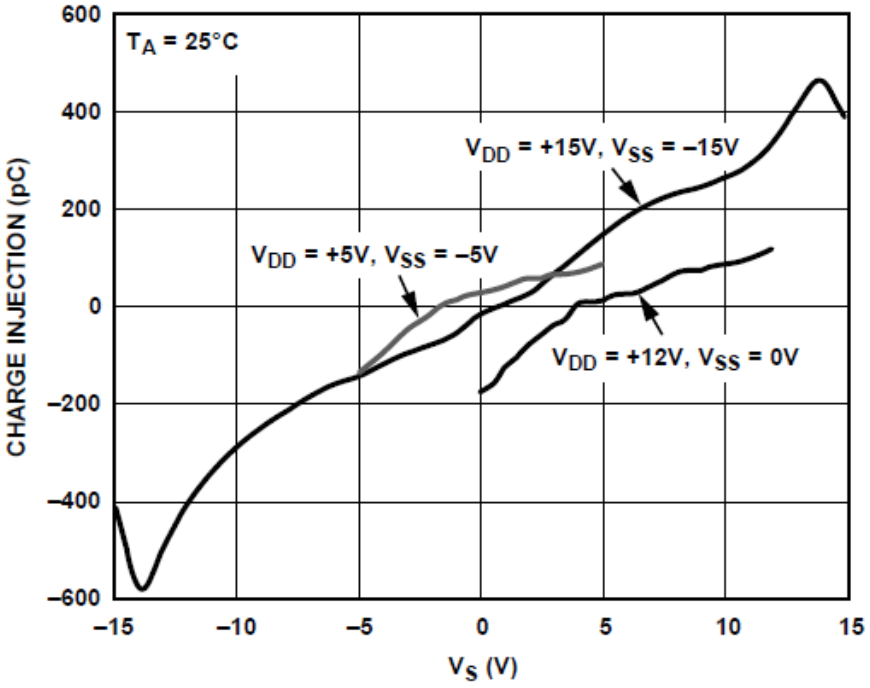


Figure 6-13: Simple voltage configuration (from datasheet)

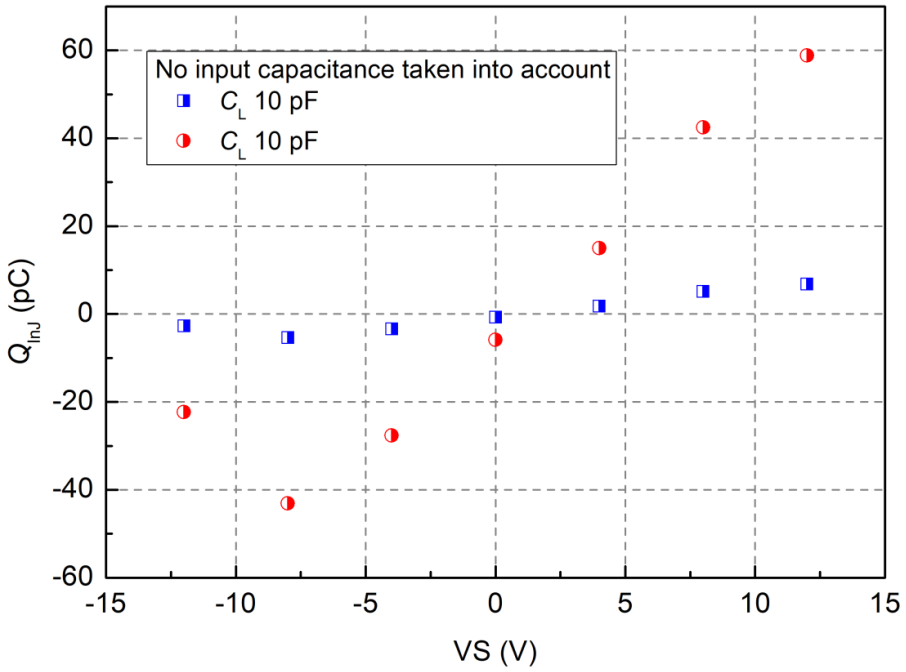


Figure 6-14: Current steering configuration ($Q_{INJ} = C_L \cdot \Delta V$)

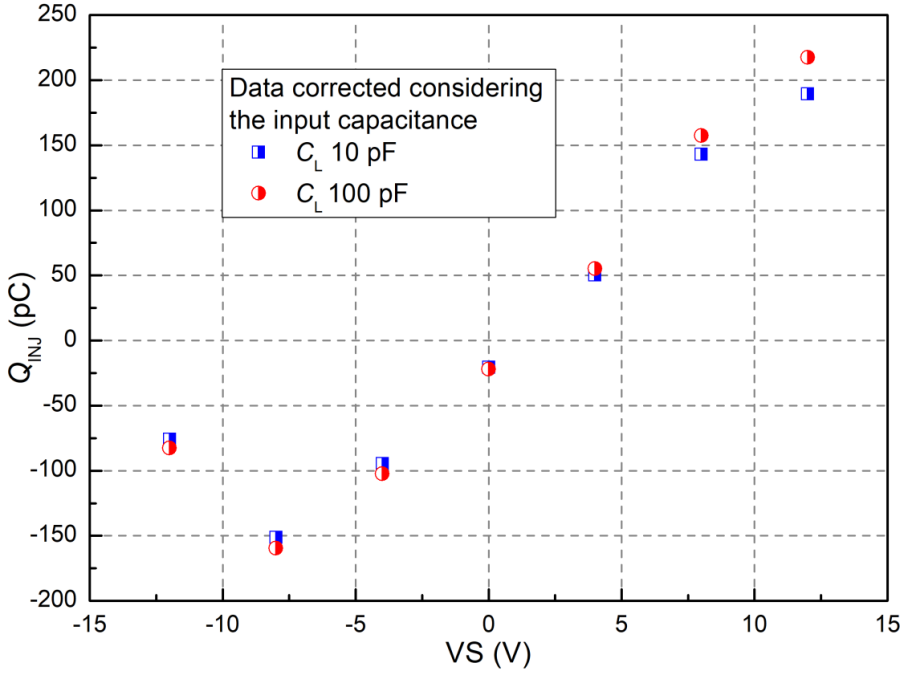


Figure 6-15: Current steering configuration ($Q_{INJ} = (C_L+C_{IN}) \cdot \Delta V$)

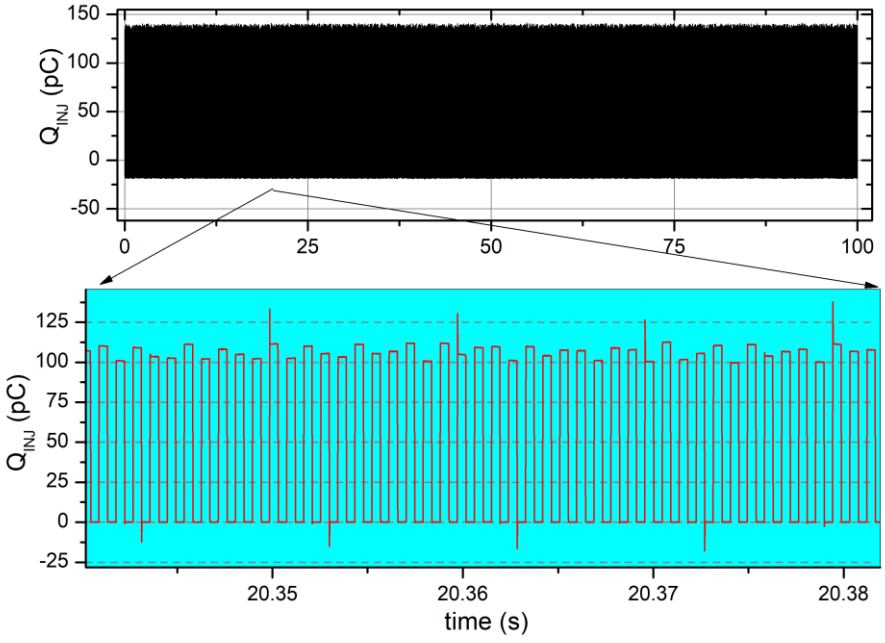


Figure 6-16: Long time frame (V_S = 6V, dual supply, C_L = 100 pG, $Q_{INJ} \approx$ 13 pC)

6.7 Conclusions

- Method for traceable charge injection measurement in electronic switches has been established
- Setup of experimental setup completed
- First measurement on ADG1413 completed

7. CHARGE INJECTION TEST

7.1 Standard test

C_2 and follower IC_{3B} used, 74HC4053 and TMUX1133 tested V_{dd} = 3 V and V_{ee} = - 2 V, switching frequency is 2 kHz.

7.1.1 74HC4053

Voltage step = 33.8 mV, $Q_i = \Delta U \cdot C$ = 15.9 pC.

Figure 7-1: 74HC4053

7.1.2 TMUX1133

ΔV = 2 mV, Q_i = 0.94 pC.

Figure 7-2: TMUX1133

7.2 Integrator

Two signals were used for S_{nul} and S_{in}, frequency is 2 kHz, duty cycle 40% (t_{on} = 200 us, t_{off} = 300 us), phase shift is 180 degrees, so there are two non-overlapping signals with 50 us delay between each t_{on}, switches are connected as current switches between ground and input of the integrator.

Figure 7-3: Integrator with 74HC4053

Figure 7-3 shows the output of the integrator - yellow trace and the S_{in} control signal - green trace for 74HC4053. A large step is visible during the on-switching, a small step during the off-switching. The value of the step is similar to the standard test for t_{on}, significantly lower for t_{off}. Total charge injection for the whole cycle is approximately 21 pC.

Figure 7-4 shows TMUX1133, t_{on} step is significantly worse than in the standard test, but it is partially compensated by the opposite step during t_{off}, the total charge is 9.4 pC, still significantly worse than in the standard test.

Figure 7-5 shows another situation - S_{in} remains the same, S_{nul} has been changed - t_{on} is 100 us, t_{off} is 1.9 ms - see green trace, so 4 cycles of S_{in} have been accumulated before zeroing.

Figure 7-4: Integrator with TMUX1133

Figure 7-5: Integrator with TMUX1133, 4 cycles

8. CONCLUSION

In this report on metrological methods for characterisation of resistors and capacitors for their stability, tracking and non-linear behaviour down to and below -120 dB THD and results obtained on a selected set of high-grade resistors and capacitors, the following results were obtained.

Resistor non-linear behaviour was characterised using a modified bridge, which uses a single ended signal source and a spectrum analyser. As the test resistor was of the highest quality with the best available linearity, a special parallel/serial combination was used as a reference resistor to reduce its nonlinearity. A thorough mathematical model was developed and detailed circuit simulations were conducted to validate bridge operation. At 6 V across the resistor, the second and third harmonic distortion was found to be frequency dependent, and the bridge was capable of reliably measuring resistor nonlinearity down to –170 dBc, which is exceptional, compared to –120 dBc as initially planned in the project requirement. Different resistor types were clearly differentiated for their linearity performance. A second order mathematical model was developed to be used in simulations.

Capacitor non-linear behaviour was characterised using modified quadrature bridge. The same bridge topology was used as for the modified resistance bridge. Results for the NP0 capacitor showed harmonic distortions slightly frequency dependent for 5 kHz to 20 kHz, with harmonic distortions between –158 dBc and –164 dBc at 7 V across the capacitor. These distortions decreased as the voltage across the capacitor was reduced reaching a lower limit of –170 dBc, which was the limit of the measurement system used for those measurements. Again, these results are exceptional. A second order mathematical model was developed.

Four precision resistor arrays (100 Ω / 100 Ω, 10 kΩ / 10 kΩ, 100 kΩ / 10 kΩ, 100 kΩ / 100 kΩ) were characterised for their stability and tracking by direct measurement of their resistance ratio. Results have been presented for the temperature range from 15 ºC to 45 ºC and humidity range from 20 %rh to 80 %rh. The test conditions were provided by a climatic chamber. Very good results were obtained, clearly showing the performance of the evaluated resistor arrays. Stability over 6 days showed no measurable ratio change for 100 Ω / 100 Ω and 10 kΩ / 10 kΩ arrays, with relative sample standard deviation of 5×10^{-8} and mean standard deviation of 3×10^{-9} in best case. Further tests gave clear evidence of the sensitivity to varying temperature and humidity. Both temperature and humidity dependences were clearly observed, and hysteresis was evident on certain components. Temperature stability of well below 0.1 ppm/ºC could be resolved. Test for ratio sensitivity to humidity showed almost no sensitivity for hermetically sealed components, as expected, but an elevated sensitivity of up to 0,05 ppm/%rh was observed for plastic SMD packages. These results demonstrate that a solid metrological capability for precision resistor ratio testing has been developed and validated.

Capacitors were characterised for their temperature dependence, humidity dependence and dielectric absorption. The measurement setup which was developed allowed the temperature dependence of the capacitor to be studied over the range from 23 ºC to 43 ºC. The best NP0 capacitors were found to have temperature coefficients of approximately –10 ppm/ºC change for one manufacturer and +3 ppm/ºC for another manufacturer. These measurements were also repeated for a sample of capacitors drawn from two different batches and showed a very small spread of their temperature coefficients of ±0.2 ppm/ºC. For NP0 capacitors, the temperature dependence was found to be slightly nonlinear, and an appropriate model was developed. Further, the temperature dependence of the capacitor's loss component was also measured. A memory effect was found on certain devices, pointing out the need to carefully characterise components for the most critical uses. Sensitivity to humidity showed a clear nonlinear dependence, where the sensitivity to humidity changes increases with the humidity level. It also showed that this effect is slow, as it can take several hours before the capacitance value settles after a humidity change. This also resulted in a large hysteresis. Finally, dielectric absorption of the NP0 capacitors was measured using a method based on IEC 60384-1. The measurement set-up was designed for minimum leakage and the leakage current across the test capacitor during voltage recovery was less than 1 fA. The recovery voltage measured 990 s after a one second discharge was between 1 % and 1.6 % of the initial voltage. The recovery voltage increase was modelled with a five parallel RC

branches, giving a very good agreement with the measured values. This model can be directly used for the purposes of simulation.

Finally, electronic switches were characterised for their input and output capacitance, delay, rise-time and charge injection. Three measurement setups were used, each with its own capabilities and advantages. Different electronic switch components were characterised, enabling an informed selection between them for their intended application. Measurement of charge injection was of the highest importance, as it is generally not specified by the manufacturer. The charge injection, measured using standard test circuit, was found to be 16 pC for initially selected switch 74HC4053 and 1 pC for TMUX1133, which could serve the same purpose. However, using a circuit used in an integrating ADC (current steering switch), the charge injection increased to 21 pC for 74HC4053 and to 9.4 pC for TMUX1133. These results, considering other switch specifications, provide solid characterisation of electronic switch components, which are not available in the literature.

9. ACKNOWLEDGEMENT

This work would not be possible without major contributions from:

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- Chapter 3: IPQ,
- Chapter 4: NSAI,
- Chapter 5: SIQ,
- Chapter 6: INRIM,
- Chapter 7: JanasCard.

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