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Parallel Operation of High-Resolution Digitizers for AC and DC Signals: Improvements and Limitations

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Corresponding Author:	Luis Palafox PTB Braunschweig, Niedersachsen GERMANY
First Author:	Luis Palafox
Order of Authors:	Luis Palafox
	Rado Lapuh
	Ricardo Javier Iuzzolino, Dr
	Nikolai Vasilev Beev
Abstract:	While parallel operation of \bm{N} equal analog to digital converters or digitizers is theoretically established to improve signal-to-noise ratio %(SNR) by \bm{$\sqrt{N}$}, its efficacy in mitigating non-linearity — specifically integral non-linearity and total harmonic distortion — remains distinct between architectures. This paper presents an empirical comparison of parallel successive approximation register analog to digital converters operating in the AC regime and of parallel integrating analog to digital converters in the DC regime. Uniquely, this study investigates these effects on state-of-the-art commercial digitizers that are already optimized for superb linearity, questioning whether parallelization yields diminishing returns in this high-performance class.

Parallel Operation of High-Resolution Digitizers for AC and DC Signals: Improvements and Limitations

Rado Lapuh, Luis Palafox, Senior Member IEEE, Ricardo Iuzzolino, Nikolai Beev, Member IEEE

***Abstract*—While parallel operation of N equal analog to digital converters or digitizers is theoretically established to improve signal-to-noise ratio by $\sqrt{N}$, its efficacy in mitigating non-linearity — specifically integral non-linearity and total harmonic distortion — remains distinct between architectures. This paper presents an empirical comparison of parallel successive approximation register analog to digital converters operating in the AC regime and of parallel integrating analog to digital converters in the DC regime. Uniquely, this study investigates these effects on state-of-the-art commercial digitizers that are already optimized for superb linearity, questioning whether parallelization yields diminishing returns in this high-performance class.**

***Index Terms*—Analog-to-Digital Conversion, Parallel ADC, Linearity, SAR, Integrating ADC, Harmonic distortion.**

I. Introduction

HIGH-resolution digital sampling systems operating from direct current (DC) to the 100 kHz frequency range are a cornerstone of modern electrical metrology, precision instrumentation, and calibration systems [1]. Applications such as DC voltage realization [2], power and energy measurement [3], AC voltage measurements [4] and impedance metrology [5], [6] increasingly demand digitizers with combined requirements of ultra-low noise, exceptional stability, and sub-part-per-million linearity across a wide dynamic range.

While the noise performance of high-resolution digitizers has steadily improved over recent decades [7], linearity remains a fundamental limiting factor in achieving further accuracy gains [8]. Digitizer non-linearity directly translates into systematic measurement errors that cannot be mitigated by simple averaging in the time or frequency domains. As a result, improving linearity has become one of the dominant challenges in the development of next-generation metrology-grade digitizers.

Parallel operation of Analog to Digital Converters (ADCs) has long been recognized as an effective technique for improving signal-to-noise ratio (SNR) by averaging uncorrelated noise contributions from multiple converters [9]. However, averaging fundamentally reduces only uncorrelated noise components, while integral non-linearity and distortion mechanisms may remain correlated between channels [10], [11]. It is therefore not evident whether parallel operation of already highly linear digitizers can provide further improvement in linearity, or whether performance is limited by correlated error mechanisms inherent to the converter architecture.

The hypothesis of this paper is that the improvement in linearity from parallel channels is fundamentally limited by the correlation structure of the underlying error mechanisms, and that this limitation depends strongly on the ADC architecture. To investigate this hypothesis, two significantly different types of high-linearity digitizers were evaluated experimentally: digitizers based on Successive Approximation Register (SAR) ADCs operating in the AC regime and integrating ADCs (IADC) operating in the DC regime. By comparing noise scaling, harmonic distortion behavior, phase correlation of harmonics, and static transfer linearity, this work aims to distinguish which error components can be reduced through averaging and which remain fundamentally architecture-limited.

The remainder of the paper is organized as follows: section II introduces the correlation-based framework used to interpret improvements from parallel operation. Section III describes the experimental configurations. Sections IV and V present the SAR and integrating ADC results, respectively. Section VI discusses mitigation strategies and Section VII concludes the paper.

II. Improvements From Parallel Operation

The scaling of linearity metrics, such as integral non-linearity and total harmonic distortion (THD), is contingent upon the correlation of errors between parallel channels. If errors are systematic or correlated, simply averaging the outputs will not reduce their magnitude [10], [11]. While parallel operation of N channels is well established as a means of reducing uncorrelated noise by a factor proportional to $\sqrt{N}$, [12], the improvement of linearity metrics follows fundamentally different scaling laws. In particular, linearity enhancement depends not only on the magnitude of the underlying errors, but also on their correlation structure between parallel channels.

For a set of N parallel digitizers with equal gain and offset, purely random and statistically independent error components are expected to decrease proportionally to $1/\sqrt{N}$. In contrast, deterministic or strongly correlated error components remain largely unaffected by averaging. Real digitizers typically exhibit a combination of both behaviors, resulting in only partial

R. Lapuh is with Left Right s.p., Ljubljana, Slovenia, (e-mail: rado.lapuh@leftright.eu), L. Palafox is with the Physikalisch-Technische Bundesanstalt, 38116 Braunschweig, Germany, R. Iuzzolino is with the Instituto Nacional de Tecnología Industrial (INTI), Buenos Aires, Argentina, and N. Beev is with the European Organization for Nuclear Research - CERN, Geneva, Switzerland, and the Slovak University of Technology, Bratislava, Slovakia.

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suppression of non-linearity. Consequently, the achievable improvement in metrics such as integral non-linearity, THD, and signal-to-noise-and-distortion ratio (SINAD) is fundamentally limited by the degree of correlation of the dominant error mechanisms [13].

A useful first-order description of this behavior can be obtained by considering that the error components in each channel have equal variance σ_e^2 and a common pairwise correlation coefficient ρ. Using the covariance of averaged correlated random variables [14], the variance of the averaged error becomes

$$\sigma_{\bar{e}}^2 = \frac{\sigma_e^2}{N}\left[1 + (N-1)\rho\right]. \tag{1}$$

This expression reduces to the familiar $1/N$ variance scaling for uncorrelated errors ($\rho = 0$), while for fully correlated errors ($\rho = 1$) no reduction is obtained. For partially correlated errors, the achievable improvement lies between these two limiting cases. Although this model is simplified, it provides a useful interpretation of why noise, harmonic distortion, and static transfer non-linearity can scale differently under parallel operation.

This work adopts a correlation-based conceptual framework for the analysis of parallel digitizer operation. Under this interpretation, the effectiveness of parallelization depends on which error class dominates the overall transfer characteristic. Digitizer errors are separated into three categories: 1) uncorrelated stochastic errors, such as thermal noise, 2) partially correlated errors, arising from component mismatch, asymmetry, or drift processes, and 3) strongly correlated deterministic errors, originating from common architectural and silicon-level mechanisms.

This distinction is particularly important for modern state-of-the-art digitizers, where random noise has already been reduced to extremely low levels and systematic effects increasingly dominate performance. In high-linearity SAR ADCs, harmonic distortion mechanisms are frequently linked to capacitor arrays, comparator structures, and charge redistribution processes, which may exhibit strong correlation even between separate devices of the same type. Conversely, IADC architectures used in precision digital multimeters are influenced by a broader set of low-frequency analog-domain processes, including integrator dynamics, switching effects, and long-term drift phenomena, which may exhibit weaker inter-channel correlation.

The observed limitations are conceptually related to the mismatch problem in time-interleaved ADC systems, where calibration is often required to suppress systematic channel-dependent errors [15]. Similarly, this work investigates calibration-based correction methods for residual multi-channel linearity errors that cannot be sufficiently reduced through averaging alone.

III. Methodology and Experimental Setup

To investigate the correlation properties of linearity errors in parallel digitizers, three experimental configurations were evaluated, covering both AC and DC operating regimes. Two high-linearity SAR ADC systems were characterized under sinusoidal excitation to analyze harmonic distortion and phase correlation mechanisms, while a two channel metrology-grade IADC system was evaluated under DC excitation to investigate static transfer linearity and averaging behavior.

For all experiments, the digitizers were operated simultaneously and their outputs numerically averaged to emulate parallel operation. The measurements were designed to distinguish between stochastic and systematic error components.

A. SAR Architectures (AC Regime)

Two independent SAR-based digitizer platforms were evaluated to ensure that the observed behavior was not specific to a single converter implementation.

1) LTC2378 Platform: A four-channel differential input CERN FGC platform ANA200 digitizer board incorporating LTC2378-20 ADCs was used. Measurements were performed at $500\,\mathrm{kSa/s}$ using a $1\,\mathrm{kHz}$ ultra-low-distortion sine-wave generated by a JanasCard source [16]. In addition to conventional spectral analysis, this setup was used to investigate harmonic phase correlation between channels specifically. Particular emphasis was placed on identifying whether harmonic components combine coherently or de-correlate during averaging.

2) AD4630-24 Platform: A four-channel system was constructed combining two Analog Devices AD4630-24 dual-channel differential input evaluation boards [17]. Synchronization between the boards was achieved by routing the $100\,\mathrm{MHz}$ clock from one board to the other, the sampling rate was set to $2\,\mathrm{MSa/s}$. An Audio Precision APx555 analyzer provided the excitation signal. This setup enabled evaluation of both time-domain averaging and frequency-domain averaging behavior in a high-linearity SAR architecture.

B. Integrating ADC Architecture (DC Regime)

To compare the AC results with a fundamentally different converter architecture, two Keysight 3458A digital multimeters (DMMs) employing IADCs were evaluated at PTB. The digitizers were connected in parallel to a Programmable Josephson Voltage Standard (PJVS), which generated quantum-accurate DC voltage steps between $\pm 10\,\mathrm{V}$.

Measurements were performed using number of power line cycles (NPLC) settings of 10 and 50 to investigate the influence of integration time on linearity correlation. Parallel operation was emulated by averaging the simultaneously acquired measurement results from both DMMs.

IV. SAR digitizer Results

Fig. 1 shows the connection diagram for the CERN LTC2378 four channel SAR ADC platform. All four channels sampled simultaneously using a common trigger. The source used is an analog ultra-pure oscillator [16] and synchronisation with the ADC was not possible. The source provided a sine wave signal close to $1\,\mathrm{kHz}$ with harmonic distortion below $-140\,\mathrm{dBc}$. In Fig. 1, channels 3 and 4 are shown in the inverted polarity connection and the arrows indicate which connections are swapped for the non-inverting connection. The maximum input amplitude is $10\,\mathrm{V}$.

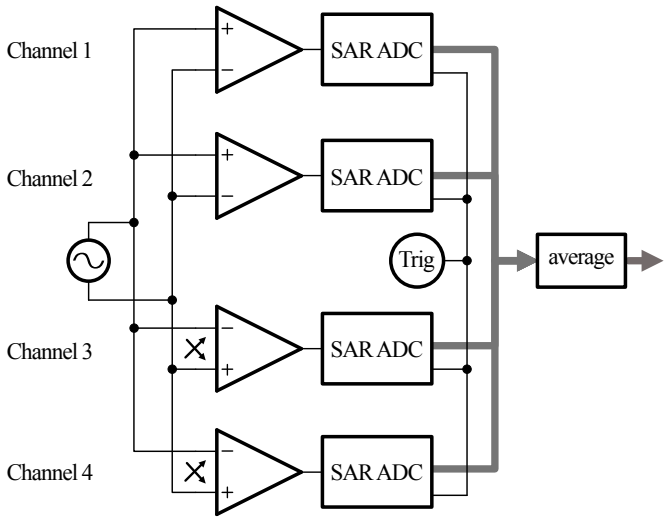

Fig. 1. Block diagram of the LTC2378 four channel SAR ADC platform. The arrows indicate which channels are swapped between the inverting and non-inverting connections.

Fig. 2 shows the connection diagram for two AD4630-24 evaluation boards [17] using a single 100 MHz clock. Each evaluation board has two SAR ADC channels with differential inputs. Two PCs were required to retrieve data from the evaluation boards. The source used was the analog generator in an Audio Precision APx555 audio analyzer, generating differential sine wave signals with harmonic distortion below -140 dBc. As no trigger input is provided on the evaluation boards, very long sample records were used and the output of the APx555 was switched on after starting the acquisition. The records were then aligned in time to the first zero crossing of the steady signal and split into frames for the analysis in the time and frequency domains.

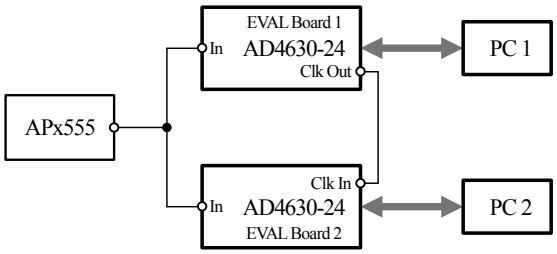

Fig. 2. Block diagram of two AD4630-24 evaluation boards connected in parallel. The input connection is a parallel connection of the differential output from APx555 to two differential channels on each AD4630-24 board.

A. Noise Performance

The SNR measured with both SAR-based digitizer platforms are summarized in Table I for the individual channels and when operated in parallel. Both cases show the expected reduction of uncorrelated noise components from parallel channels. The amplitudes chosen are large enough to realistically show the performance of the digitizers without entering large-signal limitations closer to their respective Full Scale (FS) amplitudes. For the CERN LTC2378 platform, four-channel averaging improved the SNR from approximately 93.9 dB for a single channel to 99.9 dB, corresponding closely to the theoretical $\sqrt{N}$ scaling for $N = 4$. The AD4630-24 platform shows a marginally smaller reduction in the noise level of 5.72 dB.

These results confirm that the dominant noise contributions between channels are largely uncorrelated and therefore combine according to conventional statistical averaging laws.

TABLE I
SNR RESULTS FOR PARALLEL OPERATION OF TWO SAR BASED DIGITIZERS AT 7.5 V FOR THE CERN LTC2378 PLATFORM (-2.50 dBFS) AND 4.37 V (-1 dBFS) FOR THE AD4630-24 SYSTEM.

	SNR (dB)				
Channel	1	2	3	4	‖
LTC2378	93.94	93.99	94.01	94.02	99.91
AD4630-24	103.35	103.04	103.07	103.04	108.84

B. Linearity

In contrast to the noise behavior, harmonic distortion did not improve comparably under parallel operation. Tables II to V summarize the measured THD and individual harmonic components for both SAR platforms. THD was evaluated using the first nine harmonics for the LTC2378 platform and the first four harmonics for the AD4630-24 platform.

For the AD4630-24 system (see Table II), the averaged THD lies between the best and worst individual channel results, showing no clear improvement. A similar behavior was observed for the LTC2378 platform, where the averaged THD remained close to the individual channel performance, as shown in Tables III and IV for the inverted polarity configuration. Fig. 3 plots the spectra for channel 1 and for parallel operation, i.e. the average of the four channels, for both polarity configurations ans shows a clearly lower noise floor independently of the polarity. These results indicate that the dominant distortion mechanisms are not statistically independent between channels.

TABLE II
THD AND HARMONIC AMPLITUDES FOR THE AD4630-24 DIGITIZER FOR A -1 dBFS, OR 4.37 V INPUT SIGNAL.

Channel	THD dB	HD2 dBc	HD3 dBc	HD4 dBc	HD5 dBc
1	-137.5	-141.2	-141.0	-150.3	-149.1
2	-144.8	-151.7	-149.8	-152.2	-150.0
3	-138.0	-141.3	-141.5	-154.5	-149.5
4	-143.8	-148.1	-148.5	-155.6	-150.1
‖	-143.5	-154.3	-145.0	-157.3	-151.2

To further investigate the origin of the limited distortion improvement, the phase relationship of individual harmonic components was analyzed for the LTC2378 platform. Figs. 4 and 5 show the relative harmonic amplitudes and phases for the four channels in the normal and inverted polarity connections.

The polarity inversion experiment provides additional insight into the correlation properties of the observed distortion

TABLE III
HARMONIC DISTORTION FOR THE CERN LTC2378 DIGITIZER IN THE NON-INVERTING CONFIGURATION FOR −2.50 dBFS, OR 7.5 V INPUT AMPLITUDE.

Channel	THD dB	HD2 dBc	HD3 dBc	HD4 dBc	HD5 dBc
1	−121.3	−123.1	−126.4	−149.3	−136.7
2	−123.0	−126.8	−126.1	−145.8	−135.1
3	−119.0	−120.1	−126.3	−150.7	−137.5
4	−123.7	−126.5	−127.4	−145.9	−139.0
‖	−122.6	−125.3	−126.6	−148.9	−137.0

TABLE IV
HARMONIC DISTORTION FOR CERN DIGITIZER WHEN THE POLARITY OF CHANNELS 3 AND 4 IS INVERTED.

Channel	THD dB	HD2 dBc	HD3 dBc	HD4 dBc	HD5 dBc
1	−121.3	−123.2	−126.3	−149.7	−136.1
2	−122.8	−126.7	−125.8	−144.9	−135.6
3	−119.5	−120.6	−126.6	−150.9	−137.7
4	−123.3	−126.3	−127.0	−148.7	−136.7
‖	−123.0	−126.2	−126.4	−149.1	−136.5

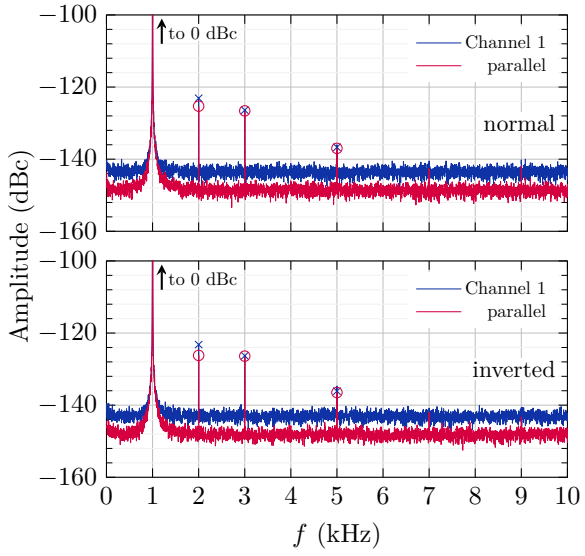

Fig. 3. Noise floor and largest harmonics from the CERN LTC2378 platform. The top plot shows the normal connection and bottom plot shows the inverted one. Harmonic levels are given in Tables III and IV.

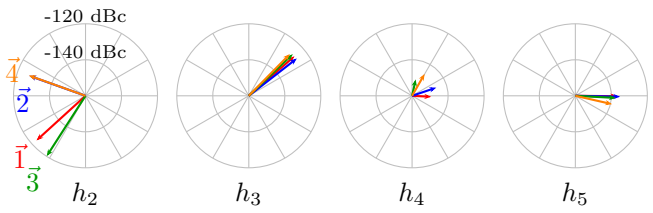

Fig. 4. Harmonic phases when the input signal was applied in the same polarity to all channels. Odd harmonics show highly correlated phases between channels.

components. When the input polarity of channels 3 and 4 was inverted, the odd-order harmonics remained highly phase coherent between channels, whereas the even-order harmonics exhibited substantial phase changes compared to the normal connection configuration. This indicates that the even-order distortion components are more sensitive to input polarity and channel asymmetry, while the odd-order components remain strongly linked to common converter behavior.

This behavior differs from the ideal response expected for simple memoryless polynomial non-linearity and indicates that the odd-order distortion mechanisms are strongly correlated and linked to architecture-dependent converter processes. As a consequence, the dominant odd-order harmonic components continue to combine coherently during averaging, which limits the achievable THD reduction despite parallel operation. It is the vector sum of these harmonic components that determines THD, so reverse polarity does not significantly reduce THD for the combined signal. Furthermore, the mismatch in harmonic amplitudes between channels hinders cancellation of even harmonics when operated in parallel.

TABLE V
SINAD RESULTS FOR PARALLEL OPERATION OF TWO SAR BASED DIGITIZERS AT 1 kHz. LTC2378 INPUT AMPLITUDE WAS 7.5 V AND AD4630-24 INPUT AMPLITUDE WAS 4.37 V

	SINAD (dB)				
Channel	1	2	3	4	‖
LTC2378	93.94	93.97	93.98	93.99	99.91
LTC2378∗	93.92	93.97	93.99	94.07	99.9
AD4630-24	103.35	103.04	103.07	103.04	108.84

∗ inverted connection for channels 3 and 4

Another common metric in this context is SINAD, defined as the ratio of signal power to the sum of noise and distortion powers [18]. The measured SINAD results are summarized in Table V. For both SAR platforms, the SINAD improvement closely follows the SNR improvement obtained through parallel averaging. This finding indicates that, for high-linearity ADCs, the overall SINAD remains predominantly noise-limited rather than distortion-limited. Consequently, the observed SINAD scaling largely follows the expected $\sqrt{N}$ behavior associated with the reduction of uncorrelated components.

V. IADC DIGITIZER RESULTS

To study parallel operation in DC, linearity measurements with the IADC systems were performed and revealed behavior

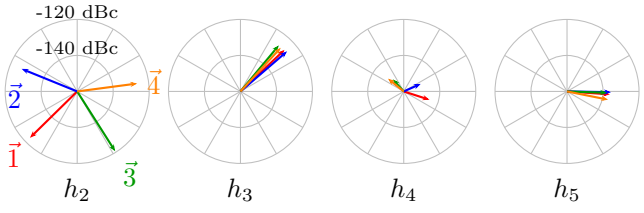

Fig. 5. Harmonic phases when the input signal was applied in inverted polarity to channels 3 and 4. The phases of odd harmonics were not changed and the phases of even harmonics did not reverse completely.

substantially different from the SAR-based digitizers discussed just above. The dominant limitation was measurement noise from the IADC at the selected settings rather than non-linearity. Consequently, aggressive averaging was required to extract the underlying transfer characteristic of each DMM with sufficient confidence.

During all measurements, the non-linearity profile observed remained stable and repeatable for each individual DMM, forming a distinct fingerprint of the corresponding IADC system. The persistence of this characteristic throughout the measurement campaign indicates that the deviation observed is non-statistical in nature and therefore not attributable to random noise processes.

All measurements were performed with the AUTO ZERO function enabled in order to suppress offset drift and low-frequency (*1/f*) noise contributions during the observation interval. The total measurement duration was intentionally limited to approximately 10 minutes to remain within the time window where AUTO ZERO effectively suppresses long-term drift mechanisms. Under these conditions, the remaining uncertainty was dominated by white noise, allowing the required averaging depth to be estimated from the expected DMM noise performance. It should be noted that enabling AUTO ZERO increases the overall noise by approximately $3\,\mathrm{dB}$ as each sample result is derived from the difference of two individual measurements [19].

A. Measurement Setup

The measurements were conducted using a Programmable Josephson Voltage Standard (PJVS), generating voltage steps from $-10.000\,021\,1\,\mathrm{V}$ to $10.000\,021\,1\,\mathrm{V}$ in $500\,\mathrm{mV}$ increments. Additional measurements at the maximum voltage from the PJVS for the chosen microwave frequency, $\pm 10.000\,060\,6\,\mathrm{V}$, and $0\,\mathrm{V}$ at the beginning and the end of each sweep were taken. Five measurements were performed at each PJVS voltage. The two DMMs were connected in parallel to the PJVS, as shown in Fig. 6, and operated in a master-slave configuration to ensure synchronized acquisition. Each increasing-voltage sweep was followed by a decreasing-voltage sweep in order to identify possible directional effects. The analysis of the measurements revealed no such hysteresis effects.

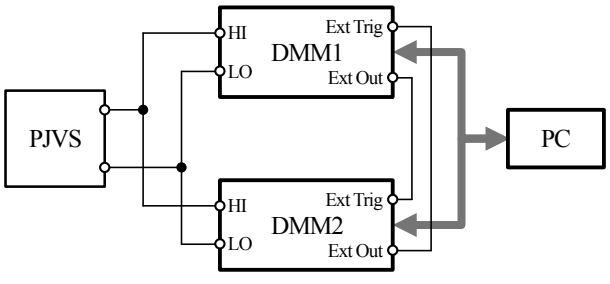

Fig. 6. Block diagram of two DMMs connected in parallel to a PJVS. Master-Slave operation was used, where the master was selected in software.

The DMM investigated produces approximately $15\,\mathrm{nA}$ input bias current spikes [20] during AUTO ZERO operation [19]. For this reason, additional sweeps were also performed with only one DMM connected to the PJVS. No significant difference was observed between these single instrument sweeps and when both DMMs were connected in parallel and operated in master-slave mode.

B. Selection of Required Averaging

Extraction of sub-$\mu\mathrm{V/V}$ non-linearity from integrating ADC measurements requires the stochastic noise contribution to be sufficiently reduced such that the residual transfer characteristic becomes observable. Assuming that the digitizer exhibits predominantly white-noise behavior, the required number of averages can be estimated directly from the standard deviation of the mean $\sigma_{\bar{x}}$

$$\sigma_{\bar{x}} = \frac{\sigma}{\sqrt{R}}, \tag{2}$$

where σ is the rms noise of a single measurement and R is the number of independent readings.

For the investigated DMMs operated in the $10\,\mathrm{V}$ range with $\mathrm{NPLC} = 10$ (corresponding to a $200\,\mathrm{ms}$ aperture time), the expected signal-to-noise ratio is approximately $150\,\mathrm{dB}$ near zero input voltage [21]. This corresponds to an equivalent rms noise of approximately

$$\sigma = \frac{10\ \mathrm{V}/\sqrt{2}}{10^{150/20}} \approx 0.224\ \mu\mathrm{V}. \tag{3}$$

With AUTO ZERO enabled, the effective rms noise increases by approximately $3\,\mathrm{dB}$ due to the difference of two measurements required to produce the sampled value [19], corresponding to a factor of $\sqrt{2}$. In addition, the noise at full-scale input voltage may increase by approximately $50\,\%$. The resulting effective rms noise at full scale is therefore estimated as

$$\sigma_{\mathrm{eff}} \approx 0.224\sqrt{2} \cdot 1.5 = 0.474\ \mu\mathrm{V}. \tag{4}$$

To achieve a target $\sigma_{\bar{x}}$ of $0.01\,\mu\mathrm{V/V}$ at $10\,\mathrm{V}$, corresponding to $0.1\,\mu\mathrm{V}$, the required number of independent readings becomes

$$R = \left(\frac{0.474}{0.1}\right)^2 \approx 23. \tag{5}$$

This estimate illustrates that extraction of stable transfer non-linearity at the $0.01\,\mu\mathrm{V/V}$ level requires substantial averaging even under carefully controlled metrological conditions and very low noise contribution from the drift-free PJVS voltages.

C. Initial Linearity Results

Fig. 7 shows the deviation from perfect linearity measured for DMM1, DMM2, and their numerical average. The deviations shown are detrended by removing their best-fit gain and offset terms, such that the remaining deviation $\varepsilon_{\mathrm{lin}}$ represents only the residual transfer non-linearity. The five consecutive readings acquired at each PJVS step in every sweep were averaged to suppress short-term white noise contributions. The resulting mean values $\varepsilon_{\mathrm{lin}}(V_{\mathrm{in}})$ from twelve repeated sweeps were then treated as independent realizations for the estimation of the standard deviation of the mean, thereby reducing sensitivity to short-term temporal correlation effects between consecutive readings. Nevertheless, as shown on Fig.

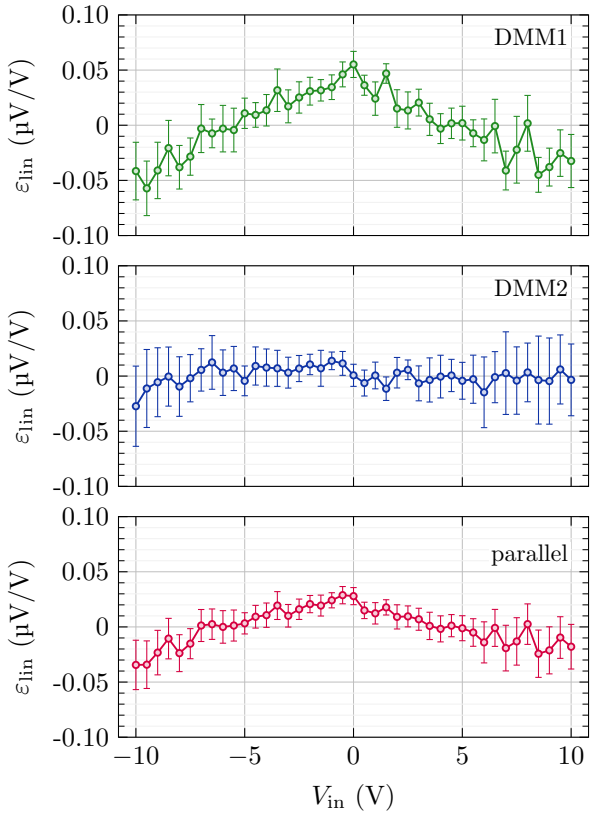

Fig. 7. Non-linearity for NPLC = 10, five samples per point, twelve sweeps. Top plot shows result for DMM1, the middle plot shows results for DMM2, and bottom plot shows the averaged result. The error bars shows resulting standard deviation of the mean.

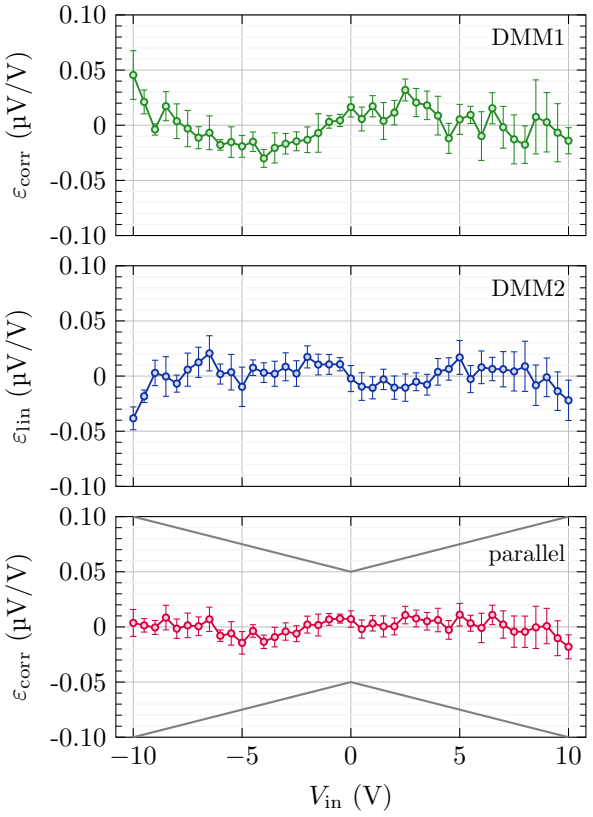

Fig. 8. Residual non-linearity for NPLC = 50, five samples per point, six sweeps, after applying a 3rd-order polynomial correction to the averaged DMM1 data. Grey lines in the bottom plot indicate DMM short-term transfer accuracy specification.

7, the $\sigma_{\bar{\varepsilon}}$ achieved was higher than expected, especially near the input voltage extremes. These results further demonstrate that extraction of sub-µV/V non-linearity requires careful metrological practice. In particular, successful observation of the residual transfer characteristic depends on sufficiently low environmental temperature variation, minimized thermoelectric effects, controlled measurement timing, and averaging depth adequate to suppress stochastic noise below the target non-linearity level.

Both DMMs exhibited smooth and repeatable non-linearity profiles. However, the detailed shapes of the two transfer characteristics are not identical and DMM1 shows a significantly stronger non-linearity fingerprint. For that reason, the averaged response generally remains between the characteristics of the individual DMMs, indicating that averaging alone does not fundamentally improve the linearity beyond the best individual instrument. This behavior is consistent with eq. (1), indicating that the observed transfer non-linearity contains both partially correlated systematic components and uncorrelated stochastic contributions.

D. Corrected Results

As DMM1 showed a noticeable non-linearity, its results using NPLC = 10 were fitted with a polynomial model. A third-order polynomial was selected as the lowest-order practical model capable of reproducing the dominant transfer characteristic while reducing the risk of over-fitting measurement noise. A third-order polynomial, $P(v)$, was fitted to the deviation data (ε_i) as a function of the reference voltage (v_i). The model for the deviation is:

$$P(v) = a_0 + a_1 v + a_2 v^2 + a_3 v^3 \tag{6}$$

The coefficients a_j are found using the method of least squares, which minimizes the sum of the squared residuals, S:

$$\begin{aligned} S &= \sum_{i=1}^{M} \left(\varepsilon_i - P(v_i)\right)^2 \\ &= \sum_{i=1}^{M} \left(\varepsilon_i - (a_0 + a_1 v_i + a_2 v_i^2 + a_3 v_i^3)\right)^2, \end{aligned} \tag{7}$$

where M is the number of points used for interpolation (41). The fit was calculated from the DMM1 deviations (see Fig. 7, DMM1 plot) using results in the span $-10.000\,060\,6\,\text{V} \le v_i \le 10.000\,060\,6\,\text{V}$.The corrected deviation, $\varepsilon_{\text{corr}}$, is the residual of this fit:

$$\varepsilon_{\text{corr},i} = \varepsilon(v_i) - P(v_i). \tag{8}$$

Additional measurements were conducted using NPLC = 50, with DMM1 corrected using (8). Fig. 8 shows detrended results for corrected DMM1, DMM2 (uncorrected) and their average.

The non-linearity observed at these two integration times is largely independent of NPLC for sufficiently long integration periods. The linearization derived from the NPLC $= 10$ measurements can be successfully applied to measurements performed at larger NPLC settings. After correction, the remaining deviation is substantially reduced and is observed to remain within the transfer linearity specification of the instruments across the range measured.

These results indicate that averaging and polynomial correction act as complementary mechanisms. Averaging reduces the partially uncorrelated error components, while polynomial correction compensates the remaining systematic transfer characteristic.

VI. Mitigation Strategies and Discussion

The experimental results presented in Sections IV and V demonstrate that the effectiveness of parallel averaging is fundamentally limited by the correlation structure of the underlying non-linearity mechanisms. While stochastic noise components follow the expected $1/\sqrt{N}$ scaling, the linearity improvement remains strongly dependent on the architecture.

For the SAR digitizers investigated, harmonic distortion components remained strongly correlated between channels. The polarity inversion experiments further showed that even-order harmonic phases changed under signal inversion, while odd-order harmonic phases remained substantially unchanged. As a consequence, averaging alone was unable to provide significant reductions in THD despite improving SNR significantly. For the SAR ADCs investigated, SINAD is noise-dominated and could also be improved by parallel operation of multiple channels.

Conversely, the IADC systems measured exhibited partially correlated transfer non-linearity. Although averaging alone did not improve the transfer characteristic beyond the best individual DMM, the residual deviation formed a stable and repeatable fingerprint that could be effectively compensated using a third-order polynomial correction. This demonstrates that averaging and calibration act as complementary mechanisms once stochastic noise has been sufficiently suppressed.

These observations are conceptually related to calibration approaches developed for time-interleaved ADC systems, where systematic channel-dependent mismatch errors must be corrected digitally rather than suppressed through averaging alone [15]. In particular, the tracking-based hybrid calibration approach presented by Sung and Choi highlights the importance of using calibrated channel data when the dominant error mechanisms remain correlated between parallel paths.

More generally, the results presented suggest that future improvement of parallel high-linearity digitizers will likely require architectures specifically designed to reduce interchannel error correlation. One possible direction is the use of digital post-correction methods based on dynamic transfer models, such as the state-space and phase-plane correction structures described by Lundin [22]. This approach explicitly models the converter transfer dynamics and may therefore provide improved compensation of residual correlated distortion mechanisms.

TABLE VI
Summary of correlation properties and effectiveness of averaging and calibration.

Architecture	Dominant limitation	Corr.	Averaging benefit	Calibration benefit
SAR ADC	Harmonic distortion	Strong	Limited	Not evaluated
IADC	Static transfer non-linearity	Partial	Limited	Strong

Another potentially important strategy is the intentional de-correlation of transfer non-linearity between channels. In particular, introducing controlled offset differences between parallel channels could break the periodicity of the underlying non-linearity patterns, potentially improving the effectiveness of averaging and calibration. Such approaches were not investigated in the present work due to implementation constraints but represent one possible direction for future research.

Overall, the results presented indicate that future progress in ultra-high-linearity digitizer systems will increasingly depend on the combined use of averaging, intentional de-correlation, and calibration-based correction methods rather than averaging alone. The experimental observations for both SAR and IADC architectures are consistent with the correlation-dependent averaging model of eq. (1), which predicts that the achievable improvement is fundamentally limited by the degree of inter-channel error correlation.

VII. Conclusion

This work investigated the effectiveness of parallel operation for improving the linearity of state-of-the-art high-linearity digitizers in both AC and DC operating regimes. Experimental results obtained using SAR ADC systems and IADC systems showed that the achievable improvement is fundamentally determined by the correlation structure of the underlying error mechanisms.

For both SAR architectures investigated, parallel averaging provided the expected $\sqrt{N}$ improvement in SNR and SINAD, confirming that the dominant noise components are largely uncorrelated. However, reduction in harmonic distortion remained limited due to strong correlation of the dominant distortion mechanisms between channels. Harmonic phase analysis further showed that the phases of even-order harmonics change under polarity inversion, while they remain practically unchanged for odd-order harmonics explaining the limited THD improvement achieved through averaging alone.

The IADC system exhibited substantially different behavior. Although averaging alone did not improve the transfer characteristic beyond the best individual instrument, the residual non-linearity formed a stable and repeatable fingerprint that could be effectively compensated using polynomial correction. For the IADC systems investigated, calibration-based correction proved effective once averaging reached its architecture-dependent limit. Table VI summarizes the correlation proper-

ties observed and the effectiveness of averaging and calibration for the digitizer architectures investigated.

In summary, parallel averaging remains effective for improving the noise-limited performance of high-linearity digitizers, whereas further improvement of linearity requires intentional decorrelation and calibration-based correction of residual correlated errors.

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