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Biography:

Albert Wang received the BS degree from Tsinghua University and the PhD degree from State University of New York at Buffalo. He is a Professor of Electrical and Computer Engineering at University of California, Riverside, USA. He was a Staff Design Engineer at National Semiconductor Corp in the Silicon Valley before joining Illinois Institute of Technology as an Assistant Professor of Electrical and Computer Engineering. His research covers semiconductor devices, AMXRF ICs, design-for-reliability for ICs, 3D heterogeneous integration, emerging devices and circuits, and LED visible light communications. He published two books and 315+ peer-reviewed papers, and holds 16 U.S. patents. His editorial board services include IEEE TCAS I, IEEE EDL, IEEE TCAS II, IEEE TED, IEEE JSSC, and IEEE TDMR. He is IEEE Distinguished Lecturer for IEEE EDS and was IEEE Distinguished Lecturer for IEEE CASS and SSCS. He was President of IEEE Electron Devices Society. He was Chair for the IEEE CAS Analog Signal Processing Technical Committee. His other committee services include the International Technology Roadmap for Semiconductor (ITRS) Committee, IEEE Heterogeneous Integration Roadmap (HIR) Committee, IEEE 5G Initiatives Committee, IEEE Smart Lighting Project Roadmap Committee and IEEE Fellow Committee. He was General Chair of IEEE Electron Devices Technology and Manufacturing Conference (EDTM2021) and IEEE Radio-Frequency Integrated Circuits Symposium (RFIC2016). He served as a Program Director of the National Science Foundation, USA (2019-2021). He was recipient IEEE J. J. Ebers Award and IEEE EDS Distinguished Service Award. Wang is a Fellow of National Academy of Inventors, an IEEE Fellow and an AAAS Fellow.

Listen: ESD Protection is About Circuit Design

On-chip ESD protection design is one of the most challenging IC reliability problems, still full of black magics. A common misconception has been that ESD protection design is about device design, which largely contributed to ESD design failures in IC design practices. It is time to reconsider on-chip ESD protection – it is a circuit design task within IC designs. A correct design mindset, along with comprehensive understanding of ESD protection details, becomes essential to successful on-chip ESD protection design for ICs, particularly for large, complex, high-performance ICs at advanced technology nodes and in emerging technologies. This talk reviews the evolution of and every detail of on-chip ESD protection circuit designs, from an IC design perspective. The discussion will cover ESD fundamentals, ESD Design Overhead Effect, ESD Design Window, ESD design prediction, low-parasitic ESD protection designs, holistic ESD-IC co-design methodologies, various CAD-based ESD protection design techniques, challenges of ESD protection design for RF ICs up to millimeter wave frequency and high-throughput IC beyond 10Gbps, full-chip ESD protection circuit physical design verification CAD algorithms and methods, ESD protection design for 3D chiplet-based chips using heterogeneous integration technologies, emerging CDM ESD protection design challenges, and non-traditional above-IC ESD protection concepts. Perspectives for future ESD protection designs will be outlined. The discussion will be supported by numerous practical ESD protection design examples. The takeaway: an IC designer should know about and can do good ESD protection designs.