5th IEEE International Conference on
VLSI Systems, Architecture, Technology and Applications
(VLSI SATA) May 23-24, 2025

https://www.vlsisata.in/

Venue: Amrita Vishwa Vidyapeetham, Amrita School of Engineering, Bangalore

Theme: Power Aware and AI Supported VLSI Innovation

The 5th IEEE VLSI SATA (Systems, Architecture, Technology and Applications) conference would promote knowledge building, engineering education, research and development activities, and networking to establish and identify research groups and collaboration opportunities. The 2025 edition of VLSI SATA is scheduled during May 23-24. The theme of the conference is "Power Aware and AI Supported VLSI Innovation." The conference is the flagship annual conference of IEEE Circuit and Systems Society (CASS) Bangalore. It is jointly organized and hosted by Amrita School of Engineering (ASE), Bangalore.

IMPORTANT DATES

Paper Submission Deadline:
16 March, 2025
Notification of Acceptance:
Rolling basis in 3 weeks
Camera Ready:
2 weeks after acceptance

WORKSHOP, TUTORIAL, INVITED PAPERS

Proposals for the Workshops/Tutorial/Invited Papers are invited from experts to be conducted in conjunction with the main conference. The length of the workshops can be half day or full day. Workshop with hands-on may attract more participants. In-depth tutorial on emerging technology within the scope of the conference would be proposed to attract scholars, graduate students and young professionals. Additionally, invited paper is also invited from senior and established researchers. Invited papers would also be submitted to be included in the IEEE Xplore on acceptance and presentation.

The following information is required from workshop/tutorial organizers. Organizers details like Name, Designation, Affiliation, Title of the workshop, Abstract, Brief profile of organizer(s), Photograph, Length of the workshop/tutorial, Targeted audience, Plan for attracting audience, etc. Contact for more details to the respective co-chairs. Please submit the workshop/Tutorial/Invited Paper proposal in pdf format via CMT submission page given below.

Workshop Co-Chairs
Sunitha R, *PhD ASE*
Praveen Jaraut, *PhD, ASE*
Vishnu Nandan, *PhD, ASE*

Tutorial Co-Chairs
Paramasivam C, *PhD ASE*
Shailashree N, *PhD, RVCE*
Uma Maheshwari, *PhD, ASC*

Invited Papers/Keynote Co-Chairs
Jitendra Bahadur, *PhD ASE*
Sushant Shendre, *PhD, ASE*
Abhilash R, *PhD, ASE*

https://cmt3.research.microsoft.com/VLSISATA2025

Special Session
Expert who would like to conduct/organize special session during the event is also invited. Any theme related and within the scope of the conference can be proposed.

Local Arrangement Co-Chairs
Sagar B, *ASE*
Ganapathi H, *PhD ASE*

Exciting Opportunity for Sponsorers
Please contact General Co-Chairs

For more details, please visit:
https://www.vlsisata.in/
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For any queries, contact us on:
https://www.vlsisata.in/

VLSI SATA 2025 will feature the presentation and discussion of new findings in the theory, methodology, design, and applications of VLSI. It serves as a global forum for researchers, academicians, and practitioners to share their ongoing theoretical research endeavours, innovative system and design solutions and practical VLSI applications. The conference program includes traditional paper presentations, engaging workshops, and keynote addresses by distinguished educational experts and authorities.

CALL FOR PAPERS
Submission https://cmt3.research.microsoft.com/VLSISATA2025

Prospective authors are invited to submit their full and original research papers in electronic (PDF) format, with the requirement that these papers should not have been submitted, published, or under consideration in any other conferences or journals.

SYSTEMS
- Reliable and/or Safe Embedded Electronics
- Systems for Testing
- Digital System Design and Validation
- Digital System and Circuits
- Memory Subsystems
- Memory Computing Systems
- HW/SW Co-design
- IoT Systems
- Cyber Physical Systems
- Embedded Operating Systems
- Analog and Mixed Signal Systems
- RF Circuits and Systems
- Low Power Systems
- Power Management Systems
- Data Converters
- High Speed Interfaces
- Reliable Systems
- Wireless Circuits and Systems
- CAD Tools and Methodologies for Design and Optimization

TECHNOLOGY
- 3D ICs
- MEMS, GaN, and SiC devices
- Layout Technology
- Physical Design
- Interconnect Technologies
- 3D Packaging and Wafer-level Packaging
- New Age Nanoelectronic Devices
- Electronic Design Automation
- Advanced CMOS Technology
- Advanced Packaging and Heterogeneous Integration Technology
- Process Technology

ARCHITECTURE
- Inter-chip Interconnect
- On-chip Interconnect
- Multicore and Manycore
- Data Centric Architecture
- System on Chip
- Embedded Processor Architecture in Vehicles
- High-performance Computing
- Embedded FPGA Reconfigurable Computing
- Built In Self Test (BIST)
- Design for Test Fault Tolerance
- Quantum Computing
- Network Security
- Side-channel and Fault Analysis
- Trusted Computing
- Hardware Trojan
- Functional Safety and Privacy
- Optical Interconnect Architecture
- Reliable Communication Architecture
- NoC for FPGA, ASIC, CMP and MPSoC
- Approximate Computing

APPLICATIONS
- IoT and Big Data Analytics
- AI-oriented Applications
- Video and Image Processing
- Applications Hardware Security and Trust
- ML-oriented Applications
- Wireless/Wired Communication Networks
- Automotive and Vehicular Networks
- RF Energy Harvesting
- Power Electronics Applications
- Biomedical and Healthcare Applications
- Sensors and Instrumentation Applications
- Signal Integrity Applications

SUBMISSION

Paper submission is through CMT paper management systems. If you already have CMT login; you can make use of that otherwise, you may need to create a login for CMT.
https://cmt3.research.microsoft.com/VLSISATA2025

Manuscript Preparation

Authors can submit their manuscript properly formatted as pdf file. Please find the template and author guidelines here.
https://www.ieee.org/conferences/publishing/templates.html
Use US Letter size in the case of MS Doc.

Overleaf

For overleaf, the template is available at:
https://www.overleaf.com/gallery/tagged/ieee-official

Page Length

Maximum manuscript length should be 6 pages. (Extra 1-2 page would cost significantly high amount). The paper must include an abstract of about 150 words and a maximum of five keywords.
Review/Survey paper is normally discouraged to be submitted in the conference.

Review Process

Each submitted paper will go several stages of screening: similarity check, format check, scope and quality check. Papers which qualify for review would be sent to minimum 3-reviewers for their comments before TPC makes a decision on the paper. The review process is DOUBLE BLIND. Please do not write author names on the paper. Authors of the accepted papers will be informed through email.
All accepted and presented papers in the conference would be submitted to IEEE Xplore for possible publication. The previous editions of the papers are available in both Xplorer as well as Scopus.

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PREVIOUS PUBLICATIONS

Please find the link of previous publications.
VLSI SATA (2015)
https://ieeexplore.ieee.org/xpl/conhome/7044910/proceeding
VLSI SATA (2016)
https://ieeexplore.ieee.org/xpl/conhome/7586733/proceeding
VLSI SATA (2022)
https://ieeexplore.ieee.org/xpl/conhome/10046417/proceeding
VLSI SATA (2024)
https://ieeexplore.ieee.org/xpl/

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