5th IEEE International Conference on

VLSI Systems, Architecture, Technology and Applications

(VLSI SATA) **May 23-24, 2025**

Designing Low-Dropout Regulators: Fundamentals to Advanced Techniques

Abstract for the Workshop

Many mixed-signal systems use low-dropout (LDO) regulators to provide dedicated supply rails for each functional block. By isolating circuits from both global VDD noise and each other's switching disturbances, LDOs preserve signal integrity. However, they require minimal input-output voltage differentials for maintaining the efficiency. Thus, LDOs are typically paired with switching converters like buck regulators for coarse voltage step-down, with LDOs filtering residual noise arising due to switching activity. LDO design involves inherent trade-offs like high power supply rejection ratio (PSRR) compromises transient speed, and vice versa. This tutorial derives core LDO topology from first principles through intuitive circuit analysis, avoiding heavy formalism. Two detailed design case studies of a high-PSRR LDO for noise-sensitive RF systems, and a fast-transient LDO for digital loads will be discussed. These will include the respective Cadence and MATLAB simulations. The latter half examines capacitor-less LDO architectures such as Flipped Voltage Follower (FVF), and Domino-like Buffered topologies, eliminating the need for off-chip capacitors without significant degradation in the performance. Recent case studies from JSSC, TCAS-I, and TPEL publications will be discussed to familiarize participants with state-of-the-art techniques.

Workshop Registration

Conference Registration

Speakers

Mr. Soham Lakhote
IISc Bangalore

Mr. Rahul Reji
IISc Bangalore

Mr. Koteswar Doddi
IISc Bangalore

VENUE: Amrita School of Engineering, Kasavanahalli, (Off Sarjapur Road) Bengaluru-560035