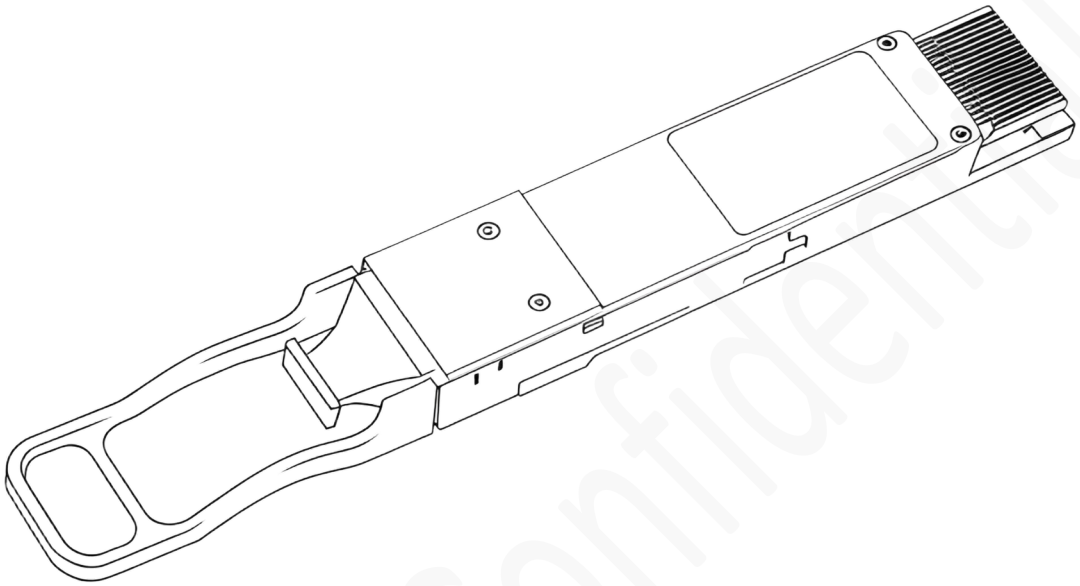
Product Datasheet

800G QSFP112-DD DR8 Transceiver



Application

- Data center & Networking Equipment
- Servers/Storage Devices
- High Performance Computing (HPC)
- Switches/Routers
- Telecom Central Offices (CO)
- Test and Measurement Equipment

1.0 Product Specification

1.1 Absolute Maximum Ratings (TC=25℃, unless otherwise noted)

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings will cause permanent damage and/or adversely affect device reliability.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Storage Temperature	TS	-40	-	+85	℃	
Maximum Supply Voltage	Vcc	-0.5	-	3.6	V	
Operating Relative Humidity	RH	5	-	95	%	No condensation
Control Input Voltage	V_I	-0.3	-	V_{CC}+0.5	V	

1.2 General Specifications (Tc=25℃, unless otherwise noted)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Operating Case Temperature	T_{OPR}	0	-	70	℃	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Maximum Power Dissipation	P_D	-	7.5	8	W	
Signaling Rate per Lane	SRL	-	53.125	-	GBd	PAM4
Two Wire Serial Interface Clock Rate	-	-100	-	400	kHz	
Power Supply Noise Tolerance (10Hz - 10MHz)	-	-	-	66	mV	
Rx Differential Data Output Load	-	-	100	-	Ohm	
Operating Distance (MMF@OM3)	-	-	-	60	m	
Operating Distance (MMF@OM4)	-	-	-	100	m	

1.3 Transmitter Characteristics (TC=25℃, unless otherwise noted)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Wavelength	λ_C	1304.5	1310	1317.5	nm	
Side-mode suppression ratio (SMSR)	SMSR	30	-	-	nm	
Average Launch Power, each lane	AOP_L	-4.6	-	4.0	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each lane	T_{OMA}	-2.6		3.5	dBm	2
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	3.4	dB	
Average Launch Power of OFF Transmitter, each lane	T_{OFF}	-	-	-30	dBm	
Extinction Ratio, each lane	ER	2.5	3.5	-	dB	
$RIN_{14}OMA$	RIN	-	-	-132	dB/Hz	
Optical Return Loss Tolerance	ORL		-	17.1	dB	
Transmitter Reflectance	T_R	-	-	-26	dB	3

Notes

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.
2. Even if max (TECQ, TDECQ) < 1.8dB, OMAouter (min) must exceed this value.
3. Transmitter reflectance is defined looking into the transmitter.

1.4 Receiver Characteristics (TC=25℃, unless otherwise noted)

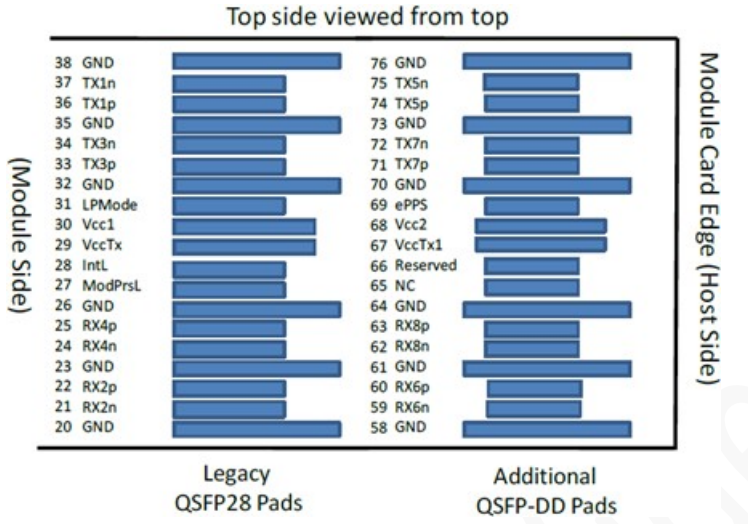
Parameter	Symbol	Min	Typical	Max	Unit	Notes
Wavelength	λ_C	1304.5	1310	1317.5	nm	
Damage Threshold, average optical power, each lane	AOP_D	5	-	-	dBm	
Average Receive Power, each lane	AOP_R	-6.3	-	4.0	dBm	
Receive Power (OMA_{outer}), each lane	OMA_R	-	-	3.5	dBm	
Receiver Reflectance	RR	-	-	-26	dB	
Receiver Sensitivity (OMA_{outer}), each lane	S_{OMA}	-	-	-4.4	dBm	1
Stressed Receiver Sensitivity (OMA_{outer}), each lane	SRS	-	-	-2.5	dBm	2

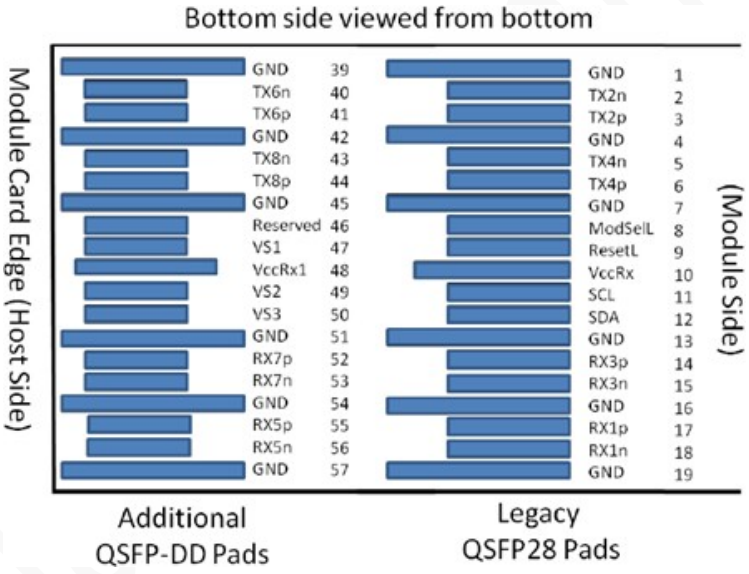
Conditions of stressed receiver sensitivity test						
Stressed eye closure for PAM4	SECQ		4.4		dB	
OMA_{outer} of each aggressor lane	OMA_{outer}		3.5		dBm	

Notes

1. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with TDECQ<=1.8 dB
2. Measured with conformance test signal at TP3 for the BER = 2.4x10-4

1.5 PIN Descriptions





PAD	Logic	Symbol	Description	Plug Seq[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	

6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select.	3B	
9	LVTTL-I	ResetL	Module Reset.	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present.	3B	
28	LVTTL-O	IntL	Interrupt.	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power Mode	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	

41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	
50		VS3	Module Vendor Specific 3	3A	
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	

76		GND	Ground	1A	1

Notes:

[1] QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

[2] VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 7. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

[3] All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

[4] Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B (see Figure 2 for pad locations).Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B, followed by 3A, 3B.

2.0 Product Information

Data Rate	Factor		Optical	Wavelength	Reach
800G	QSFP112-DD	DR8	MPO	1310nm	500m

ESD Safety Cautionsy

This transceiver is specified as ESD threshold 1KV for high speed data pins based on Human Body Model per ANSI/ESDA/JEDECJS-001. The units are subjected to 15kV air discharges during operation and 8kV direct contact discharges to the case. However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Important Notice

The performance figures, data, and any illustrative material presented in this datasheet are typical and must be explicitly confirmed in writing by Quantex before they are deemed applicable to any specific order or contract.

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3.0 Revision Record

Rev.	Comments	Date
A01	Initial Release	