Fundamentals of Electronics and Communication Engineering Lab		Semester	1/II
Course Code	1BBEEL107/207	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	0:0:2:0	SEE Marks	50
Total Hours of Pedagogy	15	Total Marks	100
Credits	01	Exam Hours	03
Examination type (SEE)	**Practical**		

Course outcome (Course Skill Set)

At the end of the course, the student will be able to

1. Apply the operating principles of diodes, transistors, and MOSFETs to construct and test basic analog circuits.
2. Implement operational amplifier configurations such as inverting, non-inverting, integrator, and differentiator for analog signal processing applications.
3. Analyze the functionality of logic gates and combinational circuits including adders, subtractors, and code converters using digital ICs.
4. Investigate amplitude modulation to explore fundamental analog communication techniques.
5. Develop solutions to open-ended electronic design problems by selecting appropriate components, constructing circuits, and interpreting results to meet defined objectives.

Note:

1. The laboratory syllabus consists of PART-A and PART-B. While PART-A has 6 conventional experiments, PART-B has 6 typical open-ended experiments. The maximum marks for the laboratory course are 100.
2. Both PART-A and PART-B are considered for CIE and SEE.
3. Students have answer 1(one) question from PART-A and 1(one) question from PART-B.
   a. The questions set for SEE shall be from among the experiments under PART-A. It is evaluated for 70 marks out of the maximum 100 marks.
   b. The open-ended question set for SEE shall be any other open-ended question and not selected from the experiments under PART-A. It shall be evaluated for 30 marks.
4. For continuous internal evaluation, during the semester, classwork, the typical open-ended questions shall be from PART-B, and any other similar questions to enhance the skill of the students

PART – A
CORE/BASIC HARDWARE EXPERIMENTS

1. Design and Testing of Half-Wave and Full-Wave Rectifiers With and Without Filter for Determining Ripple Factor, Voltage Regulation, and Efficiency
2. Design and Testing of Bridge Rectifier With and Without Filter for Determining Ripple Factor, Voltage Regulation, and Efficiency
3. Analysis of Input and Output Characteristics of a Bipolar Junction Transistor in Common Emitter Configuration
4. Study of Transfer and Drain Characteristics of a MOSFET in Common Source Configuration
5. Investigation of Op-Amp in Inverting and Non-Inverting Modes with Gain Measurement
6. Study of Truth Tables for OR, AND, NOT, NAND, and NOR Gates Using Basic and Universal Gates

PART – B
OPEN ENDED HARDWARE EXPERIMENTS

1. Design and Testing of Clipping and Clamping Circuits to obtain desired Transfer Characteristics
2. Design and test a single stage bipolar junction transistor amplifier to obtain desired gain and bandwidth requirements.

3. Testing of Op-Amp as voltage follower and a weighted summer with waveform analysis.
4. Design and Testing of Integrator and Differentiator Circuits using Op-Amp with Waveform Analysis
5. Amplitude Modulation using Discrete Components for Given Specifications.
6. Realization of Half/ Full Adder and Subtractor using Logic Gates.

Suggested Learning Resources:

Text books:

1. David A Bell, Electronic Devices and Circuits, 5th Edition, Oxford University Press, 30th Impression, 2025.
2. Ramakanth A Gayakwad, Op-amps and Linear Integrated Circuits, 4th Edition, Pearson Education, 2015.
3. John G. Proakis, Masoud Saleh, Fundamentals of Communication Systems, Second Edition, Pearson Educations, Inc., 2014.
4. D.P Kothari and I J Nagrath, Basic electronics, Second Edition, McGraw Hill Education Pvt ltd, 2018.
5. M.Morris Mano and Michael D.Ciletti, Digital Design - With an Introduction to the Verilog HDL, VHDL and System Verilog 6th Edition, Pearson Education Inc, 2024.
6. Robert L. Boylestad, Louis Nashelsky, “Electronic Devices and Circuit Theory", 11th Edition, PHI, 2016.

Web links and Video Lectures (e-Resources):

- Introduction to Basic Electronics: https://nptel.ac.in/courses/122106025
- Digital Electronic Circuits: https://nptel.ac.in/courses/108105132

Teaching-Learning Process (Innovative Delivery Methods):

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. While explaining each experiment, also focus on the application of that particular experiment in the electronics industry.
2. Students need not memorize pin diagrams, these can be provided to the student during CIE and SEE.

Assessment Structure:

The assessment for each course is equally divided between Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE), with each component carrying **50% weightage** (i.e., 50 marks each).

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The CIE marks awarded shall be based on the continuous evaluation of the laboratory report using a defined set of rubrics. Each experiment report can be evaluated for 25 marks. The laboratory test (duration 03 hours) at the end of the last week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 100 marks and scaled down to 25 marks. For both CIE and SEE, the student is required to conduct one experiment each from both Part A and Part B.

- To qualify and become eligible to appear for SEE, in the **CIE component**, a student must secure **a minimum of 40% of 50 marks**, i.e., **20 marks**.
- To pass the **SEE component**, a student must secure **a minimum of 35% of 50 marks**, i.e., **18 marks**.
- A student is deemed to have **successfully completed the course** if the **combined total of CIE and SEE is at least 40 out of 100 marks**.

Rubrics for SEE / CIE test:

Performance Indicators	Superior	Good	Fair	Needs Improvement	Unacceptable
Fundamental Knowledge (4) (PO1)	The student has good in-depth knowledge of the topics related to the course (4)	Student has good knowledge of some of the topics related to course (3)	Student is capable of narrating the answer but not capable to show in depth knowledge (2)	Student has only marginally understood the concepts (1)	Student has not understood the concepts (0)
Design Of Experiment (5) (PO2 & PO3)	Student is capable of discussing the design with its merits and de-merits (5)	Student is able to explain the design, but not able to discuss all the merits and de-merits (4)	Student is capable of explaining the design (3)	Student has made correct assumptions but is barely capable of explaining the design (2)	Student has made wrong assumptions for the design (1)
Implementation (8) (PO3 & PO8)	Student effectively implements the design using the most suitable technique for an optimal solution, with clear and complete explanation of the approach. (7-8)	Student is able to implement the design using an appropriate technique and provides a satisfactory explanation of the steps taken (5-6)	Student is able to implement the design with a partially suitable approach and gives a basic explanation, though some steps may lack clarity. (3-4)	Student is able to implement the design with significant support, and explanation is minimal or lacks coherence. (2)	Student struggles to implement the design and is unable to provide a meaningful explanation (1)
Result &Analysis (5) (PO4)	Student is able to run the program on various cases and compare the result with proper analysis. (5)	Student will be able to run the program for all the cases. (4)	Student will be able to run the code for few cases and analyze the output. (3)	Student will be able to run the program but not able to analyze the output. (2)	Both circuits set up and analysis are poor (1)
Demonstration (8) (PO9)	The lab record is well-organized, with clear sections (e.g., Introduction, Method, Results, Conclusion). Transitions between sections are smooth. (7-8)	The lab record is organized, with clear sections, but some sections are not well-defined. (5-6)	The lab record is organized but some sections are unclear or incomplete. (3-4)	The lab record lacks clear organization or structure (2)	The lab record is poorly organized, with missing or unclear sections. (1)