Digital System Design using Verilog		Semester	3
Course Code	**BEC302**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	03
Examination nature (SEE)	Theory/Practical		

Course objectives:

This course will enable students to:

- To impart the concepts of simplifying Boolean expression using K-map techniques and Quine-McCluskey minimization techniques.
- To impart the concepts of designing and analyzing combinational logic circuits.
- To impart design methods and analysis of sequential logic circuits.
- To impart the concepts of Verilog HDL-data flow and behavioural models for the design of digital systems.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Show Video/animation films to explain the different concepts of Linear Algebra & Signal Processing.
- Encourage collaborative (Group) Learning in the class.
- Ask at least three HOTS (Higher order Thinking)questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and have discussions on the topic in the succeeding classes.
- Give Programming Assignments.

MODULE-1

Principles of Combinational Logic: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps-up to 4 variables, Quine-McCluskey Minimization
Technique. Quine-McCluskey using Don't CareTerms.(Section3.1to3.5ofText1).

MODULE-2

Logic Design with MSI Components and Programmable Logic Devices: Binary Adders and Subtractors, Comparators, Decoders, Encoders, Multiplexers, Programmable Logic Devices(PLDs) (Section5.1to5.7 ofText2)

MODULE-3

Flip-Flops and its Applications: The Master-Slave Flip-flops(Pulse-Triggered flip-flops):SR flip-flops, JK flip flops, Characteristic equations, Registers, Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers, Design of Synchronous mod-n Counter using clocked T, J K, D and SR flip-flops.(Section 6.4, 6.6 to 6.9 (Excluding 6.9.3)of Text2)
MODULE-4
Introduction to Verilog: Structure of Verilog module, Operators, Data Types, Styles of Description. (Section1.1to1.6.2, 1.6.4 (only Verilog),2 of Text 3) **Verilog Data flow description:** Highlights of Data flow description, Structure of Data flow description.(Section2.1to2.2(only Verilog) of Text3)
MODULE-5
Verilog Behavioral description: Structure, Variable Assignment Statement, Sequential Statements, Loop Statements, Verilog Behavioral Description of Multiplexers (2:1, 4:1, 8:1). (Section 3.1 to 3.4 (onlyVerilog)of Text 3) **Verilog Structural description**: Highlights of Structural description, Organization of structural description, Structural description of ripple carry adder.(Section4.1 to 4.2 of Text 3)

PRACTICAL COMPONENT OF IPCC *(Experiments can be conducted either using any circuit simulation software or discrete components)*

Sl.N	Experiments
1	To simplify the given Boolean expressions and realize using Verilog program
2	To realize Adder/Subtractor(Full/half)circuits using Verilog data flow description.
3	To realize 4-bit ALU using Verilog program.
4	To realize the following Code converters using Verilog Behavioral description a)Gray to binary and vice versa b)Binary to excess3 and vice versa
5	To realize using Verilog Behavioral description:8:1mux, 8:3encoder, Priority encoder
6	To realize using Verilog Behavioral description:1:8Demux, 3:8 decoder,2 –bit Comparator
7	To realize using Verilog Behavioral description: Flip-flops: a)JK type b)SR type c)T type and d)D type
8	To realize Counters-up/down (BCD and binary)using Verilog Behavioral description.
Demonstration Experiments (For CIE only–not to be included for SEE) Use FPGA/CPLD kits for down loading Verilog codes and check the output for interfacing experiments.	
9	Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps).
10	Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Simplify Boolean functions using K-map and Quine-McCluskey minimization technique.
2. Analyze and design for combinational logic circuits.
3. Analyze the concepts of Flip Flops(SR, D,T and JK) and to design the synchronous sequential circuits using Flip Flops.
4. Model Combinational circuits (adders, subtractors, multiplexers) and sequential circuits using Verilog descriptions.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions

should not be more than 20 marks.

- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Suggested Learning Resources:
Books

1. Digital Logic Applications and Design by John MYarbrough,Thomson Learning,2001.
2. Digital Principles and Design by Donald DGivone,McGrawHill, 2002.
3. HDL Programming VHDL and Verilog by Nazeih M Botros, 2009 reprint, Dream techpress.

ReferenceBooks:

1. Fundamentals of logic design, by Charles H Roth Jr., Cengage Learning
2. Logic Design, by Sudhakar Samuel, Pearson/Sanguine, 2007
3. Fundamentals of HDL,by Cyril PR, Pearson/Sanguine2010

Web links and Video Lectures (e-Resources):

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning
Programming Assignments/Mini Projects can be given to improve programming skills.